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High Speed CMOS Comparator Design for Dynamic Power Management in IoT Applications

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Article Info
Volume 83
Page Number: 6607 - 6614
Publication Issue:
May- June 2020

Article History
Article Received: *19 November 2019*
Revised: *27 January 2020*
Accepted: *24 February 2020*
Publication: *18 May 2020*

Abstract:
By 2020, seven connected devices are projected to correspond to each human being[12].Such connected devices will follow the Internet of Things (IoT) and get into every aspect of human life. In order to power these devices,new strategies should recreated as these devices will not only have a dynamic load due to multiple features, but also dynamic sources if the rechargeable battery is supplemented by resourceful energy harvesting. The need for fine-grained power management in electronic ICs has resulted in the design and implementation of compact low drop regulators(LDOs) that are deeply embedded inside logic blocks[13]. Power Supply network(PSN) requires low drop out (LDO) regulators with high speed and low power comparators. A revised comparator architecture is modeled in 180 nm CMOS technology in order to achieve high speed and low power.A 2.5 volt comparator has been made. The engineering parameters of Cadence Virtuoso software 0.18 μm are used for development. Designed comparator demonstrates reduced power consumption and delay compared to existing comparators. For applications needing less energy dissipation, good accuracy and high resolution, comparators are used..

Keywords*: Low power Comparator, low dropout regulators, Cadence Virtuoso tools, IOT.*

Introduction:

Comparator is a circuit which compares two input voltages in which one is analog input and other is reference voltage and outputs binary 0 or 1 depending on comparison. It is basically a 1 bit analog to digital converter. In ADCs sample and hold circuit samples the analog input signal and the sampled signal is given to comparator, depending on reference voltage it produces digital output which is equivalent to analog input signal [1]. Comparators are used in all ADCs requiring less power dissipation, high speed, low noise, less offset voltage, good slew rate etc. Different types of comparators are available namely open loop comparator, regenerative comparator and combination of both open loop and regenerative comparator (cascaded comparators) [2]. Open loop compactors are basically single and two stage differential amplifiers without compensation and feedback loop. Regenerative comparators use positive feedback to improve the performance [3]. Comparator circuits can also be built by separating the comparators into number of cascaded stages. This helps in reducing the total propagation delay time and hence can be used in high speed applications like radar receivers and LAN interfaces.

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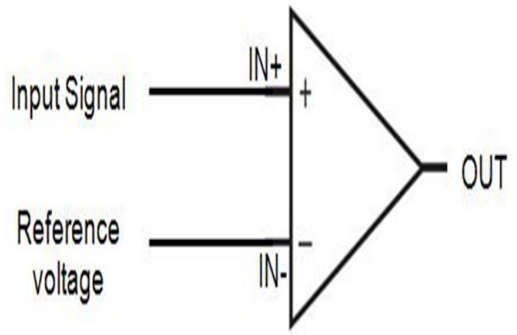

Fig -1. Symbol of comparator

Above figure shows the symbol of comparator. It is basically operational amplifier because every comparator has one or many of the same characteristics as a high gain amplifier. The

VoltageV_p applied to the positive terminal of the comparator gives output 1 if voltage V_n applied to negative terminal is
less or equal to V_p or else the output of the comparator gives 0 [4].
Power management is essential in all battery-powered portable devices such as cellular phones and PDAs in order to reduce the standby power and prolong the battery runtime. Low-dropout regulators (LDOs) are one of the most critical power management modules, as they can provide regulated low-noise and precision supply voltages for noise-sensitive analog blocks. With the widespread proliferation of modern portable devices, ever more stringent performance requirements of the LDO are needed. First, low dropout voltage across the pass device of the LDO is required provide high power efficiency. In addition, the increased level of integration in portable devices not only demands the LDO to deliver high load current, but also requires the no-load quiescent current of the LDO to be minimized for improving the current efficiency [5]. Good load transient response with small output-voltage variation including overshoots and undershoots upon load switching is critical to prevent an accidental turn off or resetting of the portable device. These four major performance requirements of the LDO, including low dropout voltage, high output current, low no-load quiescent current, and small output transient undershoots and overshoots are, however, difficult to achieve simultaneously.

I. Characterization of a Comparator

A. Static characteristics

Gain

The ideal aspect of this model is the way in which the output makes a transition between VOL and VOH. The output changes states for an input change of ΔV, where ΔV approaches zero [6]. The gain is given as

$$\text{Gain} = A_V = \lim_{\Delta v \to 0} \frac{VoH - VoL}{\Delta V} \qquad (1)$$

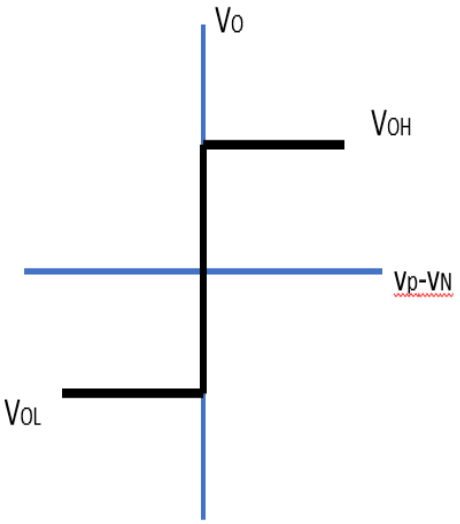

Fig -2. Ideal transfer curve

Offset Voltage

A mismatch in the threshold voltages and the Trans conductance parameters of the transistor generates offset voltage in comparator. If the output did not change until the input difference reached a value of VOS then the difference would be defined as the offset voltage [7].

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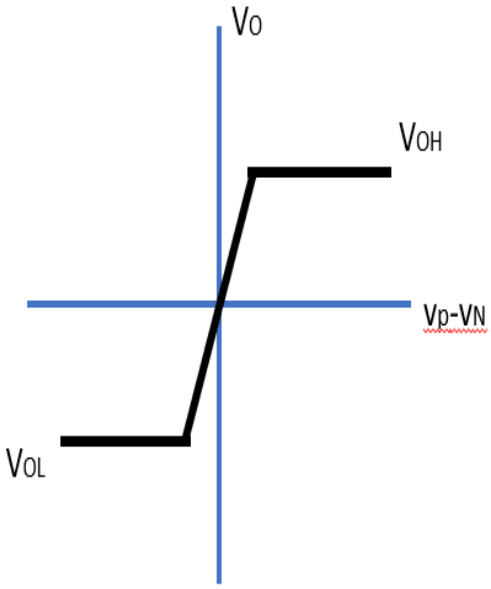

Fig -3. Transfer curve of a comparator including offset voltage and noise

B. Dynamic characteristics

Propagation Delay

Propagation delay is defined as at how much speed the amplifier responds with applied input [8].

Propagation delay time = (rising propagation delay time + falling propagation delay time)/2 (2)

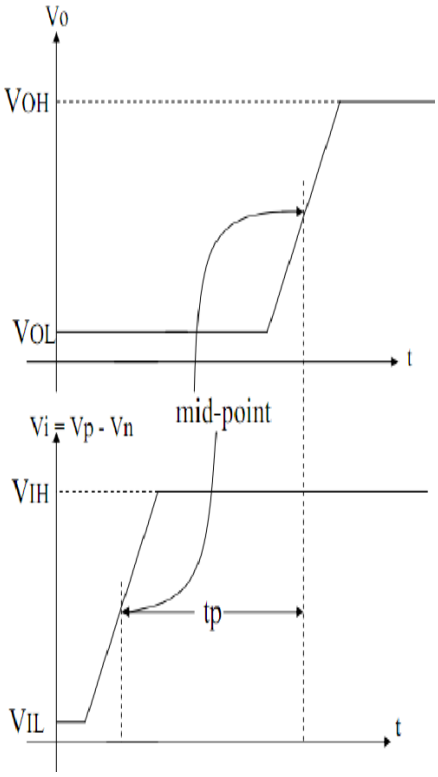

Fig -4. Propagation delay curve

III. TWO STAGE OPEN LOOP COMPARATOR

Comparator requires differential input and high gain to achieve desirable resolution. As a result two stage operational amplifiers can be used as a comparator. Comparator requires large bandwidth as possible so that faster response can be achieved. This is done by making two stage operational amplifiers as an open loop mode, thus no compensation is required [9].The advantage of this comparator is to provide high gain, large output voltage swing andfor high speed, disadvantage is that it consumes morepower. Hence, it is not suitable and low power applications.

High speed comparators should have a propagation delay time as small as possible. To achieve this goal, one must understand the requirement for fast comparator. This is best understood by separating the comparator into a number of cascading stages. So, this three cascading stages consists of input pre amplification stage, latch stage and output post amplification stage [10].

Pre amplification stage consists of current mirror single stage differential amplifier with high gain and low slew rate. This stage improves sensitivity of the comparator by isolating input from kickback noise and amplifying the smallest minimum input voltage

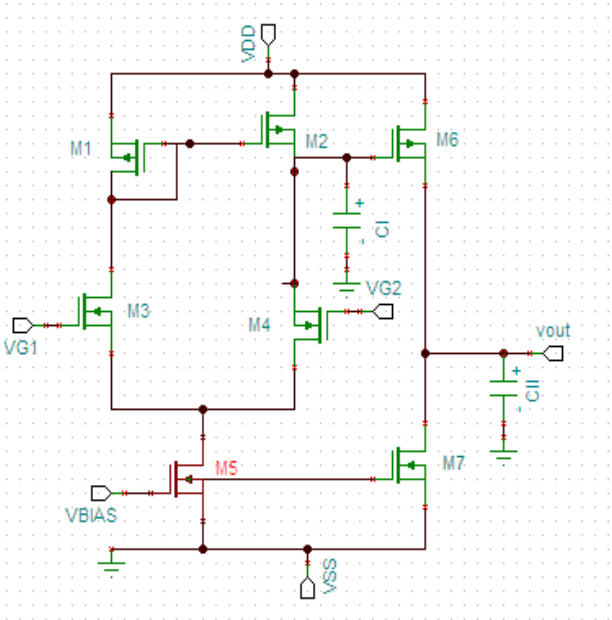

Fig -5.Two stage open loop comparator used to find initial states

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Small signal gain of the comparator as given by

$$Av(0) = \left(\frac{gm1}{gds2+gds4}\right)\left(\frac{gm6}{gds6+gds7}\right) \quad (3)$$

Two stage comparator consists of two pole, first and second stage output poles P1 and P2 respectively are given as

$$p1 = -\frac{(gds2+gds4)}{CI} \quad (4)$$

Where CI is the sum of capacitance connected to the output of first stage.

$$p2 = -\frac{(gds6+gds7)}{CII} \quad (5)$$

Where C_{II} is the sum of capacitance connected to the output of second stage.

II. Experimental results

Consider two stage open-loop comparator[11].The capacitances at the outputs of the first and second stages are C_I and C_{II} respectively. The approach is choose one of the input gates equal to a dc voltage and find the output voltage of the first and second stages when the other input gate is above and below the dc voltage on the first gate. Consider two cases for each of the previous possibilities. These cases are when the currents in M_1 and M_2 are different but neither is zero and when one of the input transistors has a current of I_{SS} and the other current is zero.

Where, i_1,i_2,i_3,i_4,I_{SS} are the currents through the M_1,M_2,M_3,M_4,M_5 transistors respectively.

We begin by first assuming that v_{G2} is equal to a dc voltage, V_{G2}, and that $V_{G1} > V_{G2}$ with $i_1 < I_{SS}$ and $i2 > 0$. In this case, as long as M_4 remains in saturation, $i_4 = i_3 = i_1$, which is greater than i_2. Consequently, v_{o1} increases because of the difference current flowing into C_I.

As v_{o1} continues to increase, M_4 will become active and $i_4 < i_3$. When the voltage across the source–drain of M_4 decreases to the point where $i_4 = i_2$, the output voltage of the first stage, v_{o1}, stabilizes. This value of voltage is

$$V_{DD}-V_{DS4}(SAT)<V_{01}<V_{DD}\ ,\quad V_{G1}>V_{G2}\ ,I_1<I_{SS} \quad (6)$$

Under the above conditions of equation(6), the value of $v_{SG6} < |V_{TP}|$ and M_6 will be off and the output voltage will be

$$V_{OUT} = V_{SS},\ V_{G1}>V_{G2},I_1<I_{SS} \text{ and } I_2>0 \quad (7)$$
$$\text{If } v_{G1} >> V_{G2}, \text{ then } I_1=I_{SS}$$

and i2 = 0 and v_{o1} will be at V_{DD} and v_{out} is still at V_{SS}. Next, assume that v_{G2} is still equal to V_{G2}, but now $v_{G1} < V_{G2}$ with $I_1 > 0$ and $I_2 < I_{SS}$. In this case, $i_4 = i_3 = i_1$ is less than i_2 and v_{o1} decreases. When $v_{o1} <= V_{G2} - V_{TN}$, then M_2 becomes active. As v_{o1} continues to decrease, $v_{DS2} < V_{DS2}(sat)$, the current through M_2 decreases until $i_1 = i_2 = I_{SS}/2$ at which point v_{o1} stabilizes. At this point,

$$V_{G2}-V_{GS2}<V_{01}<V_{G2}-V_{GS2}+V_{DS2}(sat) \quad (8)$$

Under the condition of equation (8), the output voltage, v_{out}, will be near V_{DD}. If $v_{G1} << V_{G2}$, the previous results are still valid until the source voltage of M1 or M2 causes M5 to leave the saturated region. When that happens, I_{SS} decreases and v_{o1} can approach V_{SS} and v_{out} will be determined. If the gate of M1 is equal to a dc voltage of V_{G1}. Assume that $v_{G1} = V_{G1}$ and $v_{G2} > V_{G1}$ with $i_2 < I_{SS}$ and $i_1 > 0$. As a result, $i_1 < i_2$ gives $i_4 < i_2$ as long as M4 is saturated. Therefore, v_{o1} decreases because of the difference current flowing out of C_I. As v_{o1} decreases, M2 will become active and i2 will decrease to the point

where $i_1 = i_2 = I_{SS}/2$.

Therefore, v_{o1} stabilizes and has a value given as

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$V_{G1} - V_{GS2}(I_{SS}/2) < v_{o1} < V_{G1} - V_{GS2}(I_{SS}/2) + V_{DS2}(sat)$,(9)

$V_{G2} > V_{G1}, i_1 > 0$ and $i_2 < I_{SS}$

Under the condition of equation (9), the output voltage, v_{out}, will be near V_{DD}. If $v_{G2} >> V_{G1}$, the previous results are still valid until the source voltage of M_1 or M_2 causes M_5 to leave the saturated region. If I_{SS} decreases and v_{o1} can approach V_{SS}. Next, assume that v_{G1} is still equal to V_{G1}, but now $v_{G2} < V_{G1}$ with $i_1 < I_{SS}$ and $i_2 > 0$. As a result, $i_1 > i_2$, which gives $i_4 > i_2$, causing v_{o1} to increase. As long as M_4 is saturated, $i_4 > i_2$. When M4 enters the active region, i_4 will decrease until $i_4 = i_2$ at which point v_{o1} stabilizes. The value of $v_{SG6} < |V_{TP}|$ and M6 will be off and the output voltage will be

$$V_{out} = V_{SS}, \quad (10)$$
$$V_{G2} < V_{G1},\ i_1 < I_{SS} \text{ and } i_2 > 0$$

If $v_{G2} << V_{G1}$, then $i_1 = I_{SS}$ and $i_2 = 0$ and v_{o1} will be at V_{DD} and v_{out} is still at V_{SS}.

In most applications, the two-stage, open-loop comparator is overdriven to the point where the propagation delay time is determined by the slewing performance of the comparator. The propagation delay time is found by evaluating the equation

$$i_i = C_i \frac{dvi}{dti} = C_i \frac{\Delta vi}{\Delta ti} \quad (11)$$

where C_i is the capacitance to ground at the output of the ith stage. The propagation delay time of the ith stage is found by solving for Δt_i from to get

$$t_i = \Delta t_i = c_i \frac{\Delta Vi}{Ii} \quad (12)$$

The propagation delay time is found by summing the delays of each stage. The term Δv_i in the above equation (12) is generally equal to half of the output swing of the ith stage. In some cases, the value of Δv_i is determined by the threshold or trip point of the next stage. The trip point of an amplifier is the value of input that causes the output to be midway between its limits. In the two-stage, open-loop comparator, and the second stage is generally a Class- A inverting amplifier similar to that shown in Fig-6.

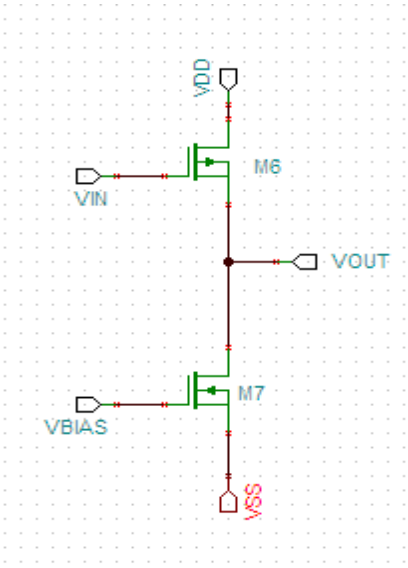

Fig -6.second stage of the two-stage open- loop comparator.

The trip point can be calculated by assuming both transistors are in saturation and equating the currents. The only unknown is the input voltage. Solving for this input voltage gives

$$V_{in} = V_{TRP} = V_{DD} - |VTP| - \sqrt{\frac{KN(\frac{W7}{L7})}{KP(\frac{W6}{L6})}}(V_{bias} - V_{SS} - V_{TN}) \quad (13)$$

We see that the trip point is really a range and not a specific value. However, if the slope of the inverting amplifier in the region where both transistors are saturated is steep enough, then the trip point can be considered to be a point.

Trip point of second stage is

$$V_{TRP2} = V_{DD} - V_{SG6} \quad (14)$$

The falling propagation delay of first stage is

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$$tf01 = CI\left(\frac{VSG6}{I5}\right) \qquad (15)$$

The rising propagation of second stage requires the knowledge ofC_{II} ,ΔV_{out},I_6

$$I_6=\frac{\beta 6}{2}(VSG6 - |VTP| \wedge 2) \quad (16)$$

The rising propagation delay for the output can be expressed as

$$tr, out = CII\,\frac{VDD}{(I6-I6(sat))} \qquad (17)$$

Consider the change of V_{G2}rom 2.5 TO -2.5V.

The propagation delay time for the first and second stages are calculated as

$$tr01 = CI\left(\frac{VTRP2-VG6}{I5}\right) \qquad (18)$$

$$tf, out = CII\left(\frac{VDD}{I6(SAT)}\right) \qquad (19)$$

The propagation delay time of the falling output is (t_{r01}+t_f), out. The average of rising and falling propagation delays time gives a propagation delay time for this two stage, open-loop comparator

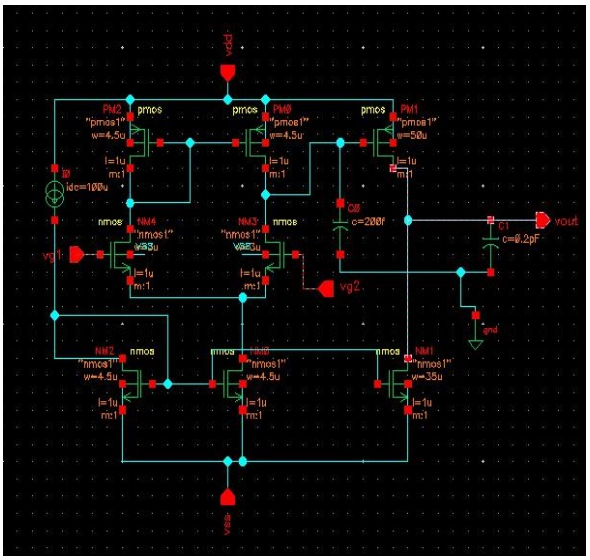

Fig-7 : schematic of two stage comparator with bias current 35 micro amperes

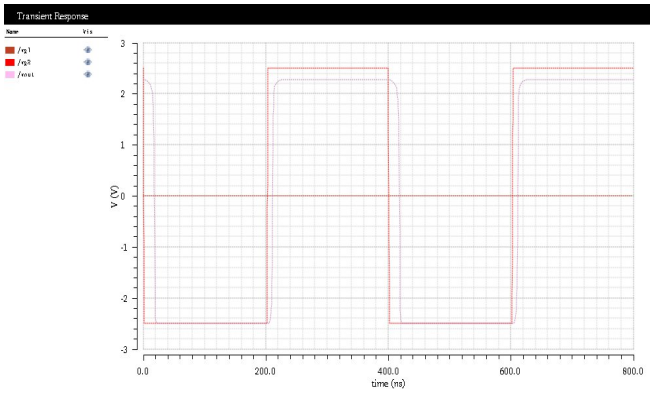

Fig-8:simulation results

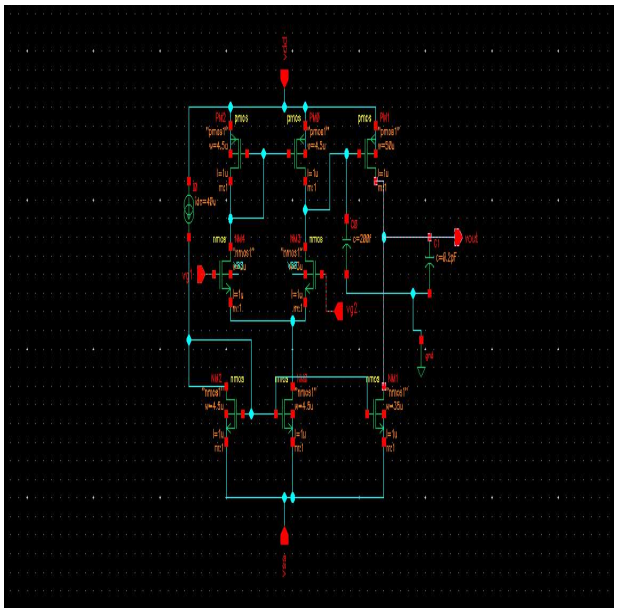

Fig-9:.schematic of two stage comparator with bias current 40 micro amperes

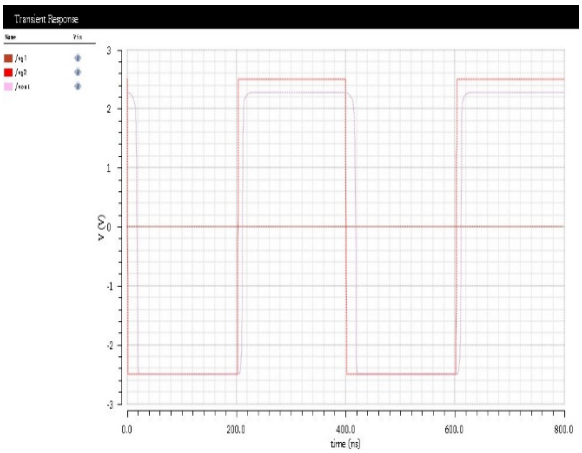

Fig-10:simulation results

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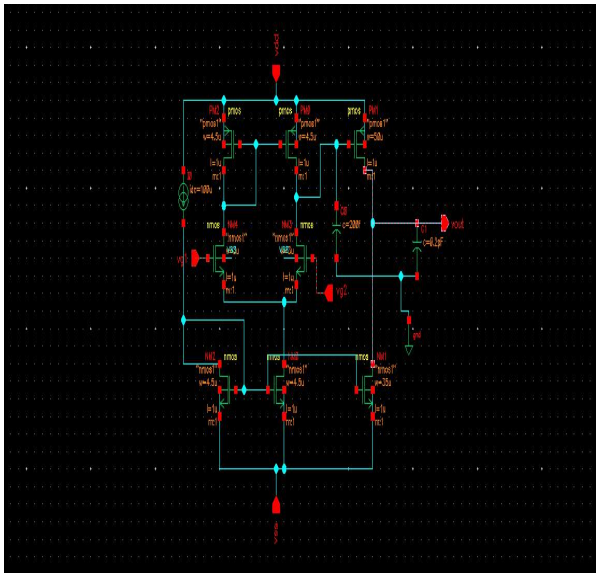

Fig -11:schematic of two stage comparator with bias current 100 micro amperes

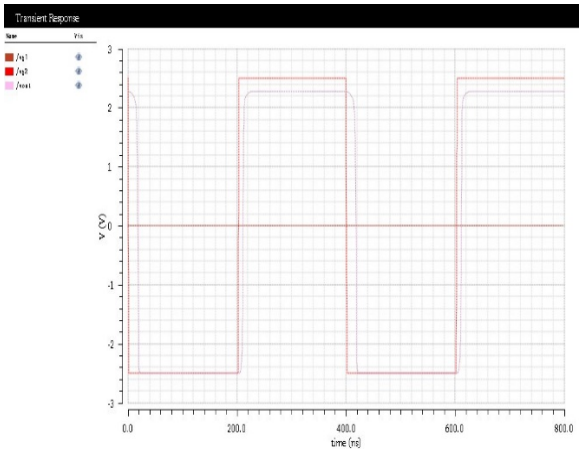

Fig-12:simulation results

Table 1:comparision of parameters

Bias current(micro Amps)	Delay(nano secs)
30	61.66
35	50.12
40	43.67
50	34.62
100	16.59

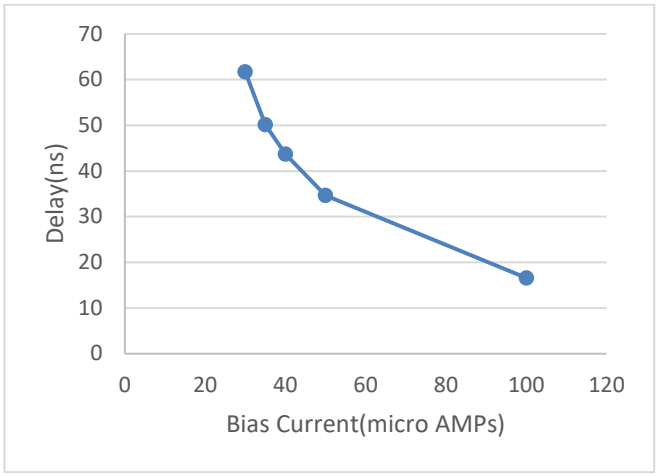

Fig -13:Graph between bias current and delay

CONCLUSION

In this paper two stage open loop high speed comparator is implemented and simulated ,simulation is carried outusing Cadence tools, with gpdk 180nm technology. The power dissipation and total propagation delay are calculated for comparator with supply voltage of 2.5v.High speed is achieved withincrease in bias current with a slight increase in dynamic power dissipation, further improvements are needed to co-optimize delay and reduce power dissipation.

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