

Network on Chip - A Study on RiCoBiT (Ring Connected Binary Tree)

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Abstract

The increased requirement of heterogeneous core was becoming an another issue because if one processor had high processing power then the other one had less power, for this reason the bandwidth, scalability and even the power efficiency was in high demand, to overcome on all these methods, Network on Chip came into picture. Thus using Network on Chip, we can transfer data in the form of packets. It basically follows layered structure of protocol stack. Network on Chip consists of Routers Processing elements and a Network interface. It uses a Network which is similar to Wide area network (WAN) but it does not use Wide Area Network. This paper will be the discussion on a hybrid architecture that is ring connected binary tree, so that a better topology with reduced latency and increased bandwidth can be used in NoC. The paper also discusses about the performance parameter and its methodology.

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1. Introduction

In everyday life, we are more towards more utilization of electronic innovation, this lead to appearance of framework on chip (SoC). SoC is commonly communicated as an IC which fundamentally joins all segment of a PC or hardware into a solitary chip. These SoC was utilized to create portable phones, tablets and so on. SoC made these gadgets look little in size with enormous Capacity and furthermore quicker than that of PCs. So Chad few short comings such as

- Productivity Gaps[8,9]- The difference of the item to be planned with the result we get can be instituted as productivity gap. In system on chip, capacity of the chip and its hardware and programming configuration were the significant issues.
- Global Synchrony[4,10]-Digital IC designs generally distributes clock tree and logic blocks function on the chip synchronized manner. Since, Technology scaling does not treat wire delay and gate delay equally; it becomes difficult for globally synchrony.
- Deep Sub Micron[6,12,13]-Prior, DSM had issues in regards with the impacts in interconnect deferral, clock

and force dispersion and placing and routing several number of gates. [6]

- Power and Thermal Management[11,14]-To run acircuit, higher frequency required with less power dissipation.

In defiance of circuit and process improvements, there was a huge utilization of power. Thus, diminishing devices to submicron dimensions, the voltage supply must be shortened to advert damaging electric fields.

Hindrance in system on chip directed network on chip to come into picture. Network on chip is used for sharing network, it has point to point link, computing module and a network switch. In NoC, communication is done by packet of bits. Routing of packets through several hop is done by switch. It also has efficient way of sharing wire and even it has parallelism. This paper is written in sections where the section starts from the introduction of study. Second Sections contains related work. Third Section contains Network on Chip architecture where a details about Ring Connected Binary Tree Architecture is discussed .Fourth Section tells us about performance analysis parameters followed by tools used, results and discussion.

2. Related works

The Theory of NoC came from "Route Packets, Not Wires: On-Chip Interconnection Networks" by Dally, William Towles, Brian. In this paper, they replaced ad-hoc global wiring with On-Chip Network[1]. "Zooming in on Network- on-Chip Architectures" by Israel Cidon, Idit Keidar is the paper with improved solution to problem such as network design, routing, and quality-of-service[2]. "Slim NoC: A Low Diameter On-Chip Network Topology for High Energy Efficiency and Scalability" by Maciej Besta, Syed Minhaj Hassan, Sudhakar Yalamanchili, RachataAusavarungnirun, Onur Mutlu, Torsten Hoefler is about improved Efficiency and Scalability. These are the base papers .We already have some existing topologies but each of them have some or the other issues regarding Switching and Routing Techniques.

Ring Connected Binary Tree gives the optimal solution for transferring data packets.

3. Network on Chip architecture

A. Topology

The topology specify the structure of the network graph, i.e., how network nodes (switches or routers) are connected physically. It defines the association(the routing possibility) Between the nodes, thus having a affect on the performances that a network performs. In RiCoBiT, the architecture is hybrid. It contains Ring and binary tree. Thus Ring1 contains 2node, Ring 2 contains 4 nodes and so on forming binary tree in rings.[16]

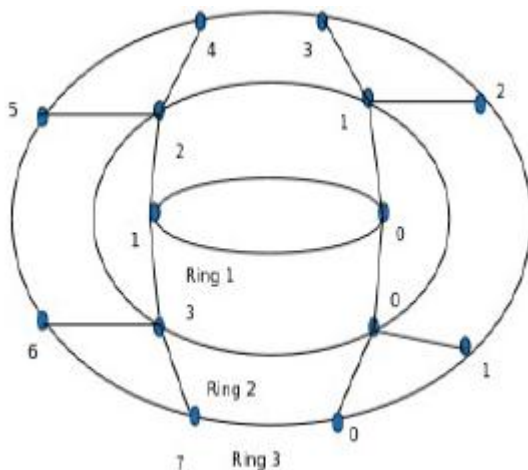


Figure 1: Ring Connected Binary Tree.

B. Switching

Switching can be determined as how the message traverses its route. Switching can be of two types

- Circuit Switching[18] In Circuit Switching, the path from source to destination is always being assigned before it starts transferring the data.
- Packet Switching In Packet Switching, messages are

disconnected via continuity of packet. A packet basically contains a header, payload and a tail.

The Header channels the sequencing and routing information. Transmission of data takes place in payload. Tail lies at the end of packet which consists of error checking code.

Further Packet Switching are of following type

- 1) Store and Forward[18]:Network node should relieve an entire packet before forwarding it to the next node below. Both buffer and link bandwidth are at packet level. The latency t for transmitting l flits. Flit (smallest unit for the link level flow control)is the minimum unit of information that can travel across the link.

$$t = (l/bw + r) * h$$

Where bw is the link bandwidth in flits per cycle; r is the routing delay per hop; hop can be expressed as connection from one switch to another. h , is the number of hops from the source node to the destination node.

- 2) Virtual Cut Through [18]: It allocate both link bandwidth and buffers in units of packets.

In virtual cut-through, a network node does not wait for the reception of an entire packet. It receives a portion of the packet, and then forwards it downstream if the buffer space in the next switch is available. The downstream node must have enough buffers to hold the entire packet. In case of blocking, the entire packet is shunt into the buffers allocated. By transmitting packets as soon as possible, virtual cut-through reduces the latency for transmitting flits to

$$t = l/bw + r * h$$

- 3) Wormhole Switching[18]: Packet are divided into flits. Likecut-through, wormhole switching delivers flits in a pipelined fashion. Due to the pipelined transmission, the latency t of transmitting l flits is the same as that for virtual cut-through. Wormhole Switching basically handles packet blocking. In this switching, buffers and band- width are designated to flits instead of packets.

Among the existing Switching Techniques, Ring Connected Binary Tree uses Wormhole Switching Technique. The packet contains source, where packet is created and destination, where packet has to be delivered. Both contain the Ring No. and Node No. The Node No. indicates the number of nodes present in each Ring. Nodes present in the ring forms the Binary tree thus first ring has two nodes, second contains four nodes and so on. The packet will occupy $\log_2 R + R$ [16] bits for source and destination field and a K bits data field where R is the maximum numbers of the rings in the configuration. So the total size of the packet is $2 * (\log_2 R + R) + K$ bits.[16]

Destination Address		Source Address		Data Bits
Ring No.	Node No.	Ring No.	Node No.	

Figure 2: Packet Format

```
struct packet
{
int source_address, dest_address;
int data;
int Ring_No;
int Node_No;
int start_timer;
int end_timer;
};
```

C. Routing Algorithm

Routing algorithm routes the minimum or shortest path from source to destination. The Algorithm that RiCoBiT uses is minimal Routing Algorithm and it does not adapt any existing algorithm. The algorithm is called as RiCoBiT routing algorithm. The RiCoBiT Algorithm is as follow shown below. [16]

Case 0: When destination node address is same as current node address
Then absorb the packet.

Calculate the node difference.

Case 1: When the destination node address and the current node address is in the same ring.

If the node difference is greater than three
Then go through the bottom interface.

If node difference is less than half
The number of nodes in the ring
Then go through left interface
Else go through right interface.

Case 2: When the destination node address is below than that of the current node address.
Go through bottom interface

Case 3: When the destination node address is above than that of the current node address
Calculate parent node
Calculate the node difference between current Node and parent node

If the node difference is greater than three
Then go through bottom interface

If node difference is less than half the
Number of nodes in the ring
Then go through left interface
Else go through right interface
If node difference is zero

Figure 3: RiCoBiT Algorithm

D. Flow Control

The flow control, let us know that how the packets get transferred from one node to another. Links and buffer becomes the shared resources. Generally flow control can be analyzed as process of sending and receiving packets for the correct delivery of packets.

```
class Interface
{
bool Req,Ack,Data,Cik,Choke;
char Receive_Register[50];
char Send_Register[50];
char Receive_Buffer[50];
char Send_Buffer[50];
bool Busy_Bit, Recieve_Bit;
bool Transfer_Bit;
void Routing_Algorithm
(struct packet,int);
void Control_Logic
(struct packet,int nnodes);
void Buffer_Operations();
};
```

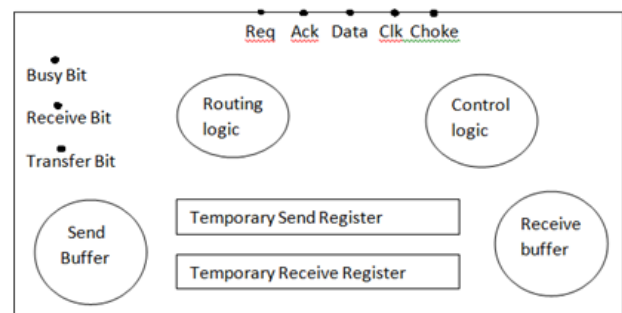


Figure 4: Flow Control

E. Quality of Service

Quality-of-Service (QoS) can be explained as how much the packets are able to perform their tasks i.e. the packet delivery is done on time or the packets moves towards the right destination path.

F. Interface

Interface can be defined as the working of the node. Each node contains the Interface that is divided into the following Segment ie Left Interface, Right Interface, Top Left Interface, Top Right Interface and the last one that is Bottom Interface as shown below in Fig.4.

```
class RiCoBiTNode {
InterfaceLeft_Interface;
InterfaceRight_Interface;
InterfaceTop_Left_Interface;
```

```
InterfaceTop_Right_Interface;
InterfaceBottom_Interface;
};
```

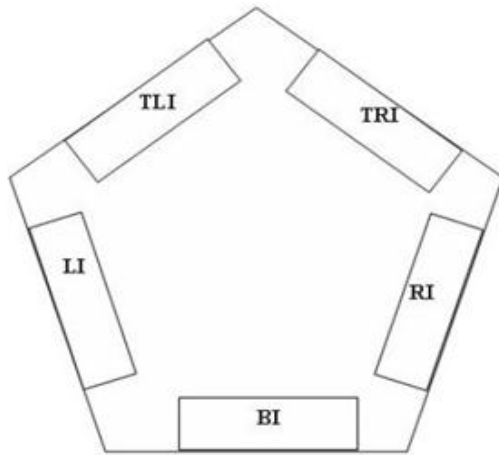


Figure 5: RiCoBiT node

4. NOC Performance Analysis

Network on Chip Performance Analysis has some of the performance parameters that are following

1) Bisection Bandwidth: Bisection Bandwidth divides the given topology into two networks. It improves the over- all performance of given network and is an important parameter. Bisection should be done in such a way that the bandwidth partitions should be less. Bisection bandwidth justifies the bottleneck bandwidth of the entire network. bisection bandwidth for RiCoBiT is $2L$ where, L is the number of Rings.

2) Max Hop Count: The maximum number of hops a node travels to obtain the optimal route path. In RiCoBiT, max hop count is $H_c(Max) = 2\log_2(N_r + 2) - 4$ where,

N_r = Number of nodes

3) Network Diameter: The longest of all determined short- est paths in a network can be considered as the network diameter. It is the shortest distance between the two most distant nodes in the network. Thus, the diameter is the longest of all the calculated path lengths[5] In RiCoBiT the Network Diameter is $2(h-1)$ where, $h = \log_2 N$ for even Rings and $h = \log_2 N + 1$ for odd number of Rings.

Node Degree: Degree of node can be calculated based on maximum number of adjacent node. Higher is the node degree, better will be communication between the node. For a regular network, if all nodes has same node degree. In RiCoBiT the node degree is

$$N_r = \sum_{k=L=1} 2^L$$

5. Tool Used

So as to perform RiCoBiT Topology, I have utilized C++ language in Code::Blocks. It is an open-source cross-stage IDE that underpins different compilers including GCC, Clang and Visual C++.Using C++, we create a seperate header file RiCoBiT.h, where we can declare our own function that we want to use for RiCoBiT in main program.

6. Results

Simulation was performed based on the RiCoBiT Routing logic, thus there were 3 cases

Case 1: destination node and source node are in same ring

Case2: destination node is below source node

Case3: destination node is above source node

Based on three cases discussed, following simulation results were obtained. The results contain row number, column number, source address, destination address, time taken by packet to transfer the data and hop count.

Case 1: destination node and source node are in same ring

Row	Col	SrcX	SrcY	DestX	DestY	Time	Hop
1	1	0	0	1	1	0.218798	1
1	2	0	0	2	2	0.325274	3
4	3	0	0	3	3	0.551096	7
3	4	0	0	4	4	0.9522	15
8	5	0	0	5	5	1.30441	31

Case2: destination node is below source node

Row	Col	SrcX	SrcY	DestX	DestY	Time	Hop
2	1	0	2	2	1	0.060375	3
4	2	1	2	2	1	0.066194	8
3	3	2	0	2	4	0.192982	7
8	4	4	3	2	3	0.031592	12
6	5	9	8	7	4	0.117243	18

Case3: destination node is above source node

Row	Col	SrcX	SrcY	DestX	DestY	Time	Hop
1	1	0	0	3	5	0.49384	4
3	2	2	0	5	7	0.076874	4
2	3	4	7	0	1	0.811899	5
5	4	8	6	1	1	0.446928	9
9	5	9	7	3	8	1.09764	14

7. Conclusion

The above simulation result could let us know about the hop count and time taken by packets to travel from one node to another in given condition. The simulator helped me in understanding the working of the RiCoBiT node. We are able to conclude that the study and analysis of existing topologies shows that performance parameter such as bisection bandwidth, hop count, diameter and throughput for RiCoBiT is better than those of Mesh, Torus, Ring, Binary Tree. Also the simulated results concluded the above stated statement.

Future Enhancement of this project can be accomplished; ERiCoBiT(Enhanced Ring Connected Binary Tree) can be the advancement of RiCoBiT in which each node in the RiCoBiT topology will have other sub tree which will help to increase the performance with lower routing complexity. This Architecture will form up the quad tree structure and can be worked accordingly.

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