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Failure Region Estimation of Linear Voltage Regulator Using Circuit Model-Based Virtual Sensing

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Abstract

Disturbance to the linear voltage regulator (LVR) output caused by the abrupt change of either output current or input voltage can be compensated using an output capacitor. The compensation can be performed by utilising the capacitor's internal parasitic resistance called the equivalent series resistance (ESR). The values of ESR vary due to aging and temperature change factors, so despite the benefits of ESR, it creates a failure region in LVR for a range of ESR and output current. Characterisation involving manual data acquisition and analysis is required to estimate accurately the failure region, but the process is time consuming and costly. In this study, the application of circuit model-based virtual sensing (CMBVS) to improve the efficiency of LVR failure region estimation (FRE) was investigated. CMBVS was developed to obtain the LVR circuit model through circuit analysis and linear regression before estimating the unmeasurable circuit parameters using simultaneous equation solution. The estimated failure region from CMBVS was then compared with the failure region benchmark, which was obtained from the manual FRE method. Findings showed that the failure region estimated using CMBVS produced MAE, MSE, RMSE and regression coefficient, R^2, of 1.16×10^{-6}, 1.16×10^{-12}, 1.22×10^{-6} and 0.9999, respectively. This investigation revealed that CMBVS is an efficient and effective LVR FRE method.

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1. Introduction

Linear voltage regulator (LVR) stability has become an important issue in power management system design for electronic products. LVR is widely used to convert unstable and noisy input voltage into a stable and noise-free output voltage that supplies to various analogue and digital load circuits [1-2].

In many cases, disturbances may occur to the LVR output due to the abrupt change of either output current or input voltage that causes the LVR

output voltage to oscillate and become unstable. Therefore, in most LVR designs, an output capacitor with specific internal parasitic resistive element called equivalent series resistance (ESR) is connected to the LVR output terminal to compensate for the disturbances. The optimum ESR range to ensure LVR output stability is typically shown in a unique graph in LVR manufacturer datasheet called the ESR tunnel graph [3-5], as depicted in Figure 1. This ESR range exists because ESR values vary due to aging and temperature change factors.

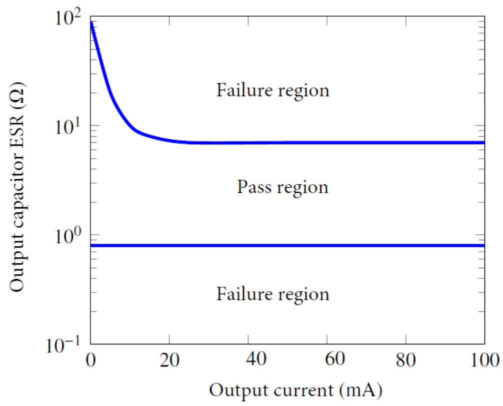

Figure 1: Example of ESR tunnel graph

Figure 1 shows three separated regions, with a pass region located between lower and upper failure regions. If an electronic system, such as LVR, operates in the failure region, then the system may fail [6-7]. The optimum ESR range is defined as the range starting from the minimum until maximum ESR of the pass region for each load current. However, the determination of this optimum ESR range has become a challenge to LVR manufacturers. Nowadays, the optimum ESR range is estimated manually in manufacturing plants because the actual model for each LVR unit is different due to manufacturing variation factor. The manual estimation involves manual data acquisition and analysis for each operating point in the ESR tunnel graph. Each operating point consists of a unique value of ESR and output current. A high accuracy of boundary between pass and failure regions can be obtained by acquiring data for several operating points manually. However, this process is time consuming and costly. In addition, an individual with high expertise must analyse the acquired data to determine the pass or fail status for each operating point. Given these drawbacks, an efficient and effective method is needed to improve failure region estimation (FRE).

Reducing the number of operating points that require manual data acquisition is one way to improve efficiency of FRE. However, the effectiveness in estimating the failure regions must also be considered because data for the remaining operating points are unobtained. Therefore, virtual sensing (VS) was utilised in this study to estimate the failure regions by determining the failure status for the remaining operating points. VS acts as sensor to obtain the unmeasurable or difficult-to-measure physical parameters in a system [8-10]. VS can be divided into two main categories, namely, (a) data-driven and (b) model-based approaches. Data-driven VS using multilayer perceptron neural network has been used to estimate the LVR failure region without any LVR circuit modelling [11]. Model-based VS has recently obtained the LVR model for a certain number of operating points using a system identification approach before estimating the model transfer function coefficients by utilisingneural network [12]. However, the obtained LVR model was the black-box one, which only based on the acquired input and output signals, disregarding the existing measurable components in the LVR circuit. Other studies have been also conducted to model electronic circuits for failure analysis [13-14].

The present paper presents a new model-based VS called circuit model-based VS (CMBVS) that considers the measurable component values in the VR circuit. CMBVS involves detailed circuit analysis and linear regression and then uses a simultaneous equation solution approach to obtain the unmeasurable LVR circuit parameters. The remaining of this paper is structured as follows. Methodology section describes the detail methodology of the work including the development of failure region benchmark and CMBVS algorithm. Then, results are reported in the subsequent section and finally the last section concludes this work.

2. Methodology

In this study, CMBVS, which can be categorised as a model-based VS approach, was used to estimate the LVR failure region. CMBVS manipulated the measurable components in an LVR circuit to reduce the number of parameters that must be estimated for increasing accuracy. To achieve this goal, an LVR circuit was fully constructed using discrete components, as depicted in Figure 2. The LVR circuit output is an adjustable output voltage controlled by feedback resistors, $R_1$and R_2, with a PMOS transistor used as the pass element to manage the output current. ESR is an internal parasitic element that is difficult to be directly measured. Therefore, an adjustable resistor, R_{ESR}, was connected in series with the output capacitor to simulate the variation of ESR values. $R_L$acted as the load, whilst R_s was connected to a signal generator to create a disturbance signal in the form of a squarewave signal. This disturbance signal can abruptly increase or decrease the output current with small magnitude. The small signal is directly related to the LVR output impedance that affects the LVR stability. Hence, the LVR circuit in Figure 2 was transformed into the small signal analysis circuit to perform analysis, as displayed in Figure 3.

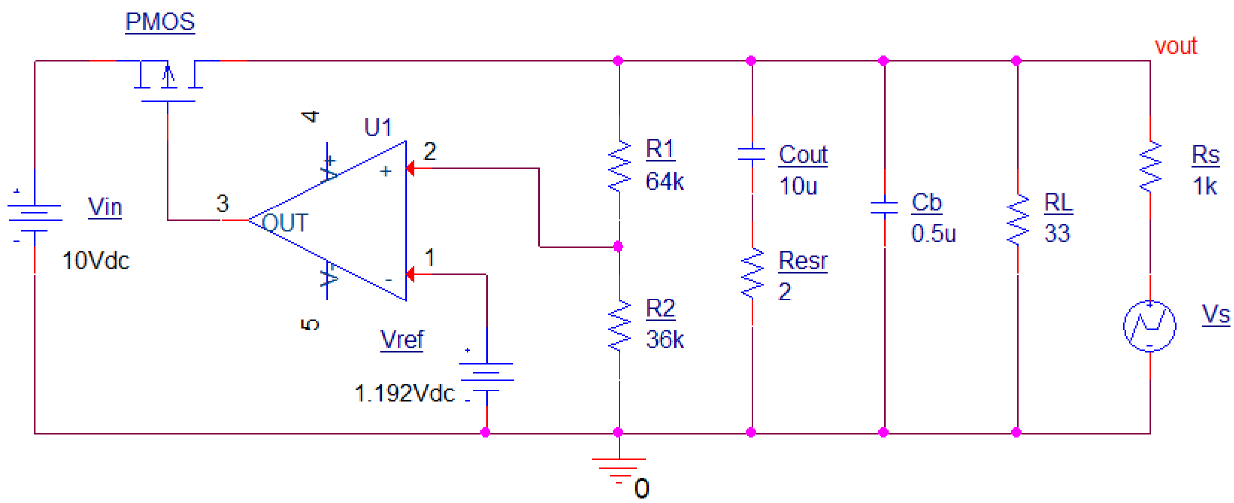

Figure 2: LVR circuit

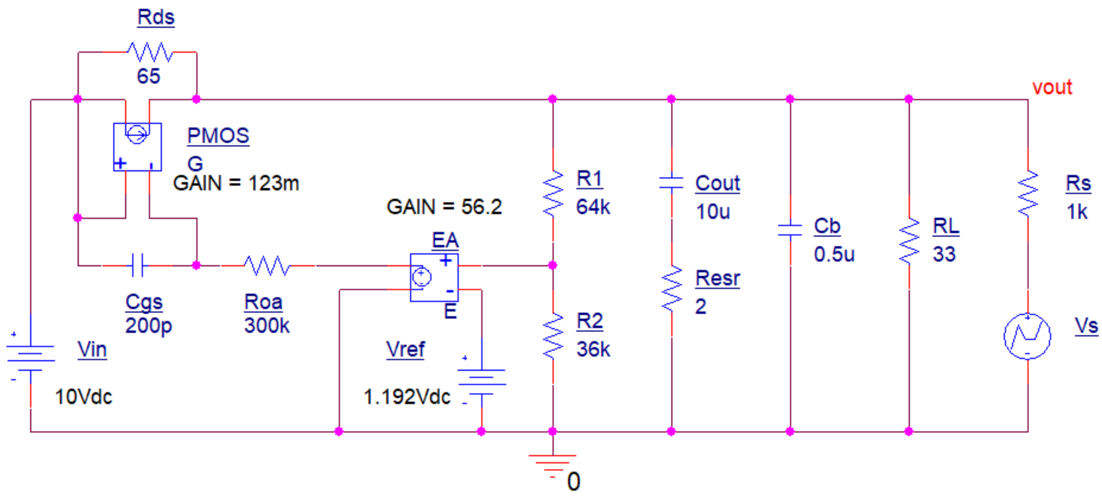

Figure 3: LVR circuit for small signal analysis

2.1 Failure Region Benchmark

All data in this work were acquired on the basis of the simulation of the circuit shown in Figure 3 using OrCAD Capture CIS Lite software from Cadence Design Systems. The acquired data, which were sampled at sampling time T_s of 1 µs, were collected in a dataset using MATLAB software from MathWorks. This study also developed the CMBVS algorithm using MATLAB with neural network and system identification toolboxes. Before developing the CMBVS algorithm, a benchmark dataset obtained from manual FRE was created. The dataset consists of various information, such as output current value before applying the disturbance, ESR of output capacitor and ESR lower and upper limit that resides on the boundary between failure and pass regions in the ESR tunnel graph. This manual process involved four subprocesses, namely, data acquisition, failure analysis, ESR tunnel graph plotting and failure region determination, as depicted in the flowchart in Figure 4. The four subprocesses were conducted for each operating point in the ESR tunnel graph until all operating points were completely analysed.

The data acquisition process acquired output current and voltage signals from the LVR circuit through circuit simulation. The output voltage undershoot was then measured and analysed either within the undershoot specification or not. If the measured undershoot was within the specification, then the corresponding operating point passed and was marked with a circle symbol on the ESR tunnel graph. If not, then the operating point failed and was marked with a cross symbol on the graph. Finally, the pass and failure region boundaries were determined from the plotted ESR tunnel graph and became the ESR lower and upper limit benchmark for the subsequent CMBVS algorithm.

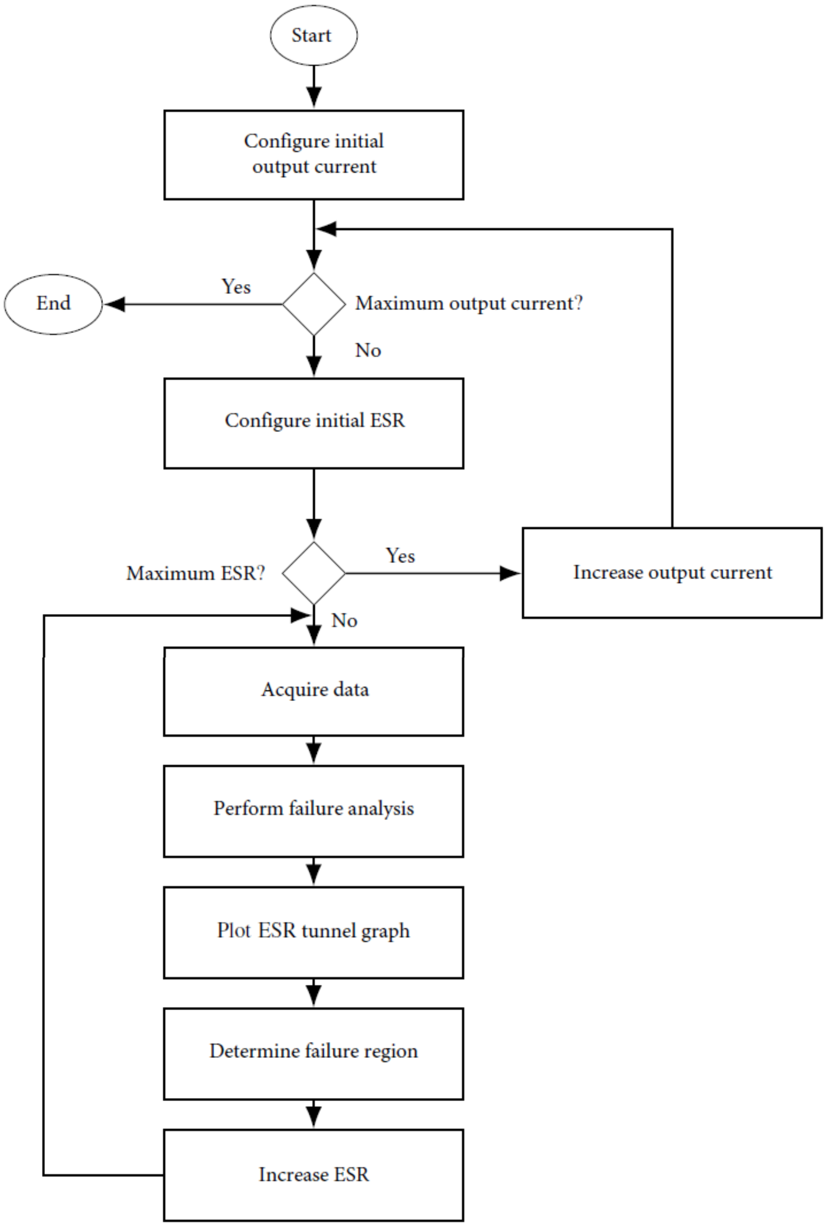

Figure 4: Manual FRE flowchart

2.2 Circuit Model-based Virtual Sensing

Figure 5 shows the CMBVS block diagram, which consists of four main processes, namely, data acquisition, circuit modelling, physical parameter estimation and failure region determination. Data acquisition and failure region determination are similar to the manual FRE in the previous section. Circuit modelling was conducted through (a) grey-box and (b) black-box modelling. The physical parameter estimation aimed to estimate the unmeasurable parameters in the LVR circuit on the basis of the information from the modelling process through simultaneous equation solution.

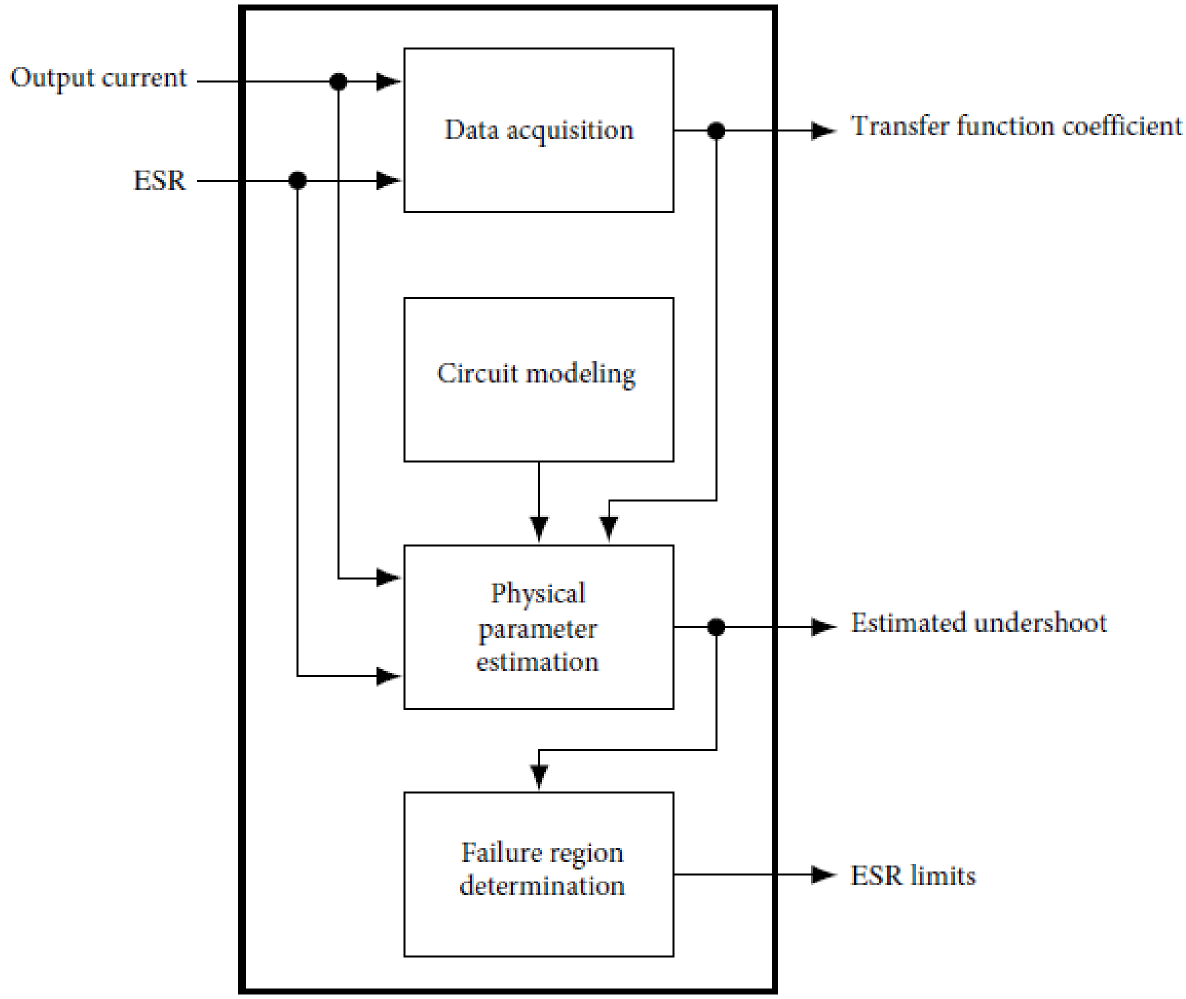

Figure 5: CMBVS block diagram

Grey-box modelling was performed via small signal circuit analysis in CMBVS algorithm. This process utilised the physical parameters that can be measured in the LVR circuit, as shown in Figure 6. In this case, the estimated model was voltage gain model. The measurable parameters were R_1, R_2, C_{out} and r_{ds}, which were substituted with the actual component values of 64 kΩ, 36 kΩ, 10 µF and 65 Ω, respectively. After analysing the circuit in Figure 6, voltage gain transfer function A_v in discrete-time domain can be derived as follows:

$$A_v(z) = \frac{g_m r_{ds} + 1}{1 + \frac{2}{T_s}\left(\frac{1-z^{-1}}{1+z^{-1}}\right) C_{out}\, r_{ds} + \frac{r_{ds}}{R_1 + R_2} + \frac{g_m r_{ds} G_{ea} R_2}{(R_1+R_2)\left(1 + \frac{2}{T_s}\left(\frac{1-z^{-1}}{1+z^{-1}}\right) R_{ea} C_{par}\right)}} \quad \textbf{(1)}$$

which can be generally represented as,

$$A_v(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \quad \textbf{(2)}$$

Each coefficient in Eq. (2) can be defined by expanding Eq. (1) into,

$$b_0 = N_1 C_{par} R_{ea} + N_2 C_{Par} R_{ea} g_m + N_3 g_m + N_4 \quad \textbf{(3)}$$

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$$b_1 = N_5 g_m + N_6 \quad \textbf{(4)}$$

$$b_2 = N_7 C_{par} R_{ea} + N_8 C_{Par} R_{ea} g_m + N_9 g_m + N_{10} \quad \textbf{(5)}$$

$$a_0 = D_1 C_{par} R_{ea} + D_2 G_{ea} g_m + D_3 \quad \textbf{(6)}$$

$$a_1 = D_4 C_{par} R_{ea} + D_5 G_{ea} g_m + D_6 \quad \textbf{(7)}$$

$$a_2 = D_7 C_{par} R_{ea} + D_8 G_{ea} g_m + D_9 \quad \textbf{(8)}$$

where constants N_1 to N_{10} and D_1 to D_9 can be calculated by substituting the measurable parameters with the actual component values. In the end, only four unmeasurable parameters, namely, g_m, $C_{par} R_{ea}$, $C_{par} R_{ea} g_m$ and $G_{ea} g_m$, remained in A_v that need to be estimated.

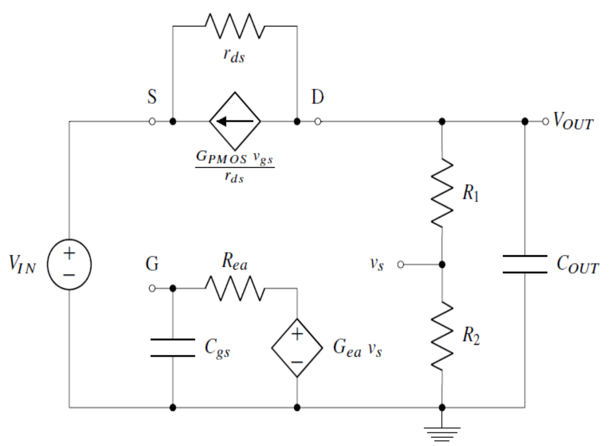

Figure 6: Voltage gain circuit for small signal analysis

In the black-box modelling, linear regression (LR) technique was used to estimate all six transfer function coefficients in Eq. (2) on the basis of the acquired input and output voltage signals from the LVR circuit shown in Figure 6. In this research, the input voltage signal that acts as the excitation signal was in the form of sinusoidal signal. Sinusoidal signal was selected because sinewave signal can simultaneously excite two frequency components. Six coefficients are in Eq. (2), indicating that six frequency components exist. Thus, at least three sinewave signals with different frequencies were required to excite the LVR circuit. However, the combination of four sinewave signals with different frequencies, namely, 5, 10, 15 and 20 kHz, were selected in this study to increase the coefficient estimation accuracy. The frequency selection was based on the peak time of the LVR circuit step response. Afterwards, the LVR circuit was simulated to obtain the output voltage signal. Then, LR was used to estimate the LVR circuit model in terms of voltage gain transfer function coefficients a_0, a_1, a_2, b_0, b_1 and b_2, without any consideration on the actual measurable components in the circuit. Subsequently, coefficients a_1, a_2, b_0, b_1 and b_2 are divided with a_0 for improving the LR estimation accuracy, generating coefficients $a_{1_{LR}}$, $a_{2_{LR}}$, $b_{0_{LR}}$, $b_{1_{LR}}$ and $b_{2_{LR}}$.

2.3 Physical Parameter Estimation

After estimating the parameter of grey-box and black-box models, all unmeasurable physical parameters, namely, g_m, $C_{par} R_{ea}$, $C_{par} R_{ea} g_m$ and $G_{ea} g_m$, in the LVR circuit were estimated using simultaneous equation solution. Individually estimating each parameter is unnecessary because the estimated unmeasurable parameters were utilised to obtain the LVR circuit time response. Firstly, each transfer function coefficients from the circuit analysis and LR models were individually compared in the simultaneous equation solution. Before this step, coefficients a_1, a_2, b_0, b_1 and b_2 in Eq. (3) from the circuit analysis model

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were divided with a_0 in Eq. (3) to produce new five transfer coefficients to be estimated, namely,a_{1CAM}, a_{2CAM}, b_{0CAM}, b_{1CAM} and b_{2CAM}. Each coefficient from circuit analysis and LR models were then equalised with one another and subsequently solved using simultaneous equation to obtain the unmeasurable physical parameters of interest.

2.4 Failure Region Determination

The LVR failure region was determined after obtaining the unmeasurable parameters. Firstly, the measurable and estimated unmeasurable parameters were substituted into the output impedance model, which was derived on the basis of Figure 2. The output impedance model was then simulated through a load transient test in OrCAD to acquire the LVR output voltage signal in the time domain. Afterwards, the undershoot of acquired output voltage was measured and analysed to determine the failure status for each operating point. The ESR tunnel graph was subsequently plotted for all operating points on the basis of this failure status. Finally, the ESR lower and upper limits were extracted from the plotted ESR tunnel graph and compared with the benchmark from the manual FRE to measure the effectiveness of CMBVS algorithm. In this case, four performance metrics, namely, mean absolute error (MAE), mean square error (MSE), root mean square error ($RMSE$) and regression coefficient (R^2), were computed as follows:

$$MAE = \frac{1}{N}\sum_{i=1}^{n}\left|y(i) - y_p(i)\right|$$

(9)

$$MSE = \frac{1}{N}\sum_{i=1}^{n}\left(y(i) - y_p(i)\right)^2$$

(10)

$$RMSE = \sqrt{\frac{1}{N}\sum_{i=1}^{n}\left(y(i) - y_p(i)\right)^2}$$

(11)

$$R^2 = \frac{\sum_{i=1}^{n}(y(i) - \bar{y}(i))(y_p(i) - \overline{y_p}(i))}{\sqrt{\sum_{i=1}^{n}(y(i) - \bar{y}(i))^2 \sum_{i=1}^{n}\left(y_p(i) - \overline{y_p}(i)\right)^2}}$$

(12)

Where y is the ESR limit benchmark, y_p is the ESR limit extracted from CMBVS algorithm, n is the number of ESR limit, and i is the output current index. CMBVS algorithm exhibits good performance if MAE, MSE and $RMSE$ values are minimum, and R^2 value is towards unity. To evaluate the efficiency of CMBVS algorithm, the duration for estimating the LVR failure region using CMBVS algorithm was also recorded and compared with duration for completing the manual FRE. The following performance metric was used to measure efficiency:

$$Efficiency = \left(1 - \frac{t_2(i)}{t_1(i)}\right) \times 100\%$$

(13)

where t_1 and t_2 are the duration for FRE of the manual method and CMBVS algorithm, respectively.

3. Results and Discussion

As previously mentioned, this study aimed to develop an effective and efficient LVR FRE method through CMBVS algorithm. The ESR limit benchmark was developed using manual estimation. Figure 7 shows the ESR tunnel

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graph obtained using the manual estimation method. Subsequently, the ESR lower and upper limits were extracted from the ESR tunnel graph, as depicted in Figure 8. Three separated regions were illustrated in Figures 7 and 8. The two failure regions at the bottom and top of the graph enclosed a pass region in the middle of the ESR range. Therefore, two ESR limits, namely, lower and upper, exist as the benchmark for CMBVS algorithm.

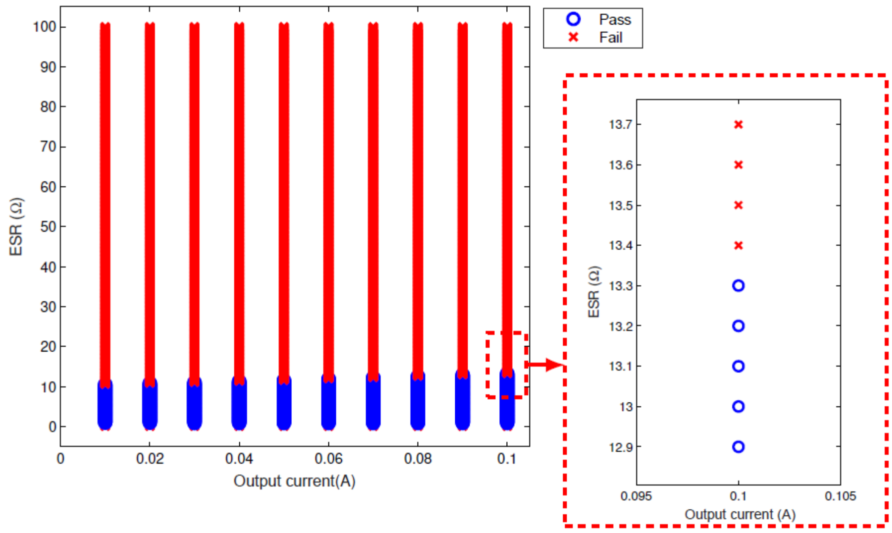

Figure 7: ESR tunnel graph of manual FRE

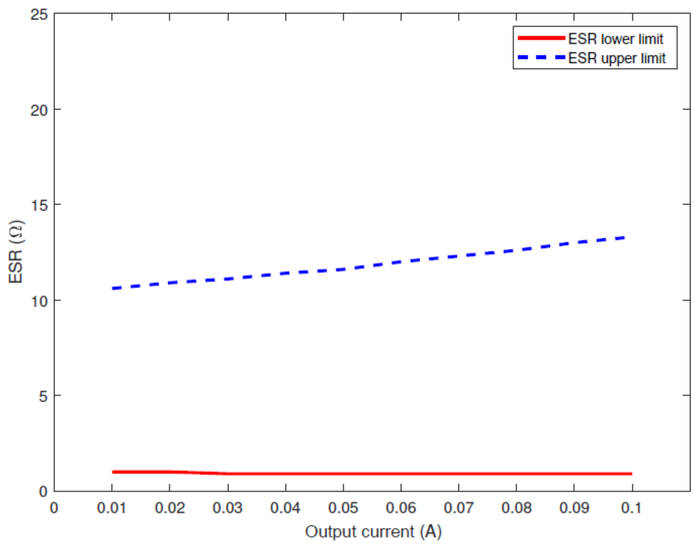

Figure 8: ESR lower and upper limit of manual FRE as benchmark

Figure 9 illustrates the finding of the ESR tunnel graph obtained using CMBVS algorithm. The comparison result between Figures 7 and 9 shows that the failure regions are similar. The ESR lower and upper limits were extracted on the basis of the ESR tunnel graph in Figure 9. The effectivenessof the FRE method through CMBVS algorithm was evaluated using the performance metrics in Eq. (4). In this case, MAE, MSE, $RMSE$ and R^2 are 1.16×10^{-6}, 1.16×10^{-12}, 1.22×10^{-6} and 0.9999, respectively, indicating that CMBVS has good

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performance. These performance metrics were computed in terms of the output voltage undershoot, which was measured on the basis of the time response of LVR circuit simulation using the estimated unmeasurable parameters. Two performance metrics, MAE and MSE, in evaluating the unmeasurable parameter estimation in CMBVS algorithm were also analysed. The outcomes are listed in Table 1. Three examples of unmeasurable parameters were investigated, and the overall performance is satisfied with MAE and MSE having small values.

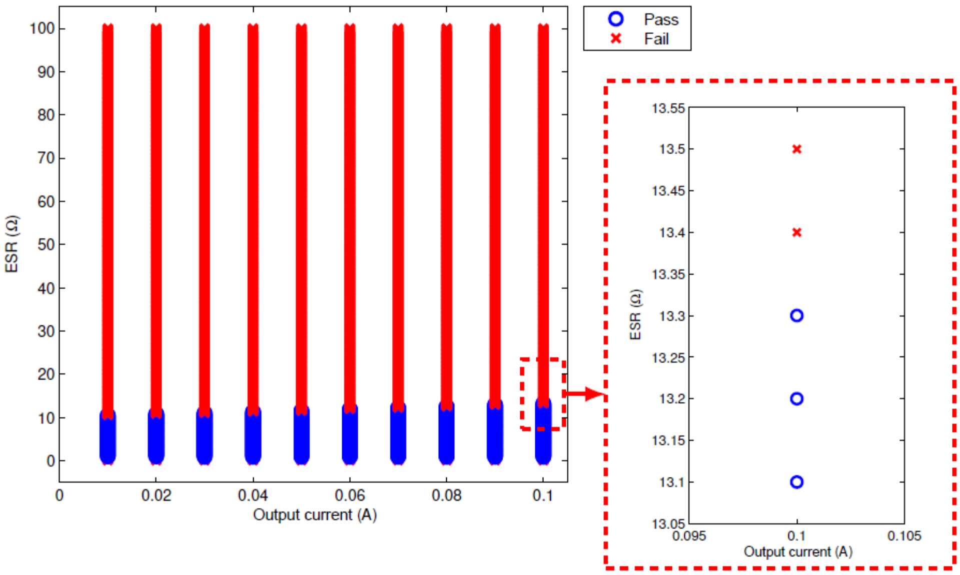

Figure 9: ESR tunnel graph from CMBVS algorithm

Table 1: Performance metrics for three examples of unmeasurable parameter estimation in CMBVSalgorithm

Set	Physical parameter			Performance metric	
	Parameter	**Expected**	**Estimated**	**MAE**	**MSE**
A	g_m	123.00×10^{-3}	101.70×10^{-3}	21.40×10^{-3}	4.5608×10^{-4}
	$C_{oa}R_{oa}$	6.0000×10^{-5}	5.9999×10^{-5}	1.0239×10^{-9}	1.0438×10^{-18}
	$C_{oa}R_{oa}g_m$	7.3800×10^{-6}	6.0985×10^{-6}	1.2815×10^{-6}	1.6421×10^{-12}
	$g_{ea}g_m$	6.9126	6.9132	6.0439×10^{-4}	3.6529×10^{-4}
B	g_m	123.61×10^{-3}	100.18×10^{-3}	23.40×10^{-3}	5.4925×10^{-4}
	$C_{oa}R_{oa}$	6.0601×10^{-5}	6.0600×10^{-5}	1.0546×10^{-9}	1.1121×10^{-18}
	$C_{oa}R_{oa}g_m$	7.4910×10^{-6}	6.0709×10^{-6}	1.4204×10^{-6}	2.0174×10^{-12}
	$g_{ea}g_m$	6.9819	6.9822	3.0192×10^{-4}	9.1153×10^{-8}
C	g_m	122.38×10^{-3}	109.08×10^{-3}	13.30×10^{-3}	1.7710×10^{-4}
	$C_{oa}R_{oa}$	5.9402×10^{-5}	5.9400×10^{-5}	1.7174×10^{-9}	2.9496×10^{-18}
	$C_{oa}R_{oa}g_m$	7.2699×10^{-6}	6.4792×10^{-6}	7.9069×10^{-7}	6.2519×10^{-13}
	$g_{ea}g_m$	6.8436	6.8439	2.5003×10^{-4}	6.2517×10^{-8}

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CMBVS algorithm is also an efficient FRE method. This algorithm can reduce the estimation time up to 80.24%. As shown in Figure 7, data had to be manually acquired for all 10,000 operating points in the manual estimation method, which took approximately 13,608 s. By contrast, FRE using CMBVS algorithm only needed to manually acquire data for an operating point to estimate the unmeasurable parameters in the LVR circuit. For the remaining operating points, the LVR circuit time response could be generated through circuit simulation using the estimated unmeasurable parameters. Therefore, the estimation time in CMBVS algorithm was significantly reduced.

4. Conclusion

The developed algorithm in this study improves LVR FRE in terms of effectiveness and efficiency. The outcomes demonstrate that CMBVS algorithm can effectively generate an ESR tunnel graph similar to the benchmark from manual estimation with all performance metrics showing good performance. In addition, CMBVS algorithm is an efficient method to estimate the failure region by greatly reducing the number of data that need to be manually acquired, thus shortening the total estimation time. As an effective and efficient method to estimate the LVR failure region, CMBVS algorithm can eventually determine the ESR stable range of output capacitor ESR in the LVR circuit.

Acknowledgments

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References

[1] G.A. Rincon-Mora, *Analog IC Design with Low-Dropout Regulators*. United States of America: McGraw-Hill, 2014, pp. 2-6.

[2] C. Basso, *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide,*. United States of America: Artech House, 2012, pp. 519-527.

[3] K.H. Chen, *Power Management Techniques for Integrated Circuit Design*. Singapore: John Wiley & Sons, 2015, pp. 28-29.

[4] K. Subasinghage, K. Gunawardane, N. Kularatna and T.T. Lie, “Selection of the stable range of the equivalent series resistance (ESR) of the output capacitor for a SCALDO regulator,” *IEEE 27th International Symposium on Industrial Electronics, Queensland, Australia*, 2018, pp. 1359-1364.

[5] B.S. Lee, “Understanding the stable range of equivalent series resistance of an LDO regulator”,*Analog Applications Journal*, vol.1, pp. 14-17, 1999.

[6] M. Dobler, M. Harrant, M. Rafaila, G. Pelz, W. Rosenstiel and M. Bogdan, “Bordersearch: An adaptive identification of failure regions,” *Design, Automation & Test in Europe Conference & Exhibition, Grenoble, France*,2015, pp. 1036-1041.

[7] R.D. Amariutei, L. Goras, M. Dobler, M. Rafaila, A. Buzo and G. Pelz, “On the stability domain of a DC-DC buck converter with software control loop,” *19th International Conference on System Theory, Control and Computing, CheileGradistei, Romania*, 2015, pp. 811-816.

[8] S.B. Sun, Y.Y. He, S.D. Zhou and Z.J. Yue, “A data-driven response virtual sensor technique with partial vibration measurements using convolutional neural network”, *Sensors*,vol. 17, no. 12, pp. 2888-2910, 2017.

[9] D. Pathak and V.P Halale, “An introductory approach to virtual sensors and its modelling techniques”, *International Journal of Scientific & Engineering Research*,vol. 7, no. 3, pp. 461-464, 2017.

[10] F.A.A. Souza, R. Araujo and J. Mendes, "Review of soft sensor methods for regression applications", *Chemometrics and Intelligent Laboratory Systems*,vol. 152, pp. 69-79, 2016.

[11] M.H.M. Zaman, M.M. Mustafa, M.A. Hannan and A. Hussain, "Neural network based prediction of stable equivalent series resistance in voltage regulator characterization", *Bulletin of Electrical Engineering and Informatics*,vol. 7, no. 1, pp. 134-142, 2018.

[12] M.H.M. Zaman, M.M. Mustafa and A. Hussain, "Critical equivalent series resistance estimation for voltage regulator stability using hybrid system identification and neural network", *International Journal on Advanced Science, Engineering and Information Technology*,vol. 7, no. 4, pp. 1381-1388, 2017.

[13] D. Binu and B.S. Kariyappa, "A Survey on fault diagnosis of analog circuits: Taxonomy and state of the art", *International Journal of Electronics and Communications*,vol. 73, pp. 68-83, 2017.

[14] S. Sindia, V.D. Agrawal and V. Singh, "Non-linear analog circuit test and diagnosis under process variation using V-Transform coefficients," *IEEE VLSI Test Symposium, California, United States of America*,2011, pp. 64-69.