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Design of CMOS Truncated Multiplier with 10T GDI Full Adder

[1]P.Radhakrishnan, [2]G.Themozhi

[1]Research scholar, Dept of ECE, Tagore Engineering College
[2]Professor, Dept of EEE, AMET University
[1]krish75radha@gmail.com, gthemozhivijayakumar@gmail.com

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Abstract

In recent technology of any applications, adder is a more priority to do a function and task of arithmetic operation. Based upon the improvement of the adder design, logic size is reduced year by year. Here the proposed discuss about design of a multiplier using single bit full adder. In this multiplier design, adder is a main priority to reduce the arithmetic logic size and increases speed of multiplier. The truncated multiplier is chosen, because, the truncated multiplier have a capability to reduce internal and external architecture size in every design. Regarding this, truncated multiplier have three operations such as rounding, deleting, truncating. The MSB bits of the partial product is truncated and the output of n bit x n bit multiplication will provide only n bit level instead of 2n bits. This proposed work is designed in CMOS Logic gate with 10-T transistor level of full adders with 45nm technology and finally proved in terms of area and power.

Keywords: *GDI(Gate Diffusion Input), Truncated Multiplier, Area, Power*

1. Introduction

The need for the usage of battery based portable electronic Devices is increasing in fast manner. The power consumption plays huge role in VLSI technology. Batteries are needed for driving small devices. The major concern in designing tablets, Laptop, mobile phones and other devices is speed and power consumption. The designed device consumes more power then the heat produced will be more which in turn reduces the battery life and performances. The DSP Process and microcontrollers are mainly used in the signal processing applications like video and image processing. The Various arithmetic and logical circuits are needed in the signal processing application.

The main aim of this work is to present a relative analysis of truncated multiplier and also to reduce area and ,power consumption of proposed multiplier when compared with conventional multiplier. The 8bit×8bit multiplier is designed using Tanner EDA tool and simulation results were compared. This paper is structured as follows. In section II, the literature survey is briefly discussed. Section III presents the proposed work of truncated multiplier. Section IV states about the simulation results and discuss about truncated multiplier and section V states about the conclusion.

2. Literature Survey

The full adders are used as the base element to design multipliers. The truncated multipliers are realized using various types of full adders. The various techniques used for truncated multiplier are discussed below.

The implementation of multiple constant multiplication (MCM) method in the high speed filter gives significant reduction in the power consumption. The single bit full added is designed using 45nm CMOS technology. The full adder was constructed using ten Transistors (10-T). The 10T full adder design consumes significantly low power (~0.001 mW) and fabrication area (~276μm2) than other full adder designs[3]. The 10T Gated Diffusion Index(GDI) full adder consumes 98% less power than conventional (28-T) method and consumes 65% less power than 16-T full adder implementation. The above results indicates rounded multipliers occupies less silicon area than the standard

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multipliers. The least significant bits of full width products are discarded in rounded multiplication [7]. The multiplier design is generally considered as a good design were the maximum value of absolute error is not more than one unit of least position[10]. To reduce the area, power and delay the truncated multipliers are used. The truncation and rounding of partial product bits are very much useful in the minimization of number of half adders and full adders during tree reduction. Here, there is no necessity to use error compensation circuits and the final output will be précised. The utilisation of truncated multiplier leads for reduction in device utilisation as compared to standard multiplier. The Truncated multiplier design is implemented in FPGS then there is a considerable reduction in FPGA resources, power and delay[17].

In Signal Processing applications the various parallel array multiplication algorithms have been proposed to meet the high speed multiplication. The comparison of various multipliers like Array multiplier, Booth multiplier, Wallace tree multiplier and truncated multiplier are discussed here. Array Multiplier is based on Add and Shift algorithm [16]. Three major steps are involved in parallel array multiplier, i.e., generation of partial products, reduction of partial products, and final carry propagate addition. Partial products are generated from the Multiplication process[7]. The aim of the partial product reduction is to reduce the number of partial products to two, and summed up by the final addition. **B**ooth algorithm is used to multiply signed and unsigned numbers[8]. The number of bits in partial products are reduced by recoding the multiplier. The main disadvantage is that it dissipates more power. In Wallace tree multiplier[4] the reduction scheme starts by regrouping the partial- product matrix into sets of three rows. The number of full adders required can be reduced by rearranging the partial products in the form a tree. Two types of operators are used to reduce the depth of the tree. First one is full adder and second one is half adder, The tree is iteratively covered with FAs and Has. The full adder accept three inputs and generate two outputs. The full adder is also known as 3-2 compressor. The final step for completing the multiplication is to combine the results in the final adder. The choice of the final adder depends on the structure of accumulation array. In general carry look ahead adder is the suitable one, as it provides the minimum delay.

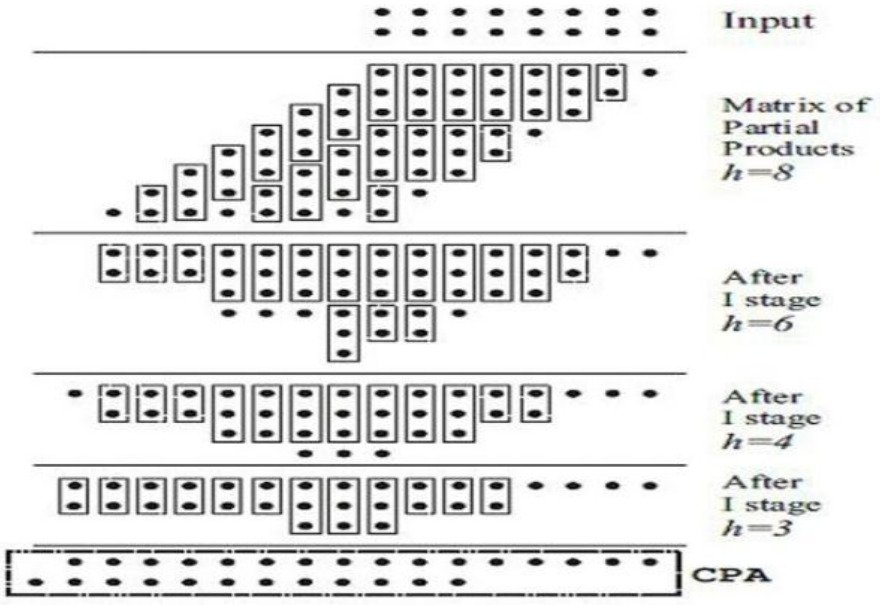

Figure 2.1: Wallace Tree Multiplier

The Truncated multiplication helps to reduce the power dissipation and area by discarding the least significant bits of full width products. A truncated multiplier is an n bit x n bit multiplier with n bit produced as an output instead of 2n bits. Here the least 8 bit of the full-width product results are discarded. Hence there is a significant reduction in the power consumption and area of arithmetic circuit. Constant correction method or variable correction method are used to design truncated multipliers. The lower n bit columns of a parallel multiplier are truncated and the correction is added to most significant columns in constant correction method. To calculate the LSP minor constant value is used instead of actual value of the inputs. The output of the multiplier can be represented as:

PCCM = truncn (SMSP + SLSP major + constant)

where the weighted sum of the elements of the LSP major[13] is SLSP major. In Variable correction method the basic design of the multiplier is similar to that of a constant correction fixed width multiplier. In full width of multiplier the least significant N-2 partial product

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columns multiplier are truncated. the partial product terms in the Nth column are added to the partial product terms in the N- 1 column using full-adders, is done to offset the error introduced due to truncation of least significant N- 2 columns. The variable correction method helps to improve the accuracy of truncated multipliers by compensating the effect of the discarded terms with a non constant compensation function. The multiplier output is calculated as:

PVCM = truncn (SMSP + SLSP major + b (IC) + Kround)

Where b(IC) is a suitable compensation function[13]. The Mathematical basis of truncated multiplier is discussed here. In a standard multiplier, two n-bit inputs are needed and represented as A and B and the following equation represent the operation to obtain the 2n bit product P.

$$A = \sum_{i=1}^{n} a_i 2^{-i}$$

$$B = \sum_{j=1}^{n} b_j 2^{-j}$$

$$P = \sum_{i=1}^{2n} p_i 2^{-i} = \sum_{i=1}^{n}\sum_{j=1}^{n} A_i B_j 2^{-i-j}$$

where a_i represents the ith bit of A and b_i represents the ith bit of B and P_i represent the P.

The 8x8 truncated multiplier output can be rewritten as below.

$$A = \sum_{i=1}^{n} a_i 2^{-i}$$

$$B = \sum_{j=1}^{n} b_j 2^{-j}$$

$$P = AB = \sum_{i=1}^{n} p_i 2^{-i}$$

3. Proposed Work

In the proposed system, the multipliers and adders in the FIR Filter design are modified. Multipliers are to be replaced to Truncated with GDI (Gate Diffusion Input) full adder. Based upon this modification our performance will increases better than existing results. The truncated multiplier will have three options such as rounding, deleting, truncating. Here, the MSB bits will be truncated and the output of n x n multiplication will be provided only n bit level. This proposed work will design in CMOS Logic gate and which 10-T transistor level of full adders with 45nm technology and finally proved the terms of area, delay and power.

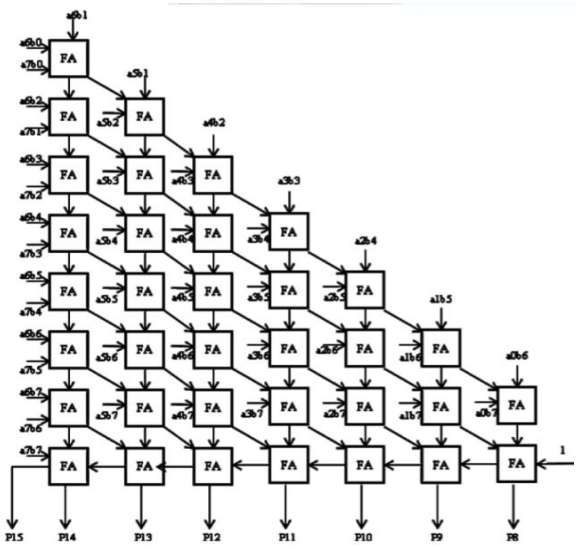

Figure 3.1: Proposed Truncated Multiplier

The Design Flow Fig 3.2 describes about the process flow of entire design of truncated multiplier. Initially the CMOS inverter is designed with the parameters. By using this, 1bit full adder at 45nm technology is designed by two half adders. Then the 8 bit truncated multiplier is designed using the CMOS full adder.

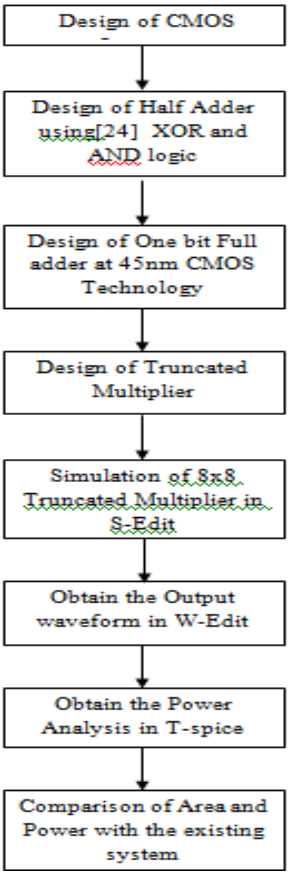

Figure 3.2: Design Flow of proposed work

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Tanner EDA tool is used to realize the half adder circuit. Here the input signal is given through input ports a and b. The output signal comes from the output port sum and carry**.**

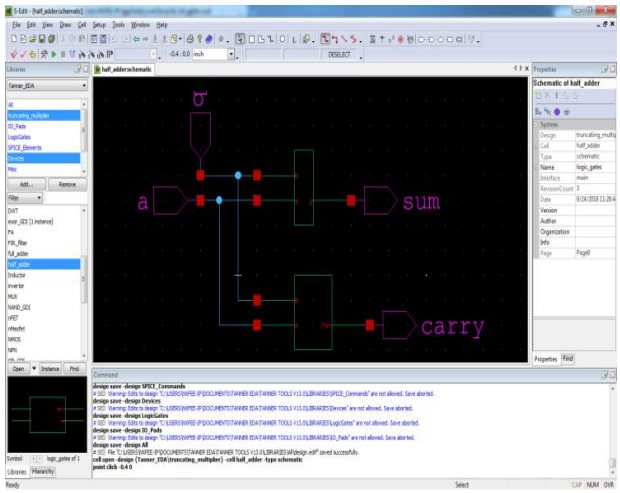

Figure 3.3: Design of Adder

The above Fig 3.3 represents the design of adder. Generally, the multiplication of multiplicand and multiplier generates a partial product and it is added to produce the output. Here the design consist of two's complement circuit partial product generator, parallel adder and the multiplexer. To avoid the sign constraint of FIR filter design, the two's complement circuit is used. The single bit CMOS full adder with 45nm technology is the base element in parallel adder.

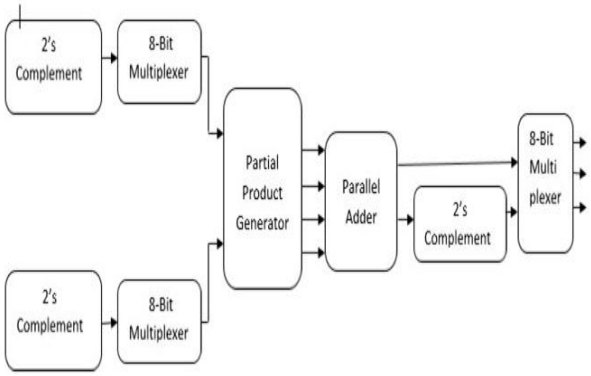

Figure 3.4: Truncated Multiplier Design

4. Results and Discussion

Generally, the multiplication of multiplicand and multiplier generates a partial product and it is adder to produce the output. Here the design consist of two's complement circuit , partial product generator, parallel adder and the multiplexer. To avoid the sign constraint of FIR filter design, the two's complement circuit is used. The parallel adder used is the 1 bit CMOS full adder with 45nm technology.

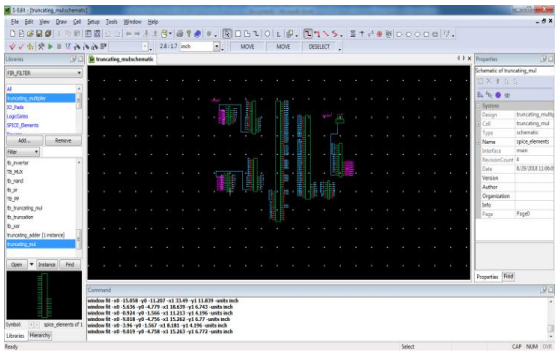

Figure 4.1: Schematic Diagram Of 8x8 Truncated Multiplier

Fig 4.1 represents the schematic diagram of 8x8 truncated multiplier using GDI Full adder. Here the least significant 8 bits are truncated and only the most significant 8 bits are taken for calculation. Since the LSB bits are truncated, the entire circuit size is reduced to nearly 50%, consequently the power will also be reduced.

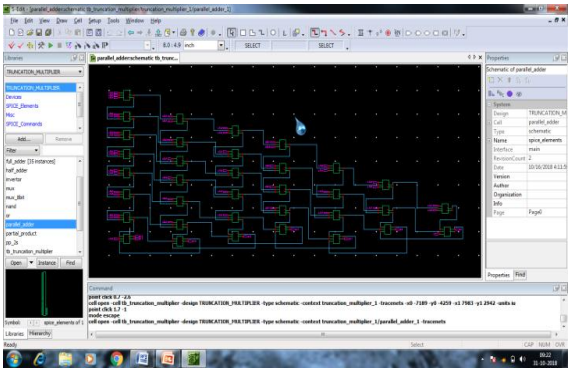

Figure 4.2: Schematic diagram after truncation

The input to the truncated multiplier is given as two's complement of the input which is made to fed to the multiplexer and finally to the multiplier. The output is obtained through out[0-7] respectively.

Let the n-bit inputs and n-bits output of the truncated multiplier is shown below..here n=8

- a0 – a7 = 64
- b0 – b7 = 45

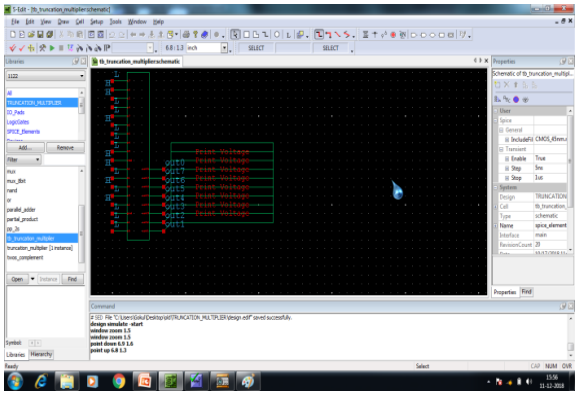

Fig 4.3 Input set up of Truncated Multiplier

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Output:

- P8 – P15 = 1A

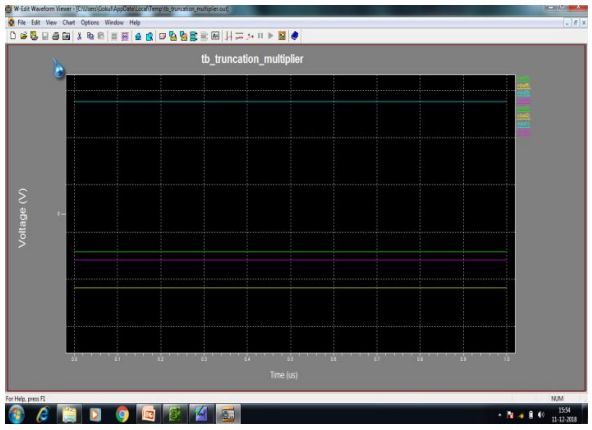

Figure 4.4: Output of Truncated Multiplier

The power consumption of the truncated multiplier is given below in Fig 4.5

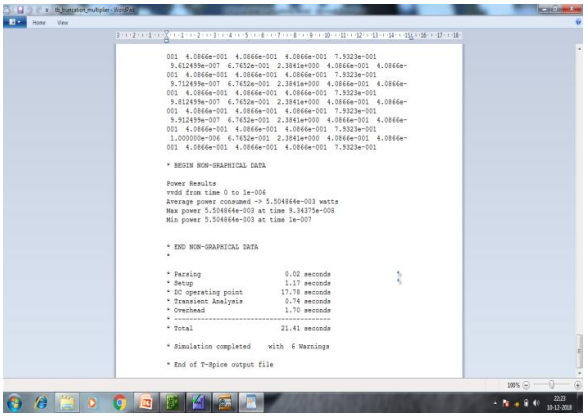

Figure 4.5: Power Analysis of Truncated Mutiplier

Table 4.1 describes about the power consumption of GDI full adder and the truncation multiplier. The CMOS full adder uses 45nm technology, so that it consumes very less power and less delay.

Table 4.1: Power Analysis

Parameters	***GDI full adder***	***Proposed truncation multiplier using GDI full adder***
Technology (nm)	45	45
Power (watts)	7.195048e-005	8.408169 e-003

The Table 4.2 describes about the area utilized by the normal 8x8 multiplier and truncated 8x8 multiplier.

Table 4.2: Area utilization

Number of logic elements	***Used***	***Available***	***Utilization***
8x8 Parallel Multiplier	189	33216	0.57%
8x8 Truncated Multiplier	109	33216	0.328%

5. Conclusion

T The Truncated Multiplier has been designed using the CMOS 10T Gate Diffusion Input(GDI) Full Adder. The simulation results of Truncated Multiplier is compared with the 8 x 8 parallel multipliers and advantages of truncated multiplier over other multipliers has been discussed. The simulation results are generated using Tanner EDA tool .the experimental resilts shows that the proposed 8x8 truncated multiplier design occupies only 0.328% of total area and the power consumed is 8.408169e-003. By comparing the above results the truncated multiplication proves as an proficient method to reduce the power dissipation and decrease in the area of parallel multipliers.

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