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Performance comparison of Array Multiplier with Wallace Multiplier using Reversible Logic Structure

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Abstract:

Over the past few years, research in reversible logic multipliers has done very efficiently to reduce the partial product number. The power and speed of the logic design is efficiently utilized by using reversible Array Multiplier. Array multiplier is an important design in VLSI because, Multiplication involves key role in Arithmetic and Logical operations. From recent years the research has going on multipliers to improve performance in various factors. Here, an array multiplier that produces less delay and efficient power utilisation is proposed using reversible half adder and multiplexer based reversible full adders. By this design the combinational path delay and chip area are decreased.A Wallace multiplier is also developed using the same reversible logic and their power and path delay are calculated to achieve high efficiency. The entire design is developed in Verilog HDL and the software used is XILINX ISE 14.5.

Keywords:*Reversible logic, Array multiplier, Multiplexer, Wallace multiplier, Verilog*.

I. INTRODUCTION

In almost all irreversible hardware outlines the primary difficulty is the indulgence of power. A little extent of energy is dripped out as heat owing to the power indulgence. The heat dissolution will be in very excess quantity that it influences the performance and results in the reduction of life time of the components. The quantity of energy that is not debauched from a system as far as the same permits to replicate the inputs from observed outputs is KTln2 according to Benett. Reversible logic gates comprise the capability to minimize the amount of power indulgence which is the foremost obligation in VLSI design which has low power requirement. It is applied in diverse fields in electronics such as signal processing in optical communications, low power CMOS technology and various computation technologies.

The complexity in the majority of the systems which undergo computing is that they set free some energy in thermal form when their voltage level needs to be altered from positive level to negative level. Reversible circuit elements utilize the principle of shifting the charge from one node to the next progressively instead of altering voltages to new levels [1]. Herewith, only a diminutive extent of energy is anticipated to be vanished on each alteration.

The state of the inputs is not recovered from the outputs in everyday irreversible structures. However, this problem of input recovery is completely overruled by using reversible structures which in addition affects the design of the logic in digital domain. In early days, the structures employing reversible logic which are driven only by their inputs without the necessity of any additional power supply have been implemented. More to the point, the mounting area of quantum computation recognized itself as a hopeful application of reversible logic. In comprehending a reversible logic circuit certain limitations need to be deliberated, i.e., feedbacks and fan-outs are not permitted. In a reversible logic circuit, a mapping on one-to-one subsists amidst the

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input and output trajectories. To assist in maintaining reversibility, standardized subordinate inputs for making the gate functions and garbage outputs to exhibit reconfigurable behavior are essential. It is enormously challenging to comprehend reversible circuits of several qu-bits. Thus, the reduction of the number of secondary inputs and the outputs that are not used is the crucial objective of optimization. Plentiful models of multipliers relying on full adders and half adders which employ reversible logic have been recommended by the researchers in the conventional literature. The transparency is enhanced in provisions of the number of secondary inputs and garbage outputs by the employment of reversible full and half adders for summing up of partial products.

Several designs related to the reversible array multiplier structures have been suggested in the prevailing literature. The approach for designing an array multiplier can be relied on the succeeding two measures. On the very first, engender the partial products by means of the partial product production circuitry employing reversible logic. Subsequently, with the aid of an array of partial and full adders that employ reversible logic, take the partial products that are carried out at first step and accumulate them. In this work, we are assuming that step one which is responsible for the generation of partial product using the reversible partial product generation circuitry will be identical for all multipliers.

II. REVERSIBLE LOGIC GATES

A logic gate is said to have employed with a reversible logic structure if it has the equal inputs and outputs count i.e., n-input n-output logic device. In other words it is said to have mapping of one-to-one among the inputs and outputs. This assists to resolve the inputs from the outputs in a unique way along with the recovery of outputs from inputs. Moreover, in the synthesis of reversible circuits as one–to-many perception is not reversible, an undeviating fan-out is not permitted [2]. Owing to this reason, in reversible circuits, fan-out is achieved using additional gates and also while designing a circuit based on reversible logic structure it should always be remembered that minimum number of gates must be used. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits such as reversible gate count, count of inputs which are constant and outputs which are not used in circuit, cost of basic gates.

There are certain limitations related to design of circuits employing reversible logic that have to be either guaranteed or assured in order to put into practice any particular functions that employ Boolean operations. To begin with, the inputs count is required to be balanced with the outputs count in all the structures employing reversible logic. Subsequently, there must be an output pattern that is unique corresponding to each input pattern. Followed by, only one time usage of each output is allowed, i.e., fan out is not accepted. Finally, the consequential circuit is desired to be acyclic.

In this portion, all about reversible logic and reversible logic gates will be discussed with added apposite examples and figures.

Feynman Gate

Let the vectors corresponding to the input and output of a 2*2 Feynman gate be Ip and Op respectively. Here Ip = (i1,i2) and Op = (O1=i1, O2=i1⊕ i2). The circuit representation for 2*2 Feynman gate is shown in Fig 1.

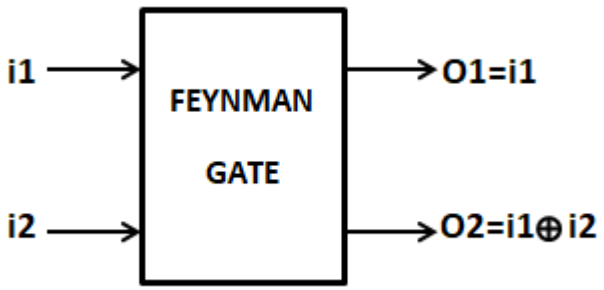

Fig 1: Block diagram of Feynman gate

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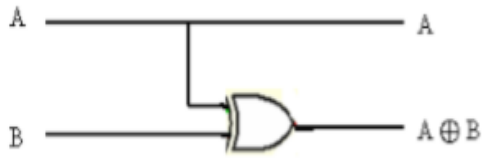

Fig 2: Circuit representation of Feynman gate

Toffoli Gate

Let the vectors corresponding to the input and output of a 3*3 Toffoli gate be Ip and Op respectively. Here Ip = (i1, i2, i3) and Op = (O1=i1, O2=i2,O3=i1i2⊕ i3). Fig 3 shows the 3*3 Toffoli gate.

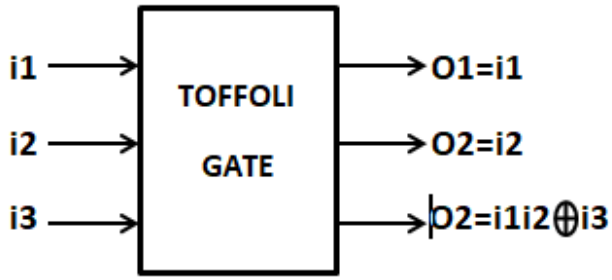

Fig 3: Block diagram of Toffoli gate

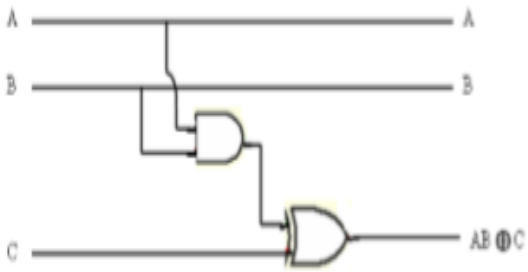

Fig 4: Circuit representation of Toffoli gate

Peres Gate

One important advantage of a 3*3 Peres Gate when weighed against other gates is that it is said to be comprised of low quantum cost. One necessary condition for a Peres gate to attain output is that its third input ought to be identical to zero i.e., C=0..A full adder likewise be developed by combining two Peres gates.

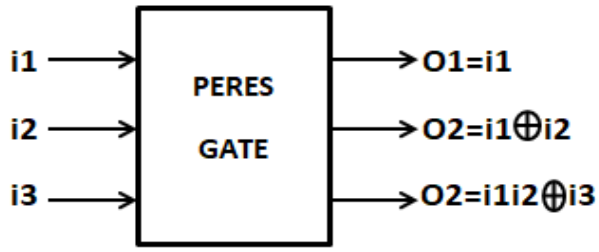

Fig 5: Block diagram of Peres gate

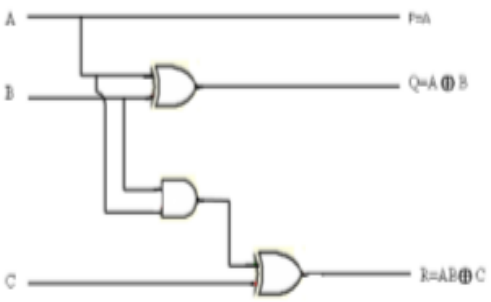

Fig 6: Circuit representation of Peres gate

III. Proposed Array Multiplier Using Reversible Logic Structure

IA multiplier is simply nothing but, it is a logic circuit which is doing multiplication of two or more numbers. If we talk about multiplier then we talk about multiplier from designer side but not from the user side. Here the multiplication operation is done on the numbers only logic 1 and logic 0 i.e., binary, because, the computer or logic circuit takes any number into binary form only. The logical multiplication is done on the basis of basic multiplication rules that are 0 x any number = 0, 1 x 0 = 0 and 1 x 1 = 1. Suppose if we multiply two binary numbers 1011 and 1001 then from the above procedure result would be 01100011. It is an number comprising of 8 bits.

As a result, these multiplication exercises n-shifting operations and n-addition operations to multiply n-bit binary number. The combinational circuit that is designed to perform such multiplication is called as an array multiplier or combination multiplier. To design array multiplier we need to have adders because multiplication process involves addition [3].

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That is why the multiplier is designed with half adders and full adders. The array multiplier basic diagram is shown in Fig 7.

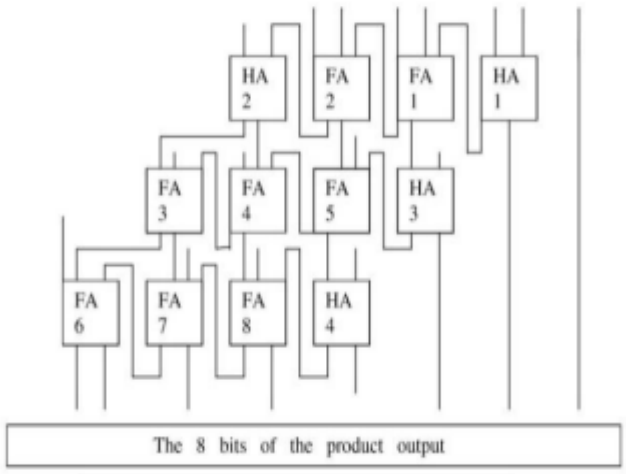

Fig 7: Basic 4x4 Array Multiplier

Full adder means, a logical circuit that performs binary addition of three numbers and produces output as sum and carry. The full adder is plays very crucial role in array multiplier because in array multiplier addition process is involved. Here we designed full adder with multiplexers and ex-or gate using reversible structure, because to reduce time delay and power. We proposed full adder with two multiplexers and one exor gate. Here exor gate output is the control inputs of both multiplexers. The one of the output „sum" is obtained from the first multiplexer and another output „carry" obtained from the output of second multiplexer. In this design we used 2 X 1 multiplexers. The two inputs are applied to exor gate are B and C. And for multiplexers we applied inputs as shown in Fig 8. Here the addition is based on the bits B and C. For example if the inputs B and C are both have logic 1 and A also have logic 1 then sum output is A and carry output is B that is 1 and 1. Because it is purely dependent on exor gate which we connected. By this the full adder operation is satisfied. It is observed that it has quite enhancement in the design than the existing design when compared to delay and power.

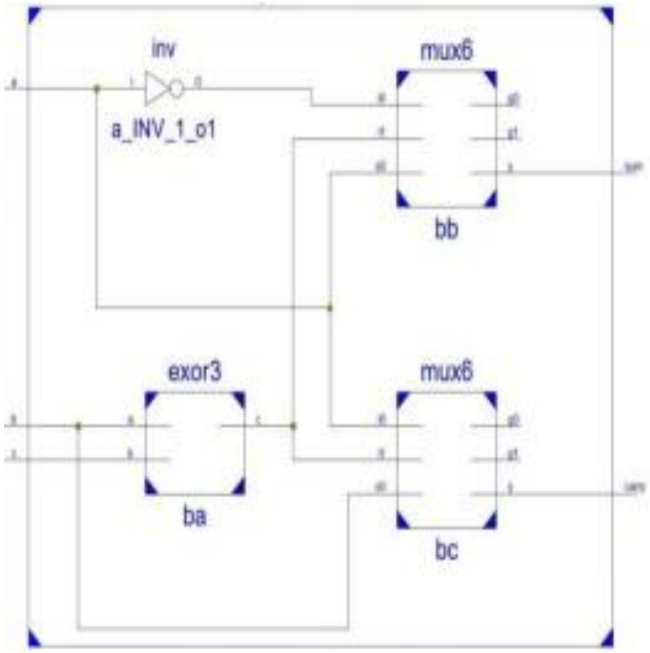

Fig 8: RTL Schematic Representation of proposed Array Multiplier

IV. Proposed Wallace Multiplier Using Reversible Logic Structure

A Wallace tree multiplier has been considered with the aid of an adder which has a converting from binary to excess one circuit and a carry select input [4]. The proposal was set up to be fairly productive in terms of area and power. The binary multipliers both for 8 bit and 16 bit are intended using multi-channel C type Metal Oxide Semiconductor expertise. In this connection, NMOS and PMOS have unalike lengths of their respective channels and the whole design was intended to be power effective with minimal amount of leakage current. In this exertion, we used multiplication algorithm using Wallace tree structure for developing a binary multiplier which carries the operation of multiplication for 4 bit values [5]. A comparative study on the time consumed for obtaining result is carried out between the above mentioned multiplier and 4 bit Vedic multiplier and 4 bit Conventional multiplier by carrying out simulation and the results prove that the multiplier which functions using Wallace tree logic achieved a pretty less amount of delay when compared to other structures.

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To find the delay for the conventional Wallace tree multiplier first so that the results could later be compared with the fast multiplier which is proposed with the help of Kogge stone adder. Therefore, in the architecture of straight multiplier using wallace tree structure 4-bit input A and B are taken so that we get 8-bit output P which is the product for both A and B inputs. Different wires used in between are declared next.Multiplication is a central maneuver in DSP based algorithms [6]. It needs large area, and consumes considerable power. Therefore, there is need of designing low power multiplier for various applications especially in Digital Signal Processing. Wide-ranging work is carried out on low power multipliers at technology, physical, circuit and logic levels. The objective of realizing a good multiplier is to have small size and ultralow power consumption [7]. The primary objective behind this work is to reduce average power consumption of multiplier which in turn saves significant Power consumption of VLSI system such as SoC, NoC and DSP. The architecture of Wallace tree Multiplier is shown in the figure 9.

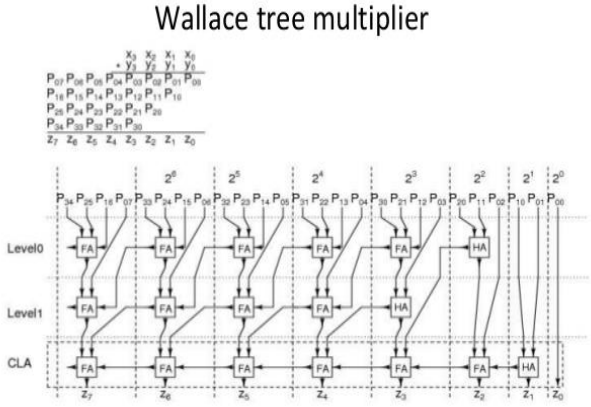

Fig 9: Wallace tree multiplier Architecture

V. Implementation Results

ISim is a tool used to visualize the output signals and XILINX ISE is the software used for implementing different modulation techniques in VHDL.
For proposed array multiplier, 2 four bit numbers are applied as inputs and output results are observed with respect to the applied clock.

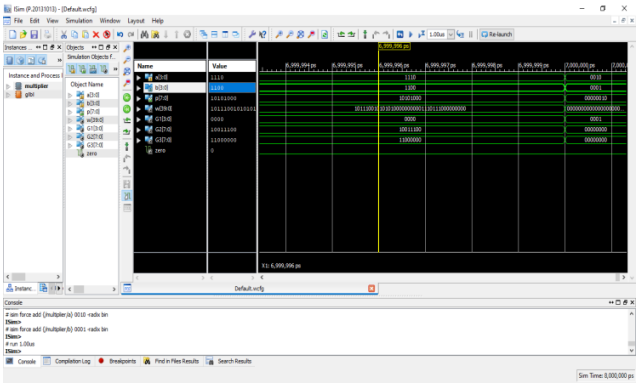

Fig 10: Implementation Results of Proposed Array Multiplier

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In case of a 4 bit Wallace multipliers, 2 four bit numbers are applied as inputs and output result of 16 bits is observed with respect to the applied clock.

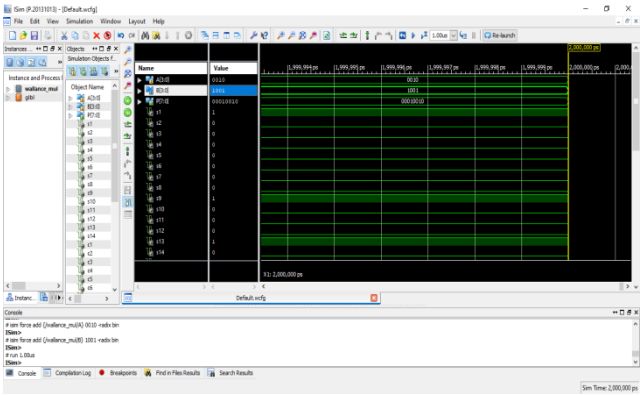

Fig 11:Implementation Results of 4 bit Wallace Multiplier

For implementation of an 8 bit Wallace multiplier, 2 eight bit numbers are applied as inputs and a 64 bit output result is observed with respect to the applied clock.

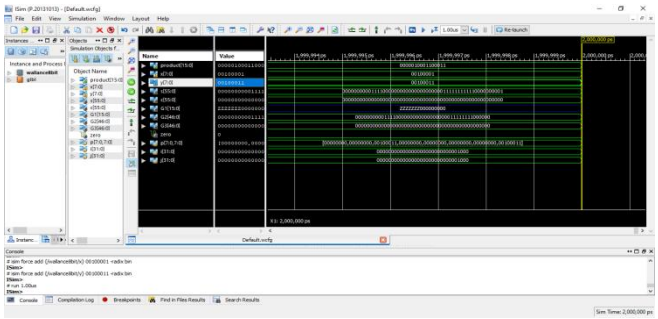

Fig 12:Implementation Results of 8 bit Wallace Multiplier

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The project was designed in Xilinx ISE design suite 1using VHDL. The device used was Virtex4 starter kit. The three multiplier structures proposed here are analyzed in terms of performance. The time delay reports are obtained in the design summary and power breakdown is done using power analyzer generated by ISE Design Suite. The performance comparison of all the three implementations i.e., the array multiplier, Wallace 4 bit multiplier and Wallace 8 bit multiplier are summarized in table I.

Time Delay Analysis

For all the three implementations of array multipler, Wallace 4 bit multiplier and Wallace 8 bit multiplier, time consumption is estimated in Design Summary.

In Wallace 8 bit multiplier, delay is found to be 26.693ns and is reduced to 11.557ns in Wallace 4 bit multiplier because of reduction in number of input bits which is further reduced to 13.833ns in proposed array multiplier which proves to be the best when compared to other multiplier structures.

Power Analysis

This is done in Xilinx using Power Analyzer.

For array multiplier proposed, the power consumed is about 0.092w which is reduced to a greater extent when compared to Wallace 8 bit multiplier whose power consumption is more than 0.132w.

Performance Comparison of Different Multiplier Structures

Parameter	**Delay**	**Power**
Array multiplier	13.833ns	0.092W
Wallace 4bit	11.557ns	0.090W
Wallace 8bit	26.693ns	0.132W

VI. Conclusion

In this project three modules are proposed namely Multiplexer based Array Multiplier, 4 bit Wallace Multiplier and an 8 bit Wallace Multiplier. Comparison of these proposed modules was performed so as to determine minimum power consumption and less path delay. The Multipliers which were proposed show prodigious improvement in various design parameters using Reversible Logic.

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