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Design and Implementation of High Speed Adders Using the GDI and CMOS Technology

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Abstract:
In the recent trends, all industries are focusing on speed, delay, less area and power consumption in the manufacturing of any digital applications. These parameters are requirements in the chip design. In VLSI technology different techniques are present to design any chip. In this paper, we are concentrating only on two techniques i.e. CMOS and GDI (Gate Diffusion Input). The parallel prefix adders (PPA) are implemented using these two techniques. These two techniques are designed in 180nm technology in tanner v13 EDA tools. The GDI technique is better when compared to the CMOS technique in terms of area, delay, power, speed.

Keywords: *VLSI, Low power, CMOS, GDI, back end tool, PPA.*

I. INTRODUCTION

All the digital application using the approximation computation (AC) is sufficient for designing this type of application. The complexity of the hardware is less in approximation adders when compare to the other adders. A digital application such as synthesis, DSP, multimedia, data mining, and wireless communication. All these applications are computed using the AC. The approximation computation recently attracted attention in developing digital applications [1]. The different techniques are used to determine the performances of the logic circuit. The different technique is CMOS, GDI, Pass transistor logic (PTL), Transmission gate logic (TGL).

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The CMOS technique is used for implementing logic circuits for decades. PTL is used for developing the low power VLSI circuits. This technology facing some problems. To overcome these problems different techniques are mentioned above [3]. The problem likes transistor count and low power problem can be overcome by using the GDI method. This method is used for the implementation of different complex logic circuits by using two transistors. From this, we can overcome the problem facing different techniques [4].

The main purpose of the adders is to perform the binary addition for digital systems; these adders are used in computers and different kinds of processors. There are different types of adders are constructed for improving the parameters that are present in the VLSI technology [5]. The adders are used in microprocessors to perform the n number of instructions with in the seconds. All these adders are defined by binary values of 1's and 0's. This research work tells about how the parallel prefix adders (PPA) are constructed and its parameters. The area and delay are very less in PPA with compare to different adders. There are different technology are used for the construction of these types of adders.

The software used to determine the parameters in 180nm and 250nm. We consider 180nm to design the high-speed adders these adders are also known as

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the PPA. Tanner software is used for chip designs with different technique as mentioned above. This software is known as Back End tool in this we are using the version 15.2 [2]

This paperwork consists of 5 sections. Section I describe the Introduction part of the project. Section II speaks about the existing background. Section III carries out the proposed GDI. Results and Tabular column is described in section IV. Section V represents the Conclusion of the project.

II. Existing Background

Parallel Prefix Adders:

The basic adders like ripple carry adder, carry look-ahead adder and so on. But rather than these adders, we are going with PPA is used to overcoming the carry propagation problem that is occurring in the basic adders. The main purpose of going with PPA rather than with basic adders is speed and delay. There are lots of adders that are implemented using parallel prefix adders (PPA) and most of the researchers are concentrated on the Kogge-stone adder (K-S adder) and brent-Kung adder (B-K adder). The important factor of considering these adders is less delay and fewer transistors [6].

In PPA the operation of any adder is done in three steps

- Step1- preprocessing
- Step2 –carry generation signal
- Step3- generation of the sum signal.

The 3 steps processing is shown in figure 1.

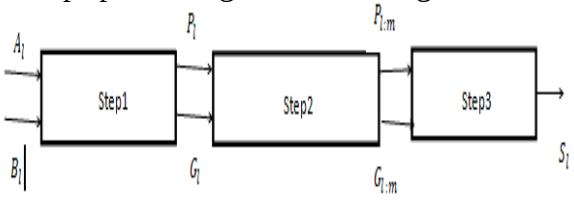

Figure 1: operation steps of PPA adders

- Step 1:

When A_l and $B_l$are set as an input signal, this stage produce Propagate and generate cells. The Propagate and generate cells are represented as below [10]:

$$P_l = A_l \oplus B_l \quad (1)$$

$$G_l = A_l B_l \quad (2)$$

- Step 2:

The output signals from the first step are taking as inputs to the next step. This step is producing the carry signals.

$$P_{l:m} = P_{l:n+1} P_{n:m} \quad (3)$$

$$G_{l:m} = G_{l:n+1} + P_{l:n+1} G_{n:m} \quad (4)$$

- Step 3:

This step will produce the computational sum bits. Stage3 is default for all adders.

$$S_l = P_l \oplus C_{l-1} \quad (5)$$

GDI (Gate Diffusion Method):

The basic structure of the GDI cell is shown in figure 2. This cell looks like the basic CMOS inverter, but they have two differences, firstly this GDI cell having the 3 terminals which are instructed in figure 2. These terminals are mentioned as G (gate input is common to NMOS and PMOS), P (source for NMOS/drain to PMOS) and N (source for PMOS/drain to NMOS). Secondly bulk of NMOS and PMOS are connected to their diffusion [7], [8]. By the bulk effect can be reduced by this method. The PPA's is designed by using this method and CMOS method[9]. The comparison of the delay and transistor are given in the table1 and table 2.

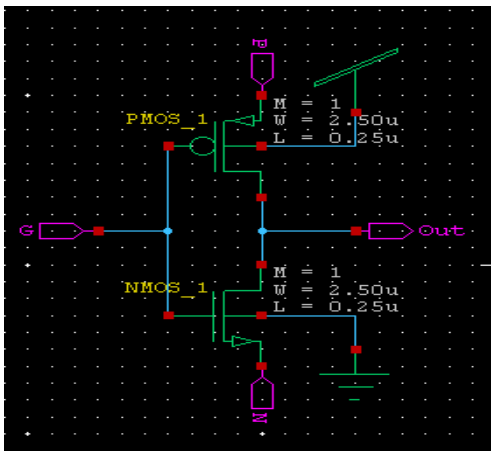

Figure 2: cell of basic GDI

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III. Proposed Method

Parallel prefix adders using GDI and CMOS:

B-K adder implementation:

The $2log_2N - 1$ is used to calculate the stages in this adder. This adder is also known as tree structure. This adder is having the less delay and few transistors. The implementation of this adder is done in two methods which are descried above. In both the methods less delay and few transistors as compare to the other adders that are consider in this research. The implementation is shown in figure3.

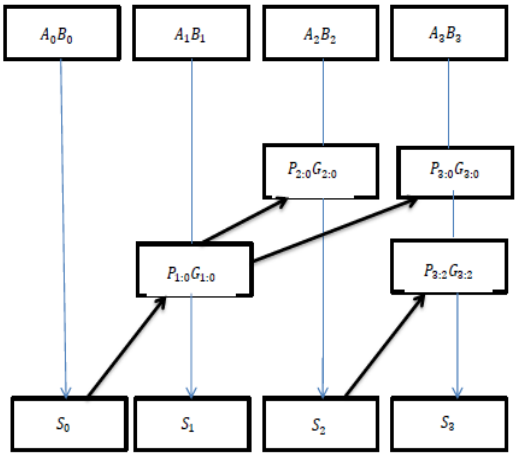

Figure 3: 4-bit b-k adder

K-S adder implementation:

The delay is calculated by using the number of stages that is given as the *log2N* stages. These types of adders are also known as the tree type of structure. These structure consist of long wires between the stages so the delay is more when compare to the other adders. This adder is compared in the both GDI and CMOS techniques. The delay and transistors are mentioned in table 1. The k-s adder is show in figure 4.

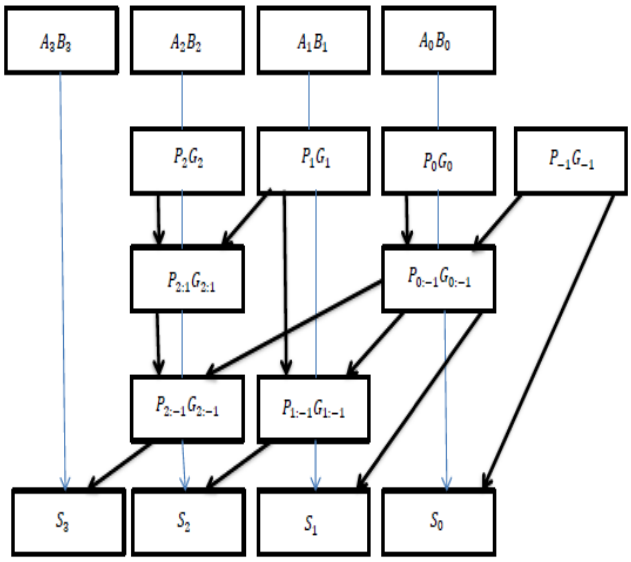

Figure 4: 4-bit k-S adder.

IV. Results

Schematic and simulation:

The schematic and simulation of these adders are designed by using 250nm technology in tanner EDA tool. The delay and fan out are representing in pie chart show in the figure 13 and figure 14.

Parameters	*CMOS*	*GDI*
Delay (ns)	3.77	1.74
Fan out	232	72

Table 1: comparison of B-K adder in CMOS and GDI

Parameters	*CMOS*	*GDI*
Delay (ns)	2.44	1.66
Fan out	220	66

Table 2: comparison of K-S adder in CMOS and GDI.

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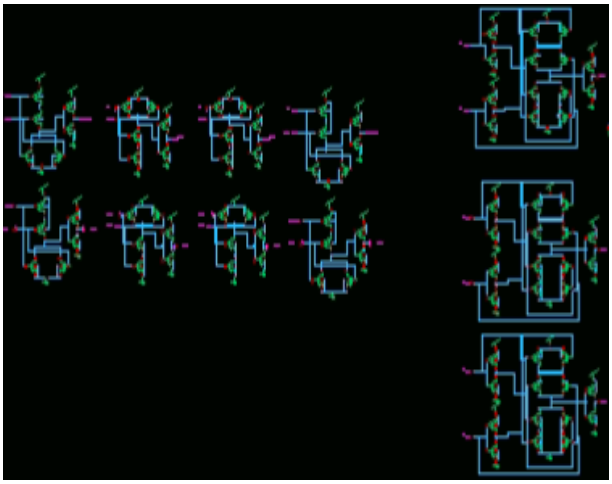

Figure5: 4 bit B-k adder schematic of CMOS.

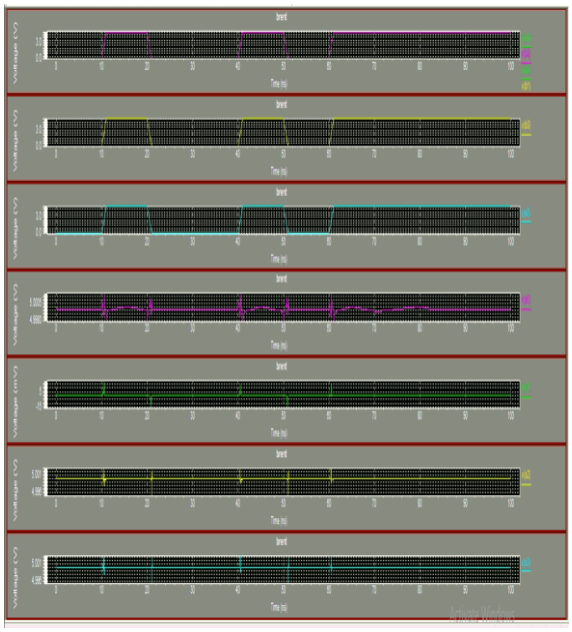

Figure6: simulation of B-K adder of CMOS.

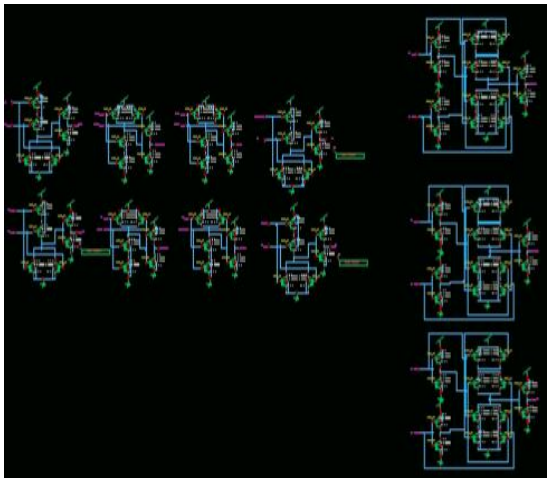

Figure7: 4-bit K-S adder schematic of CMOS.

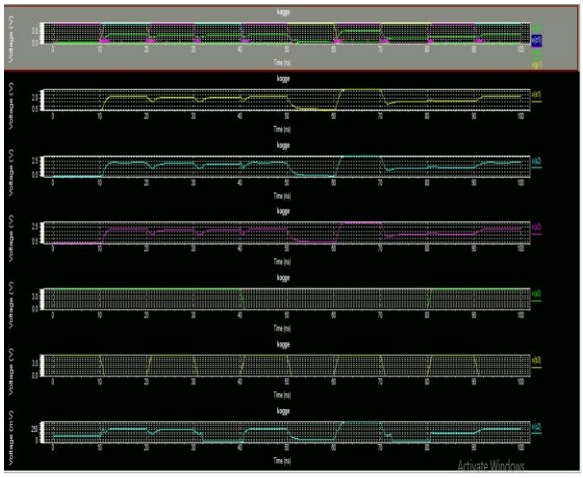

Figure8: simulation of K-S adder of CMOS.

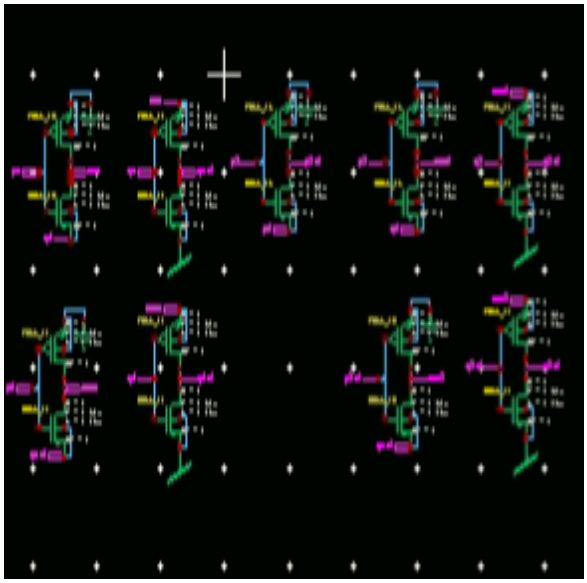

Figure 9: 4 bit B-K adder GDI.

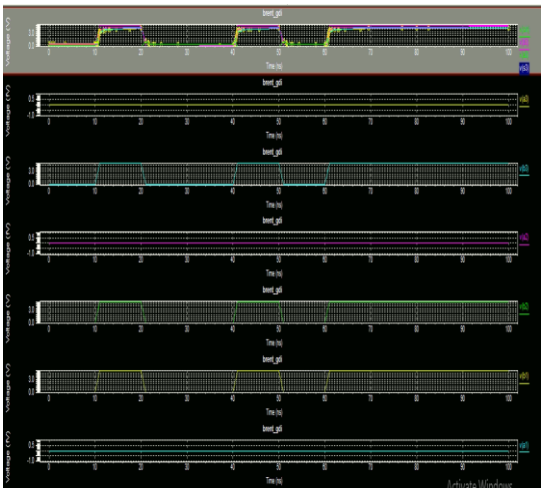

Figure 10: simulation of B-K adder in GDI.

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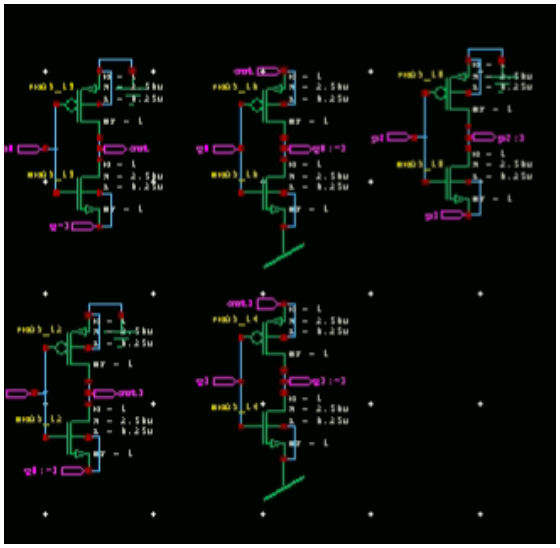

Figure 11: 4-bit K-S adder in GDI.

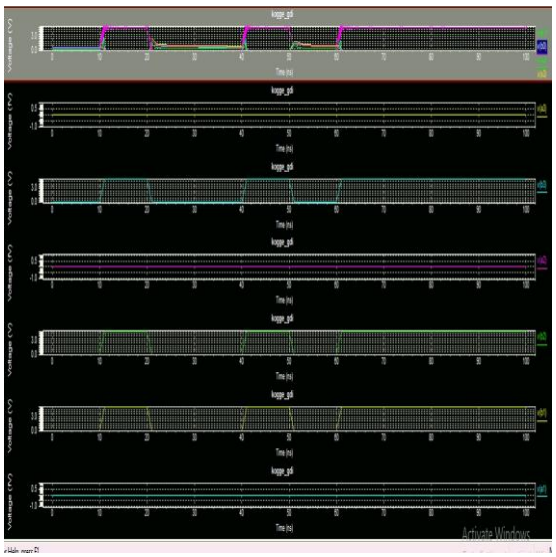

Figure 12: simulation of K-S adder in GDI

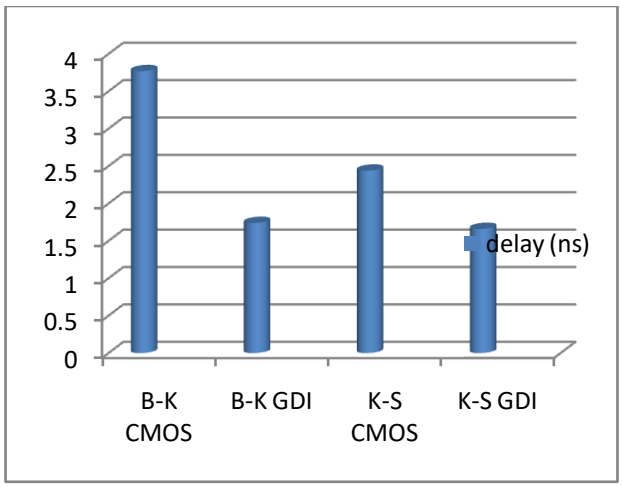

Figure 13: Delay compassion for B-K and K-S adder in CMOS and GDI.

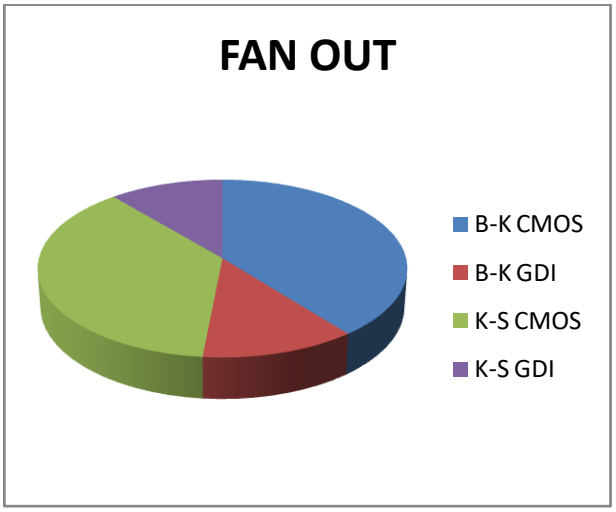

Figure 14: Fan out compassion for B-K and K-S adder in CMOS and GDI.

V. Conclusion

These types of adders can be used for high speed operation. These adders implemented using the two techniques that are present in this paper. The GDI and CMOS methods are suitable the high speed operation, but GDI method has less delay and few transistors compared to CMOS method. So we prefer GDI method for designing any high speed adders

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