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Design and Implementation of Smart Electronic Voting Machine Using FPGA

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Abstract:

Voting machines are implemented by using different techniques like Arduino microcontroller. This paper proposes FPGA based Electronic voting machines. EVMs are combination of electromechanical equipment (including hardware and software). This device is used to cast, count votes and display election results. Initially these machines were mechanical but in the latest technologies undergo many upgrades to electric voting machine due to lack of security and accuracy. EVMs are developed for smooth and secured elections. The voting machines are highly basic in configuration and efficient to utilize and implement. Authorities says these machines are tempered evidence as these are standalone machines are needed to be associated with external firmware. this paper proposes the EVM which provides high security by encryption, 20% efficient when compared to microcontroller, less power consumption in terms of milliwatts, voters friendly, flexible, portable and with less expensive.

Keywords – *Spartan 3E FPGA Kit, Arduino, Xilinx ISE Software, Micro Controller*.

I. INTRODUCTION

The Electronic Voting Machines are often invoked on SPARTAN 3E FPGA hardware kit by dumping the VHDL code into it. Once the VHDL code is dumped and therefore the FPGA board is ready, we will assign different ports to shifted signals present in our software. Electronic Voting process is the standard means of organizing elections using EVMs, sometimes called Electronic Voting Machines in India. The use of EVMs and electronic voting was implemented and verified by the state-owned Electronics Corporation of India Limited (ECIL). Electronics within the 1990's. These are introduced in Indian in the period of 1998 to 2001. The EVM'sare utilized in all state and central elections of India since 2004.

Fig: 1 – General Voting Scenario Components

Before the introduction of electronic voting machines, India used mechanical devices, paper ballots and manual counting. The paper ballots process was widely criticized because illegal voting and booth capturing, where supporters of gathering are caught corners and adjusted them with counterfeit polling forms. The printed paper voting forms were additionally costlier, requiring significant post-casting a ballot asset to tally huge

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numbers of individual voting forms. Inserted EVM highlights like electronically restricting the speed of throwing votes to five for every consistently, a security lock-close element, a web database of casting a ballot marks and thumb impressions to approve the character of the voter, leading decisions in stages more than half a month while conveying broad security at every corner have diminished discretionary maltreatment and misrepresentation, kill stall catching and make progressively serious and more attractive races. Indian EVMs are remain solitary machines worked with once compose, ROM. The EVMs are created with secure assembling practices and style, are independent, battery-fueled and come up short on any systems administration capacity.

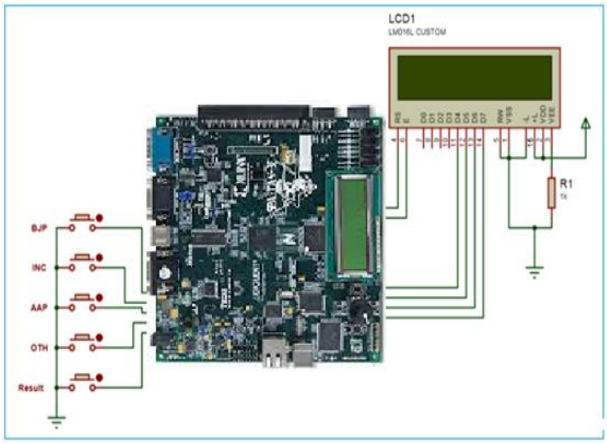

Fig: 2 – Basic Design Implementation.

India is one of the world's largest democratic countries with a population of 1.1 billion, has the number of voters of 900 million people with 1035 thousands polling stations, over 1.37 million voting machines and 543 parliamentary constituencies' covers 5.5 million polling officials. The history of election process enforced us to specialize in the utilization of new technology in Electronic voting process. The existing voting mechanism has numerous security issues, and it's very difficult to demonstrate even basic security perspectives about them.

Voting systems that can be correct demonstrate has many complications. Some of the important needs of government concerning electronic voting process are to enhance election activities and to limit the expenses involved in election process. Still there is a chance of verification of voters in electronic voting system in terms of security and to protect the EVM from felon. This paper provides other countries overview using e-voting system. The comparative study on the implementation of electronic voting systems is international level design is contested in this paper. The electronic voting machines are expected both to accelerate the tallying procedure and to decrease blunders.

Advantages of Electronic Voting Machine over the conventional ballot box/paper system are

i. It minimized the cost of printing almost zero
ii. It decreases to a great extent in expanses a large number of trees are used to make the quantity of paper making this process eco-friendly.
iii. It eliminates the possibility of invalid and uncertain votes which is the root causes of dispute in election appeal.
iv. It makes the methodology of checking the votes a lot quicker than the conventional system.

II. RELATED WORK

Initially EVMs are implemented on Arduino board (ATmega328P) manufactured by Arduino.cc. The Arduino microcontroller boards are designed with 14 digital I/O pins, 6 analog I/O pins. This board can be programmable with (IDE) Integrated Development Environment.

Later on, due to some technical issues EVMs are implemented on 8051 microcontrollers. In 1981 Intel manufactured 8051 microcontrollers. It is an 8-bit microcontroller. It is featured with 4kb of ROM storage and 128 bytes of RAM storage, 40 pins in DIP (dual inline package), 2 16-bit timers. It also consists of four 8-bit ports placed in parallel, which can be used for both programming and addressing as per the requirement. An on-chip crystal oscillator

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with frequency 12 MHz is integrated in 8051 microcontrollers.

FPGA board is a pre-fabricated silicon chip that can be electrically programmed to implement digital designs. Initially, static memory-based FPGA chip known as SRAM is used for configuring both interconnection and logic using a stream of configuration bits. Today's modern FPGA contains approximately 3, 30,000 logic blocks and around 1,100 inputs and outputs.

The programmable logic block provides basic computation and storage elements used in digital systems. A basic logic element consists of programmable combinational logic, a flip-flop, and some fast carry logic to reduce area and delay cost.

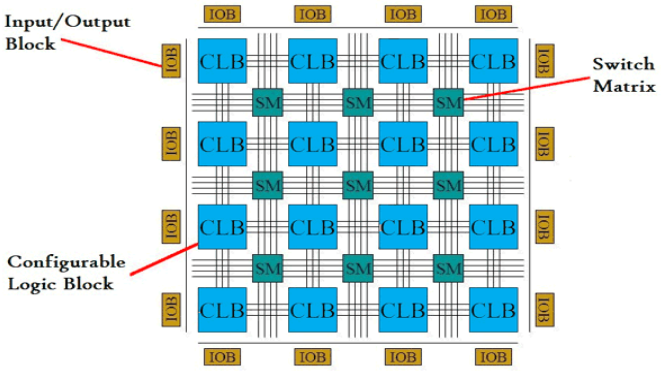

Fig: 3 – Xilinx Board Architecture.

In FPGA electronic voting system procedure keep up the exacting protection and uprightness of the vote threw and validation before the voter is cast their votes. In FPGA voting system security is main concern in online voting vote casting transference is also considered. Automatically, sort the votes and votes are calculated automatically after election time is over.

In FPGA voting process authentication is the major concern, only authenticated voter can cast their vote to the candidate. Person can be authorizing by some methods that can be secrete message or user identity proof, personal identification number (PIN), All authenticated details will be collocated by voter. All authentications are verified within the main database. Authentication is verified by the biometric identification process then voter is allowed to cast the vote.

In order to reduce these issues, the researchers advice moving to a voting process that provides higher transparency, such as optical scan, precinct count, paper ballots or a voter verified paper examine trail, in any of these systems, unidentified voters in principle, scrutinized the manual counting process to make assurance that the outcome is correct. But Election Commission of India rectifies that for such tampering of the EVMs, EVMs can be accessed by someone, and good technical skills are required. EVMs are managed under high security which can be observed by candidates or their assistants all the time, it is not possible to gain virtual access to the machines to manipulate the results of an election, lot of machines will be needed to tamper with, which is almost impossible given the hi technical and time tedious nature of the tampering process.

Since the start of using the electronic voting machine, this system has numerous upgrades and updates. These upgrades and updates involve changes from manual to technology, paper-ballot to a paperless, offline to online, mechanical to electronic, polling based stations to remote places and so on. In this paper, we examine the above issues of the electronic voting machine also the development of its revolution and legalization, security and protection, vulnerabilities and hacking, guidelines and recommendations, vulnerabilities and hacking, and the similar in course of time.

1. Comparison of Parameters with Existing Systems.

Design Metric	Arduino	Microcontroller	FPGA
I. **Execution**	Serial execution	Serial execution	Parallel execution
Language	C, C++	Assembly Language (Hexadecimal codes)	VHDL, Verilog

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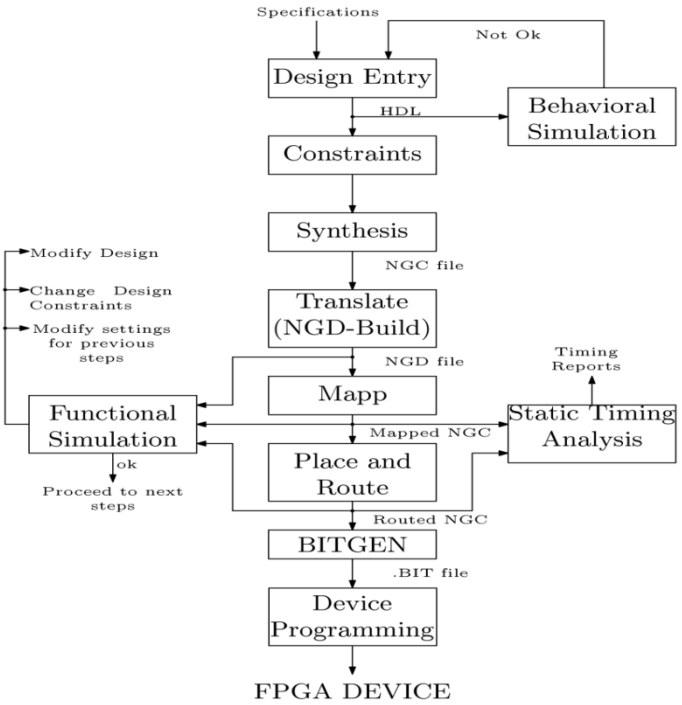
Efficiency	Less	Moderate	high
Power consumption	0.054 mA with the 3.3 V	6.5mA	12V, 1Amp
Accuracy Clock speed	16 MHz	12 MHz	200-500 MHz
Storage capacity	Less (Flash, EEPROM)	External chips are needed	In built
Memory Used	SRAM	4k on chip ROM 256 bytes of RAM	128 MB Strata Flash Memory.
Size	68.6 mm × 53.3 mm [2.7 in × 2.1 in]	5.3×1.6×0.8cm	28 cm x 20 cm x 8 cm
Cost	₹499	₹ 1,299	₹ 22,000
Propagation delay	Milliseconds(m sec)	Microseconds (µ sec)	Nanoseconds(n sec)

III. Sequence of Steps During Implementation.

A. Proposed System Design Flow



II Fig: 4 – Basic System Design Flow.

B. Design Entry.

There are different techniques for design entity. Some of the basic design entries are given below:

- Schematic based
- Hardware Description Language (VHDL, Verilog)
- Combination of both Implementation

C. Synthesis tool (XST).

The process which translates Verilog or VHDL code into a device net list format i.e. a complete circuit contains of logical gates, flip flops for the design. Synthesis process will verify code syntax and analyze the hierarchy of the design which results that the design is optimized for the design architecture. The final net lists are saved to an NGC (Native Generic Circuit) file for Xilinx Synthesis Technology (XST).

D. Implementation.

- Translate process
- Map process
- Place and Route

E. Device Programming.

But the design must be converted into a bit file format so that the FPGA can understand it. The routed NCD file is then taken to the BITGEN program to generate a bit stream (a. .BIT files) now the design must be dumped on the FPGA. This can be used to configure the target FPGA device.

F. Design Verification.

Verification will be done at multiple stages of the process.

- **Behavioral Simulation** (RTL Simulation)
- **Functional simulation**(Post Translate simulation)
- **Static Timing Analysis**

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G. ISE Simulator (ISim).

ISim supports the following languages:

- Verilog IEEE-STD-1364-2001
- VHDL IEEE-STD-1076-1993
- VITAL-2000
- Standard Delay Format (SDF) version 2.1

H. Procedure.

votingmachine Pr	
Project File:	evm.xise
Module Name:	votingmachine
Target Device:	xc3s500e-4fg320
Product Version:	ISE 14.7
Design Goal:	Balanced
Design Strategy:	Xilinx Default (unlocked)
Environment:	System Settings

Fig: 5 – Project File

Open Xilinx ISE software go to new project and create new project saved in new directive select synthesis tool XST and ISE simulator go to file create source file and the code is written in VHDL language synthesis the code by using check syntax and create test bench file combine with source file simulate behavioral model for test bench synthesis then generate user constrain file to convert VHDL code to bit file to implement the program on the Xilinx kit.

IV. System Implementation:

Signal Requirements Table.

SIGNAL NAME	SIGNAL PURPOSE	NUMBER OF SIGNALS	RANGE OF OUTPUT
CLOCK	Provides timing reference for operations	Only one signal.	Binary value1-digit.
CLEAR	To erase previous data	One signal.	Binary value1-digit.
CONTROL SIGNAL	Monitors eligibility of the voter; default=0; becomes 1 when the voter has voted.	As many as the voter signal; 8 signals.	1-digit binary value.
VOTER'S SIGNAL	Contains the information of the candidate to which vote has been casted.	The number of voters allotted for a polling booth; 8 signals.	For this case, giving4 combinations for 4Candidates 2-digit binary value.
STATUS SIGNAL	Displays vote after each voter has casted the vote. Displays when control signal is 1.	The number of control signal; 8 signals.	1-digit binary value.
CANDIDATE SIGNAL	Updates and gives information about the vote casted for candidates. Gets updated with each voting.	Equals the number of candidates contesting in the division; 8 signals.	Range of integer values equaling to the total number of voters.
WINNER COUNT	Displays the final winner of the election process.	Only one signal.	ASCII values to depict the winning candidate.

V. Hardware Implementation.

A. The Electronic Voting Machine can be implemented on hardware using SPARTAN 3E FPGA kit by burning the VHDL code into it.

B. Once the VHDL code is burned and the FPGA chip is ready, we can designate various ports to various signals present in our software.

C. After designating ports, a PROM file is

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generated and load FPGA with specified bit file and the designed logic is ready for implementation.

D. Since on a typical SPARTAN 3E kit provided by Texas Instruments, we have only four input ports, in order to accommodate our signals, we can interface connectors with the SPARTAN 3E kit.

VI. Experimental Results

As, if we have executed and flashed the code into the Xilinx Spartan 3E device. We will be able to see the synthesis report as shown below will be generated. The synthesis report is:

```
=========================================================
*                     Synthesis Options Summary
=========================================================
---- Source Parameters
Input File Name                    : "votingmachine.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "votingmachine"
Output Format                      : NGC
Target Device                      : xc3s500e-4-fg320

---- Source Options
Top Module Name                    : votingmachine
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
```

Fig: 6 – Synthesis Report

For now, let's look into the output of the electronic voting machine VHDL code.

Output-1 Case-I: Initially at 0(n sec), Every input and clock are set to Zero i.e., Initial state. After clock period duration(10ns) the reset input is set to '1' and then reset to '0' that indicates that operation is started. So, the output image will be looks like as shown in Fig: 7.

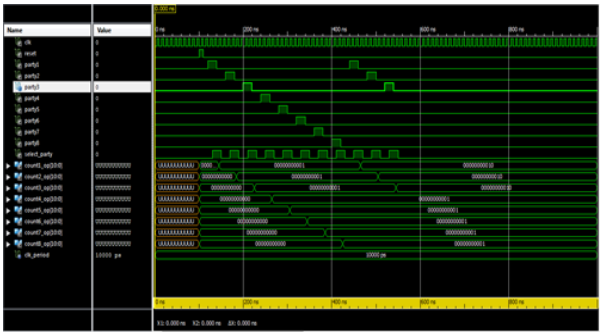

Fig: 7 – Output-1 @ Initial State.

Output-1 Case-II: Whenever the reset input is set to '0' then the actual process of EVM starts. As shown in the Fig: 7, after 10(n sec) the party1 input is given and then next the select party for party1 is also given. Then the output count1_op count has increased from 0 to 1. Similarly, for the next eight party inputs.

Output-1 Case-III: Till now, this is not a problem but now if multiple votes has casted for party1 in the next clock cycle duration as shown in Fig: 7. Then the process is the same he/she has to give input to the corresponding party and then he has to select with "select_party" input. Then, the respective parties output count can be incremented.

Output-2: So, now we got the idea of EVM is working fine. So, let us give multiple party inputs and check the count at the output. So, the output of the corresponding scenario is as shown in Fig: 8.

Fig: 8 – Output-2 @ Multiple party Voted Scenario.

So, now if we just have observed the inputsselected parties and we can clearly observethe outputs of corresponding party in the simulation graph as an 8-bit value.

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VII. Conclusion

The designed Electronic Voting Machine can be used for secure voting, where the tampering of votes has very less probability. It is easy to build and a large number of votes can be casted and recorded depending on the memory of the system. Since it does not contain any memory card and has a password which is digital in nature. It provides a secure system for conducting elections.
This can be further extended to online system by using Internet Of Things (IOT) which is useful to cast the vote in remote places and people living in distant places security can be improved by Block chain algorithm

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