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Design of Carry Select Adder based on a Compact Carry Look Ahead Unit using 18nm Fin FET Technology

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Abstract:

In all the arithmetic operations, addition is one of the most important and initial operation used everywhere. The operation is performed by many adders present in the digital world. These adders gives us carries with preferred delay and power. The three main features like structure, logic used and the compact circuit layout helps to design a better adder. In this paper the CSA adder is built or designed using the compact carry look ahead adder which is the vital component. The adder CSA is designed using the software tool called cadence with the FinFET technology. This technology is the fastest and much used in the present world for designing the VLSI circuits. Cadence software is more sophisticated and advanced tool which provides us the results in accurate values. The carry select adder which is represented is simulated using the Cadence tool and designed with FinFET transistors of different specifications. The FinFET technology used in this paper is 18nm. The carry select adder present in this paper is suitable for the VLSI implementation. The carry select adder is estimated with static and compact carry look ahead adder with a simple select circuit. These adders are used in electrical industries for fast and exact results in the large circuits. The FinFET based CSA is designed and parameters are calculated in this paper.

I. INTRODUCTION

Adder is one of the most common used digital feature in the sketch of digital built-in circuit. Carry choose adder furnish a properly compromise between value and performance in carry propagation adder design. From the structure of raise pick out adder there is nevertheless a scope of lowering the vicinity and electricity consumption with mild extend in delay. In this paper the amendment at gate stage is introduced. The modified architecture is applied for 16-bit, 32-bit, 64-bit and evaluate the delay, strength and vicinity with the normal raise pick out adder [1]-[5].

From the above chapter we have learnt the basic structures of the CLA, CSA and their behavior. The methodology that we are using to present the carry select adder with the help of the software tool called cadence using FinFET technology. Both the carry look ahead adder and the carry select adder are built with the components like RCA and multiplexers. But in the proposed work we are using carry look ahead as the main component for the construction of the CSA. The representation of the carry select adder is based on the static and compact multi output CLA. The cadence software used to obtain the required outputs and also helps to achieve the power, area, performance calculations.

II. FinFET Characteristics and Modeling

CMOS circuits have been invented in 1963 with the help of Frank Wanlass at Fairchild Semiconductor. In 1968 with the help of a group which was led by Albert Medwin the first CMOS built-in circuits were made using RCA (Ripple Carry Adder). Later in the 7400 series, many functions were introduced and

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came into picture and to be manufactured in CMOS, nMOS, Bi-CMOS or every other variant.Complementary MOSFET (CMOS) innovation is generally utilized today to shape circuits in various and changed applications. The present PCs, CPUs and mobile phones utilize CMOS because of a few key points of interest. CMOS offers high noise margin, moderately fast, low power dissipation in the two states, and will work over a wide scope of source and input voltages [6]-[9].

The present semiconductors are cheaper, smaller, faster and cooler when compared to the past few decades semiconductors. The electronic units which are based on the ideas of the solid state physics deliver an extreme good substitute to the vacuum tubes, switches and amplifiers. The process similar to the printing is used for the fabrication of integrated circuits that are linked with the various transistors.Thus the dimensions of the present transistors has evolved with computing, making structures like thinner, speedier and with extra energy efficient.

2.1 Demerits of CMOS

In phrases of CMOS technology for enforcing vision chips the negative aspects are as follows

1. **Photodetectors:** The photodetector constructions are now not distinguished in any of the way of processing. The functions are desired based on the designer's view of manufacturing.
2. **Analog circuits design:** The top most facet techniques are not distinguished for the construction of the analog circuits.
3. **Second order effects:** The 2d ordered machine characteristics like subthreshold operation are not concentrated and are removed for better improvement in the scaling technique.
4. **Mismatch:** In CMOS devices, mismatch is notably high. This is due to the obstructing of the reliability of analog processing in the chips.

2.2 CMOS SCALING PROBLEM

Over the past few years, CMOS scaling has been considered as the leading driver of theelectronics enterprise and has supplied a path towards both quicker and denser integration. The transistors that are manufactured these days are 20 times faster and occupy less than 1% of the place area of those built 20 years ago.

The wide variety of chips and overall performance of the system are increasing gradually from the past few years. The overall performance improves when there is reduction in the channel length. The density increases when there is a decrease in the switching tournament. But the whole circuit per chip and density, the electricity consumption has been increasing for the total chip [10]-[14].The need for extra overall integration and performance has increased the scaling traits in almost each and every system parameter, such as lithography, channel length of high quality, dielectric thickness of the gate terminal, device leakage, input supply voltage etc. Some of the parameters are coming near quintessential limits and selections to the current fabric buildings may also need to be continued in scaling for identification.

2.3 FinFET

A Fin field-effect (FinFET) transistor is a multi-gate device, a MOSFET is built on a substrate place the gate is positioned on two, three, or 4 facets of the channel or it can also be wrapped around the channel, forming a dual gate structure. These units have been given the widely wide-spread identity "FinFETs" because of the source and drain regions that form on the surface of the silicon. These FinFET devices have high contemporary density and high switching capacity when compared with the CMOS technology.FinFET is a type of non-planar transistor or a 3D transistor. This transistor is the main element that is used in the present nanotechnology semiconductor gadget fabrication. Microchips which are utilizing the FinFET gate grew to be more commercial on the early days of 2010 [15]-[18].

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FinFET innovation has as of late observed a significant increment in appropriation for use in integrated circuits. Compared with the more normal planar innovation, FinFET transistor innovation offers some huge focal points in IC structure. The FinFET innovation vows to provide a better degree of versatility required than guarantee that the present advancement with expanded degrees of coordination inside incorporated circuits can be kept up [5]. The FinFET offers numerous focal points regarding IC preparing that imply that it has been embraced as a significant path advances for joining inside IC innovation.The FinFET structure consists of a fin like skinny physique on the substrate. The gate terminal is wrapped all over the channel offering terrific control from the three aspects of the channel. Thus the structure is known as FinFET as per the below Figure 1, because of the Si physique fin which resembles as a fish.

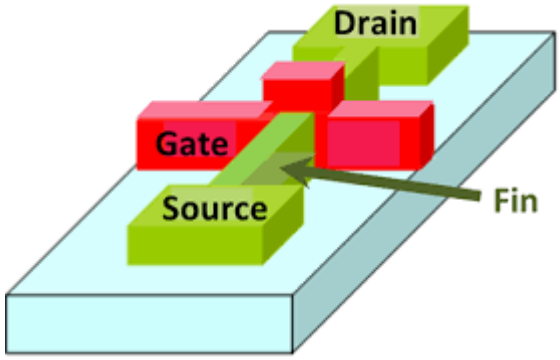

Figure 1. FinFET structure

The gate which is wrapped around is used to reduce the leakage current and also by increasing the effectiveness. Smaller the fin size gives us more flexibility that leads to multiple fins which in turn leads to more silicon area. Larger the fin size may lead to structural instability and also requires less silicon. Different types of FinFET and their architectures are discussed in the [2]. If the channel length of the MOSFETS is reduced then the short channel effects length increases. The channel shows less conductance when no voltage is applied to it on the gate terminal [19]-[20].

2.4 Benefits of FinFET

To exploit various advantages of FinFET, it is manufactured into two kinds: (1) Dual-gate FinFET, which cut downs the overabundance silicon by creating the channel utilizing a ultra-fragile layer of the silicon that is on a protector, along these lines the electric field from the entryway to the blade which is on the top is radically decreased. It is discussed in the paper [13].

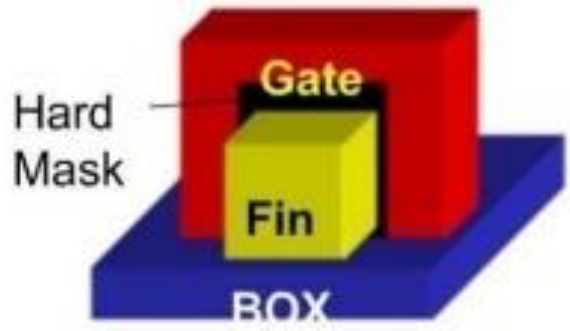

Figure 2. Dual gate FINFET

Tri-gate FinFET, where the FET door folds over 3 sides of the transistors raised channel, or "balance". Since balances are made vertical in nature, high pressing thickness can be accomplished, by pressing transistors closer. Further, to get much more execution and vitality effectiveness gains, creators additionally can keep developing the tallness of the fins.

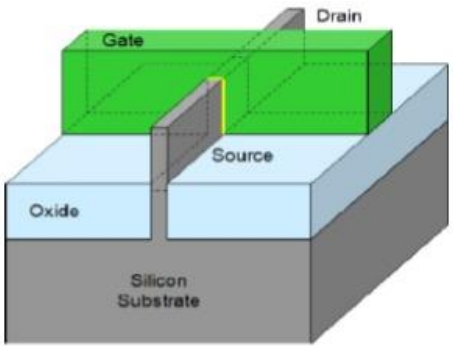

Figure 3. Tri gate FinFET

FinFET innovation gives various focal points over mass CMOS, for example, lower spillage, subsequently lower power utilization, no irregular dopant fluctuation, consequently better portability and scaling of transistor past 28nm, higher drive current for a given transistor impression, henceforth higher speed.FinFETs give various preferences and a

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few key weaknesses contrasted and mass planar procedures. Advantages incorporate expanded voltage headroom for circuits, for example, cascodes, lower gate resistance, which assists monitor with flicker noise to be in control, just as improved coordinating, higher current drive and higher increase [8].

III. Carry Look Ahead Adder

In ripple carry adders, every block has two bits which are brought instantly. Every block waits for the carry from the preceding block. Until the input carry is known there is no way or generating the sum.Carry look ahead adder is simply labeled as CLA which is another version of RCA. Carry look ahead adder is one of the fastest adders that are available in the digital logic circuits. CLA is used to obtain the carry bits more fast when compared to the adder that are manufactured before. The carry look ahead adder is made up of full adder which accepts input signals and also produces carry if needed.During the process of obtaining the carry bits its works slow and considerable delay is produced because of the blocks. That delay is named as carry propagation delay.

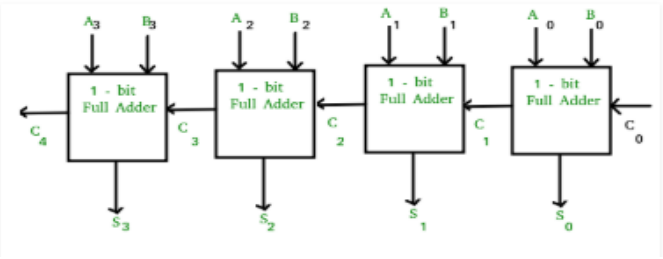

Figure 4. 4-bit ripple carry adder

The above Figure 4 tells us about the carry C_4 that is produced is depending on the inputs given to the block and also the previous carry bits like C_3, $C_2$and C_1 from the remaining blocks. That means the adder propagates a delay for producing a carry. The propagation time that is produced is calculated as the propagation delay by each block multiplied by number of blocks in the adder. To reduce the defects produced in the above Figure 5 there is a gate level circuit which reduces the propagation.

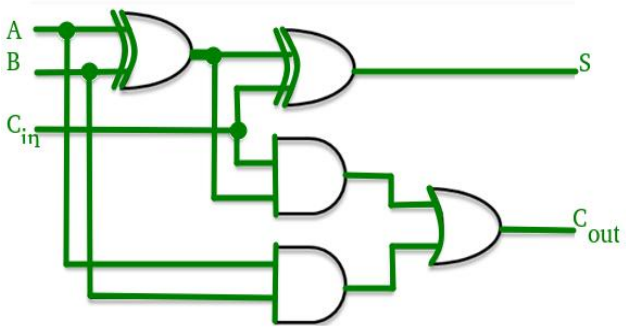

Figure 5. Full adder gate diagram

Table 1. Full Adder Truth Table and conditions

A	B	C	C+1	Condition
0 0 0	0 0 1	0 1 0	0 0 0	No Carry generated
0 1 1	1 0 0	1 0 1	1 0 1	No Carry propagate
1 1	1 1	0 1	1 1	Carry generated

From the above Figure 5 and Table 1 we consider two signals called carry propagate named as P_i and carry generate named as G_i. The expressions for both P_i and G_i are given as

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

The sum and carry output are expressed with the help of carry propagate P_i and carry generate G_i. The sum and carry out equations are given as

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

Where the G_i signal is produced when the both signals A_i and B_i are 1 regardless of the input signal. The propagate signal P_i is generated when the carry

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is from C_i to C_{i+1}. The carry output expressions of the all four blocks in the carry look ahead adder are noted as

$C_1=G_0+P_0C_{in}$

$C_2=G_1+P_1C_1=G_1+P_1G_0+P_1P_0C_{in}$

$C_3=G_2+P_2C_2=G_2+P_2G_1+P_2P_1G_0P_2P_1P_0C_{in}$

$C_4=G_3+P_3C_3=G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0+P_3P_2P_1P_0C_{in}$

In the above equations C_4 does not need to wait the C_3 and C_2 signals instead it is propagating along with the C_3 and C_2 signals. The implementation of the three Boolean functions for every carry output C_2, $C_3$and C_4 for a carry look ahead generator is given as

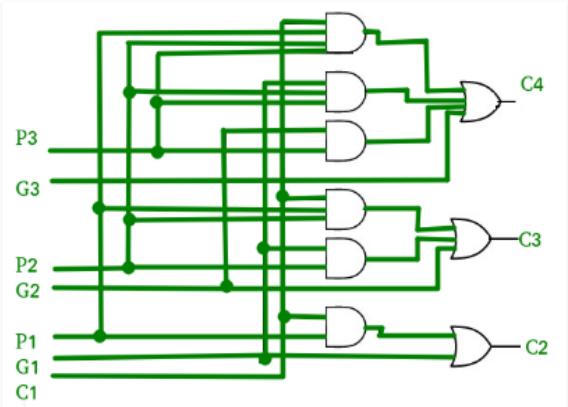

Figure 6. Gate implementation of carry outs C2,C3 and C4

The Figure 6 shows the gate way implementation of the carry out signals C_2,$C_3$and C_4 with the components like AND gate, OR gates with the propagate signals and generate signals as the input signals.

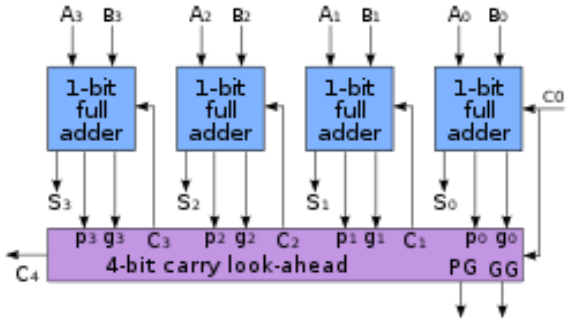

Figure 7. 4-bit carry look ahead adder

The actual block representation of the 4 bit carry look ahead adder with all the input signals and also both the propagate signals and generate signals is shown in the Figure 7.The advantages of carry look ahead adder are that it reduces the propagation delay when compared with other adders and also provides fastest addition logic. The disadvantage of the using CLA is that it occupies more space and circuit gets more complicated when the variables are increased.

IV. Proposed 4-Bit CSA

Carry select adder is a parallel adder which can add two n-bits numbers at a time. Carry select adder is considered as more efficient than carry look ahead adder and also works very fast. Generally a CSA consists of ripple carry adders and multiplexers as shown in the Figure 8. The addition of two bits is carried out with the help of two adders considering both cases, when carry is 0 and when carry is 1. After the calculation is done the correct sum and the correct carry out is selected with the help of the multiplexer when correct carry in is known.

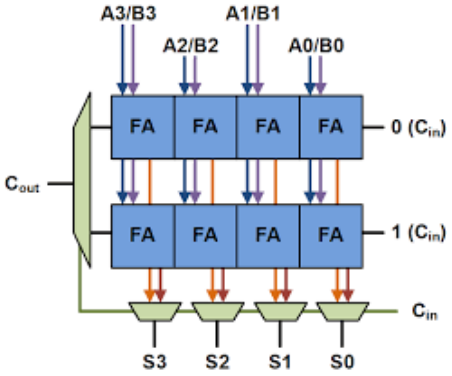

Figure 8. 4-bit carry select adder

The above Figure 8 is the building block of the carry select adder with the size 4. It consists of two 4 bit ripple carry adders and multiplexer. The sum and the carry bits are selected according with the carry in signal. One of the ripple carry adder assumes the carry as 0 and the other one as 1. The adder that has the required assumption which is based on the carry in that result the desired output. There are different sized adders in carry select adders like uniform sized adder, variable sized adder and conditional sum adder.

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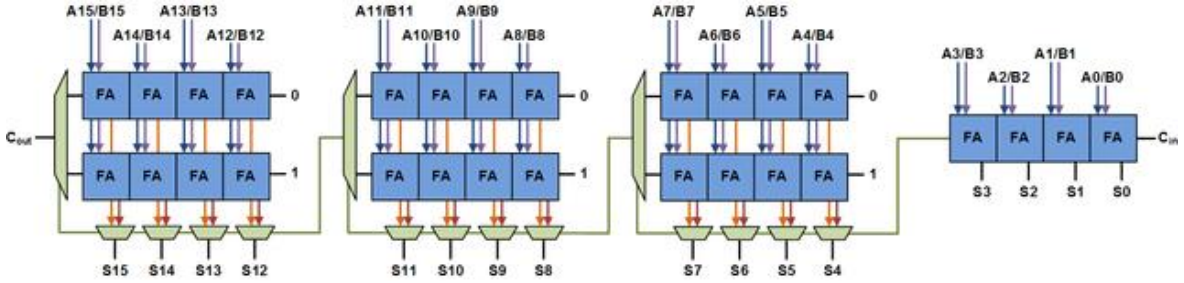


Figure 9. Uniform sized adder of CSA

In uniform sized adder the since the carry is known at the beginning of the computation. The best example for the uniform sized adder is a 16 bit CSA it has four ripple carry adders and 3 multiplexers. The delay is also based on the ripple carry adders and the multiplexers.

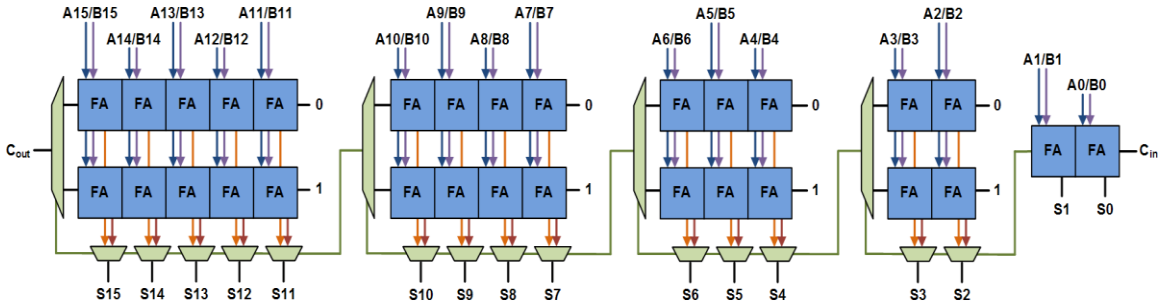
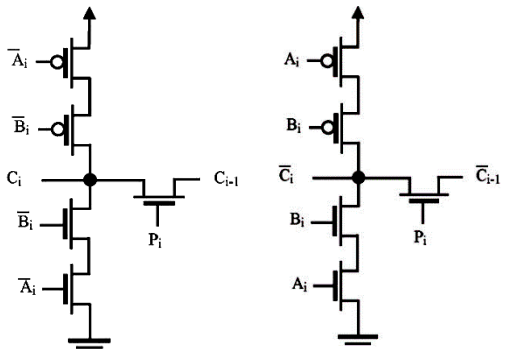


Figure 10. Variable sized adder of CSA

A 16 bit carry select adder is also created with variable sized with less number of adders in the beginning to reduce the delay. The ideal delay is taken when the delay of the full adders is equal to the delay MUX.Based on the carry select adder the conditional sum adder is considered as the recursive structure. The conditional sum adder has high fan-out due to the intermediate outputs produced in the adder.

In the existing method, the CSA is designed using the CLA unit with CMOS technology, select circuit and multi output AND gate. The adders that are used for the implementation of the VLSI are based on the carry look ahead adder which helps to reduce the delay. Those adders are also used to calculate the carries in each parallel stage. The compact look ahead adder and its instant form of the parallel prefix CLA, is the chosen conspire for time-basic applications with an extensive expense as far as silicon region and power dissipation. The CSA gives a tradeoff between a RCA and a CLA adder. Highly specified adders consolidate components of various ways to deal with acquire adders with a better, diminished region and low power utilization.



(a) (b)

Figure 11. Cell generation of C_i and $\overline{C_i}$ [1].

The ripple adder uses three inputs like A_i and B_i also the C_{i-1} from the previous state. The construction of the above Figure 11 includes the pMOS and nMOS transistors of CMOS technology. Consider the both the 11a and 11b figures, the pull up transistors used are the PMOS transistors and the pull down transistors are nMOS transistors. The transistor with inputs like P_i and carry in is also the nMOS transistor. The Figure 11 gives us the information about the effective static CMOS implementation and also the carry outs C_i and $\overline{C_i}$. The signals G_i, P_i, N_i are mutually exclusive [1]. For the implementation

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of the CLA we use the Figure 11b because the noise margin that is produced by 11b is much lesser when compared to the Figure 11a.

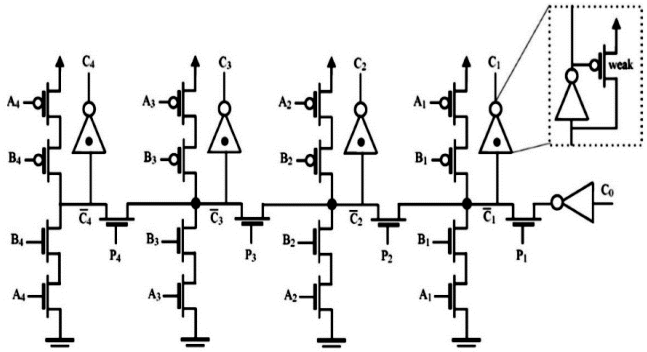

Figure 12. Four bit CLA using the cell 11b [1].

The noise margin that is produced by both the cells in Figure 12 can be reduced with the help of a restoring inverter. The problem is occurred due to the exceeding of the threshold voltage level of the pass transistor (P_i) to the supply voltage. These restoring inverter increases the fan-out and electrical insulation of the cell.The 11b cell is cascaded into 4 stages and the level restoring circuits that i.e. The restoring inverter is placed in the Figure 13 to make a full swing when a high level is transmitted through the pass transistors. Both the P and N transistors should be placed in such a way that they have to balance the rising and falling time. The pMOS transistor is made to be a weak fed back to the inverter.

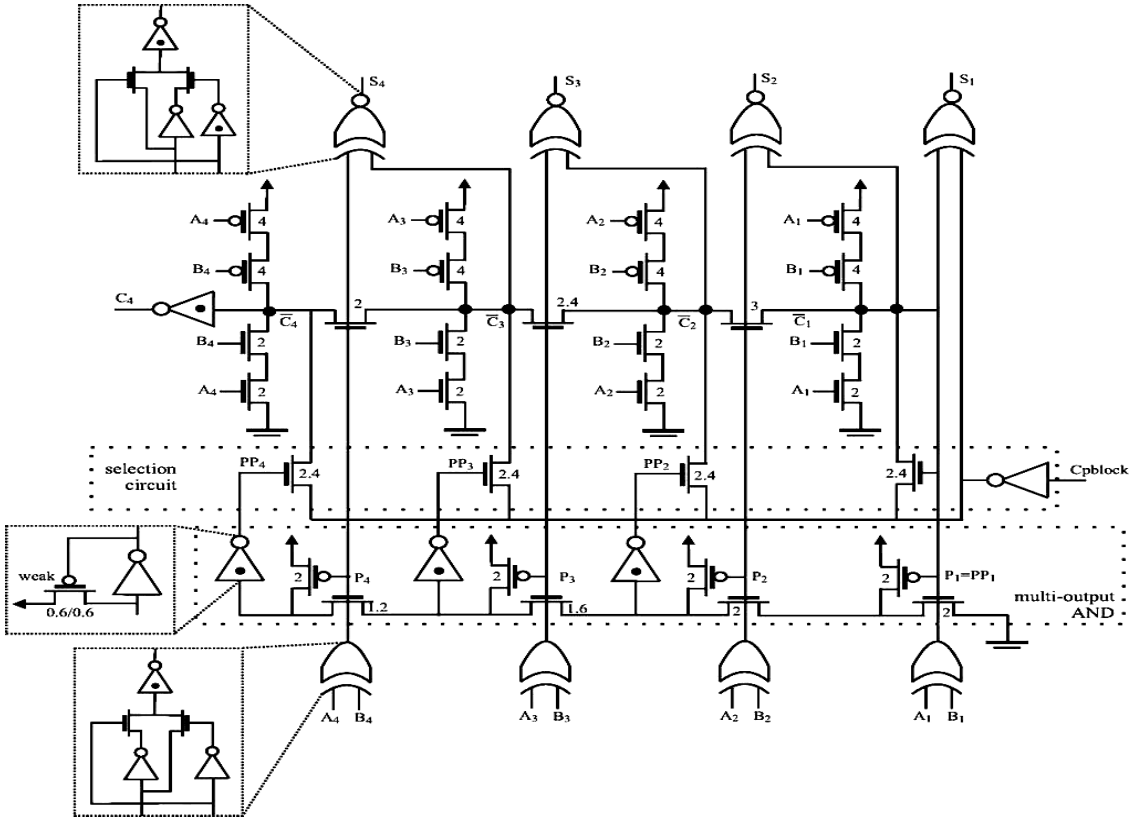

Figure 13. Static and compact 4 bit CSA [1].

The Figure 13 is the actual carry select adder which is designed with the help of compact CLA, select circuit and multi output AND gate. The power and area of the CSA circuit is linked with the carry look ahead adder circuit. Basically the carry select adder is constructed using the 4 bit CLA circuit and with the select circuit for the generation of the PP_i signals. The select circuit is made up of the pass transistors (*Pi*) and similar to the figures in [1]. Since the adder is using the restoring inverters we need to use pass transistors.In this CSA the critical phase is determined with the carry chain of the primary block and also with the select circuit. Many of the researches have conducted on CSA with different bits like 32 bit is provided in [1].

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The carry out is calculated with the help of the following equations,

$C_i = A_iB_i+P_iC_{i-1} = G_i+P_iC_{i-1}$

$$\overline{C_i} = \overline{A_i}\ \overline{B_i} + P_i\overline{C_{i-1}} = N_i + P_i\overline{C_{i-1}}$$

In the above equations,

$G_i = A_iB_i$ and $N_i = \overline{A_i}\ \overline{B_i}$

To know the sum and carry out of the carry select adder we need to use the classical CSA equations that are detailed in [1]. Let the equations be,

$$\overline{C_i} = \overline{C_i^0} + PP_i\overline{C}_{pblock} \text{ and}$$

$$Si = (Pi \oplus \overline{C_i})$$

Table 2. Full adder carry out

A_iB_i	C_i	$\overline{C_i}$	P_i
0 0	0	1	0
0 1	C_{i-1}	$\overline{C}_{i-1}$	1
1 0	C_{i-1}	$\overline{C}_{i-1}$	1
1 1	1	0	0

The above truth table shows us the full adder carry outs and also its complement. From the table 2, when $A_i=B_i=0$ and $A_i=B_i=1$ the carry output is generated at the i^{th} stage and the P_i signal is indicates the previous carry C_{i-1} to pass to the next stage.

The carry select adder is designed using the cadence. For designing the carry select adder first we need to check the CLA circuit in the schematic and verify the outputs with the truth table. When we observe the CLA circuit in the Figure 14 it has a inverter at the foremost right side. The adder has to be checked from right to left along with the carries and input signals. The P transistors used in this designing are p1lvt and N transistor as n1lvt. The output of the inverter is given to the N transistor which already has P1 as the input signal.

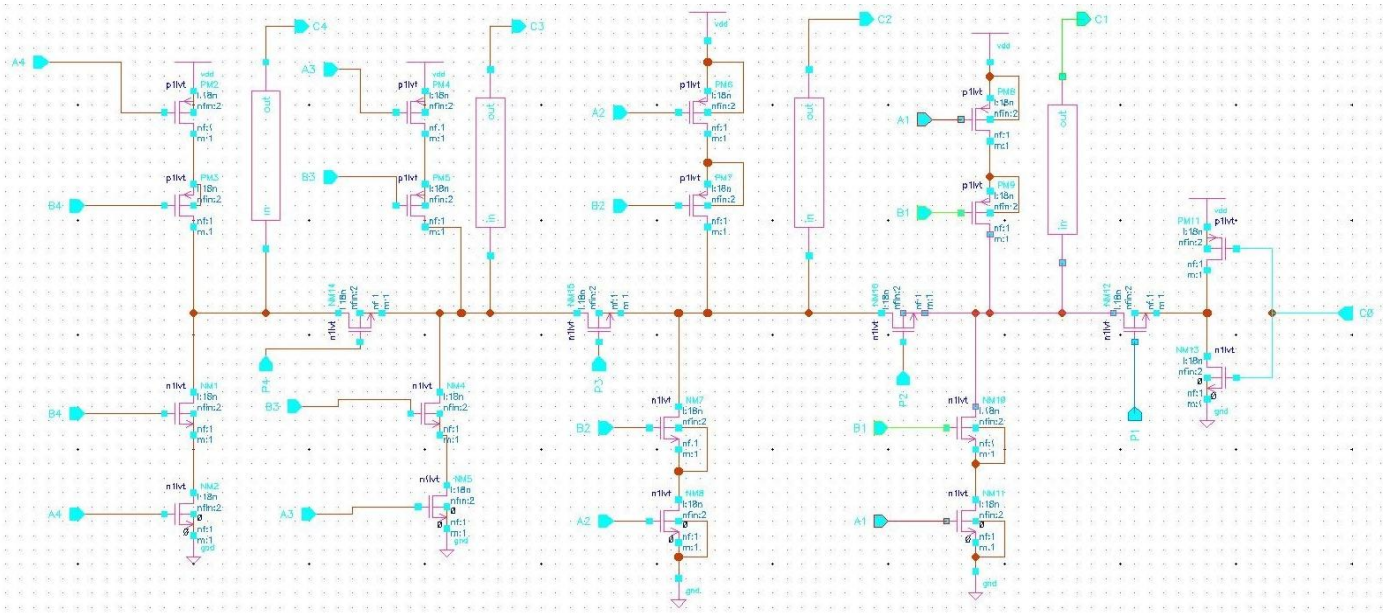

Figure 14. Schematic of CLA

The restoring circuit is made up of the inverter circuit with the weak pMOS transistor. A separate schematic is made for the restoring circuit and converted into a symbol for easy designing and to visible neat and clean in the schematic. Such that all the four blocks are connected in cascade with all the input pins and voltages gives to the inputs and the outputs are collected at the C1, C2, C3 and C4 pins. Every individual block has its own inputs and pins. After connecting all the required components we

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need to save and run the schematic with the prescribed steps. We need to select the input pins, output pins from the schematic and run it. The output waveforms are observed based on the voltages given to the input pins. The voltage that we have given is 0.1V.

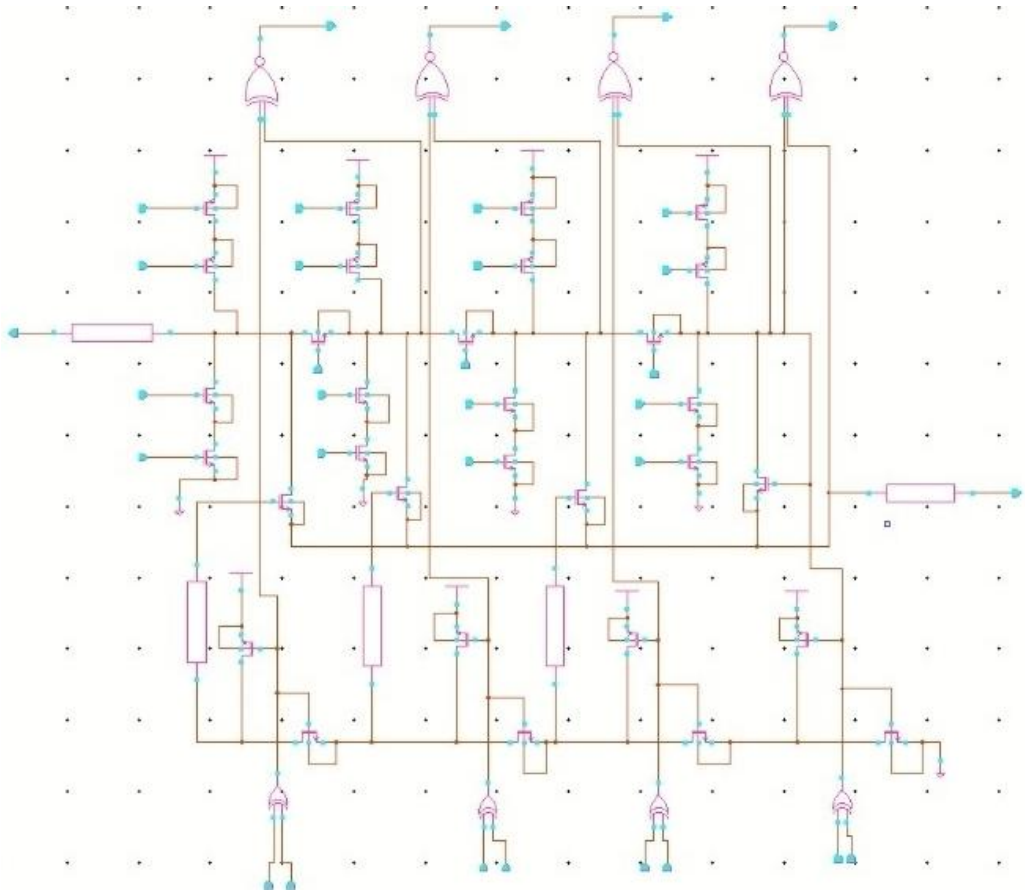

Figure 12. Schematic of CSA

The Figure 12 is the schematic of the carry select adder which is seen the Figure 13. All the sub-circuits like XOR, XNOR gates and the restoring level circuit are made in a separate schematic and used as the symbols in the main circuit. The XOR gate is consists of one level restoring circuit, two inverters and two N transistors. The XNOR gate is made up of two level restoring circuits, one inverter and two P transistors.

The select circuit is composed of one inverter and four N transistors. The section is seen below the CLA circuit. The multi output AND gate is having three restoring level circuits and four P transistors. All the inputs like Ai and Bi are given as inputs to the XOR gates and the output of those gates are given as input to the XNOR gates. The propagate signal Pi is also connect to the output of the XOR gates. The carry outs are collected at the CLA section and the sum signals S_1, S_2, $S_3$and S_4 are collected at the outputs of the XNOR gates. The VDD signal which is inbuilt with specified voltage is given to the pull up transistors and the pull down transistors are ground, respectively.

V. Simulation Results and Experimental Findings of the Proposed Work

From the existing method, the carry select adder is designed using the FinFET technology with the cadence tool. The transistors that are present in FinFET technology are used in place of PMOS and NMOS transistors. When compared with CMOS technology, the FinFET devices have greater faster switching times. The carry select adder is designed in the schematic form with the software. The specifications that are used for designing is different

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from the CMOS and provides accurate and fast outputs.

4.1 Simulation Results of 4-bit CSA

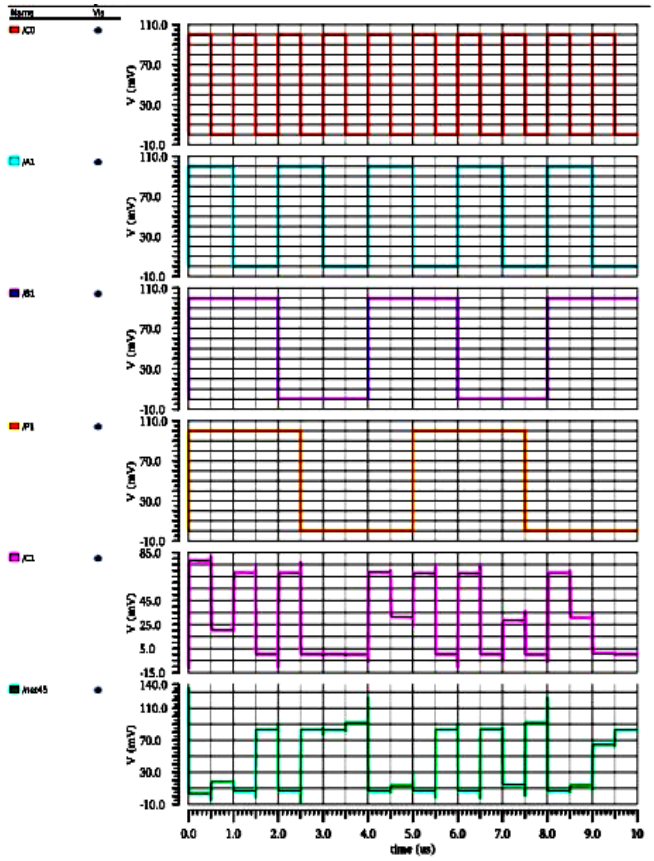

Figure 13: Output waveform of one cell CLA

The above waveform is obtained with one cell of the CLA circuit with the inverter output as the input given to it. From the waveform the C_0 signal is the main input, A_1 and B_1 are the inputs given to both P and N transistors, P_1 is the propagate signal which is the ex-or operation of both the A_1 and B_1 signals.

C_1 is the output signal that is the carry out signal obtained by the impact of the pass transistor also. The signal that is passing from the first block will be complimented based on the signal receiving the restoring circuit.

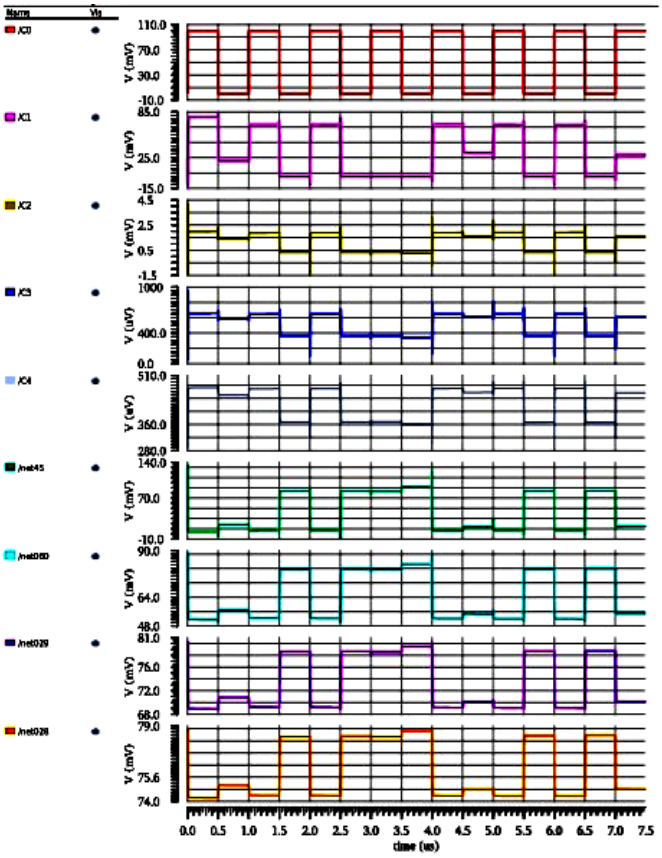

Figure 14: Output waveform of one cell CLA

The output waveform of the carry look ahead adder is seen in the Figure 14. All the outputs are compared with the C_0 signal which is the main input signal. The last four waveforms show the graphs that are obtained near the nodes of the each block.

VI. Conclusion

The carry select adder which is designed in this paper is very suitable for the implementation of the VLSI circuits. The optimized delay power among the adders, power consumption and also reducing the transistors is carried out. The overall objective of the project is to construct a static and compact carry select adder which can be implemented in further purposes. The FinFET technology used in this project is very much advanced with sophisticated specifications. This technology takes use of the cadence tool that is used in the present day of VLSI designing. The thesis not only gives us the information about the adders but also about the usage of the software and it working process for designing. It is inferred that FinFETs are incredibly

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quick and force effective gadgets, as gadget measurement is downsized to littler innovation, its drive current is extremely enormous in contrast with spillage current that implies proportion of on to off current is exceptionally huge. We can use this adder in various applications and speed up the devices with different specifications.

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