TEST Engineering & Management

May – June 2020
ISSN: 0193-4120 Page No. 2141 - 2145

Architectures and limitations of Wide Area Synchro-phasor Measurement device: A Review

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Article Info
Volume 83
Page Number: 2141 - 2145
Publication Issue:
May - June 2020

Article History
Article Received*: 11August 2019*
Revised*: 18November 2019*
Accepted*: 23January 2020*
Publication*: 10 May2020*

Abstract:

The wide-area synchronized measurements is now having attention for the researchers to monitor the power quality while integrating the renewable energy sources with the grid. To monitor the power quality more accurately phasor measurement units are used in which the sensor that detects the frequency is called the phasor measurement device (PMD). This paper gives the brief overview on the architectures and limitations of PMD. This PMD device is synchronized with GPS and internet to give the accurate results.

Keywords: *Phasor measurement device, generations of frequency disturbance recorder (FDR), Power Quality.*

I. INTRODUCTION

Overall the world renewable energy is getting attention for the researchers. The Gigawatts renewable power sources has new parameters that needs to be discussed as the conventional power sources. High power renewable energy sources requireadevotionfor machinists and designers [1-3]. Outputs of renewable energy sourcesare unpredictabledue to weather condition as compared to conventional generation as conventional power generation uses fossils fuels and uses the available natural resources. Renewable energy sources dynamics acquires some challenges that aremultifaceted and demand more requirements to simulate the awareness of power grids in real-time [4].Due to the low inertia, the increment in renewable energy sources will propagate the electromechanical wave faster. Furthermore, the irregular distribution for the renewable sources can consequence in irregular distribution, moreover it adds the dissimilarity in the distribution of electromechanical wave propagation speed [5]. The dissimilar wave propagation speeds in power grids will harm the accuracy to locate the disturbances.Microgrids are having the common configurations at the load end to integrate renewables accurately and make it higher reliable and more flexible.

Though, it is difficult to collect the information of the microgrids in real-time at the load end and turns out to be a blind zone for the distribution system operators [6]. A significant tool to get the situational awareness is the synchro-phasor measurement device. It sends the data which is timely synchronized with GPS [7]. An important technology, FNET/GridEye is a wide area monitoring system that is deployed throughout the world.

Wide area monitoring system is comparatively a new tool to get the awareness of power system, it also provides real time grid status that is synchronized with GPS [8,9]. As it gives unique visions into dynamics of power system, wide area monitoring system is improving the awareness for power system operators while in the framework of smart grid. Initially in 2003, the frequency monitoring network is a wide area phasor

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measurement system which covers a nation-level power grid [10-12]. It uses highly accurate and low-cost frequency disturbance recorder to collect the frequency, voltage, phase angle, voltage magnitude in power grid and an updated data storage center that is called phasor data concentrator to store, receive and process all the measurements.

Because of the increasingly multipart behavior displayed by huge power systems, wide area monitoring system has been used to overcome the conventional supervisory control and data acquisition to improve the awareness of any situation [13-16]. While synchronizing the time with GPS to measure the high time-resolution grid status, it can tell the dynamics for the power system that is not apprehended before. Especially due to uncertainties in renewables that transfers to the grid, wide area monitoring system is more important tool for future renewable energy sources.

Sensors that are installed at the distribution grid consist of a network, called the frequency monitoring network (FNET) also known as GridEYE, can measure voltage magnitude, voltage phase angle and voltage magnitude, etc. Based on monitoring the power quality, numerous applications have been developed and are operating for real-time power grid awareness. Furthermore, various new applications are being tested to improve the awareness and reliability of power grids which are having high level saturation. Section II gives the background of synchro-phasor measurement device. Section III presents the limitations of the synchro-phasor measurement device and section IV is the conclusion.

II. BACKGROUND OF SYNCHRO PHASOR MEASUREMENT DEVICE

Mostly used methods for real-time and embedded systems is the top-down approach this is the natural way to approach a complex design especially it relies on multi levels of abstraction to fix those concepts that are independent. These design approaches are very significant for the next generation phasor measurement device designs because all these are being distinguished from many years.

Like the Phasor Measurement Device (PMD) design primarily focus on portability and comfortability of deployment, the PMD is composed of four important sections as shown in fig. 1. It includes the input system in analog form, processor, network communication subsystem and timing subsystem. The input system where the signal is analog consist of analog to digital converter (ADC), signal acclimatizing system and transformer. The timing for the synchro-phasor measurement device must be proficient of producing variable frequency pulses that are synchronized to UTC time for activating ADC to convert.

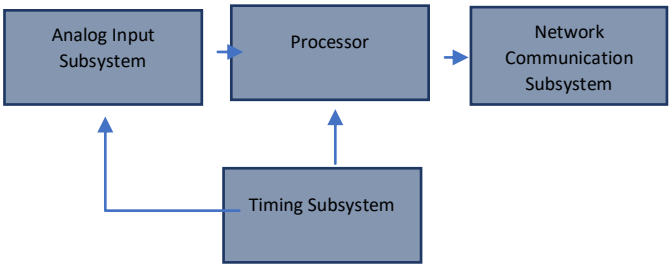

Fig. 1 System Block Diagram of Phasor Measurement Device

The important goals of the synchro-phasor measurement device are the ease of deployment and portability. Embedded System is the clear choice for the design and it has the model for the first and second generation of SMD design.

A. Analog Input Subsystem

The heart of the analog input subsystem is the analog to digital converter. There are a lot of ADC available now. However, the mostly used ADC architectures are the ADC [17], Flash ADC [18], Successive Approximation Register ADC [19], Sigma Delta ADC [20], Pipelined ADC [21]. Total of five architectures have a difference in algorithm designing and encoding method, But the characteristic of PMD are the characteristics of each ADC like speed of conversion, resolution, size and price. Although the relationship between such factors and phasor estimation accuracy is complex.

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Generally, SAR ADC is very much used for almost all the data acquisition system as well as in instrumentation applications. Because of easy use of interfacing and integration, it is being used in both generation of PMD [17]. Ideal techniques to measure the industrial applications are the sigma delta ADCs and integrating ADCs. As compared to other ADC architectures, the integrating ADC has a low speed with typical conversion speed of 20ms [20,21]. The sigma delta converter controls in voiceband and audio markets. The need for the ADC filter has been lower by the oversampling process in theses ADCs. However, the sigma delta converter has many disadvantages. First the attenuation at the harmonics side is not provided by this filter. Also, the conversion speed and filteringgivethe long latency sandwiched between the first digital output and first sampling cycle [21].

TABLE I. ADC ARCHITECTURES AND ATTRIBUTES

ADC types	Flash	SAR	Integrating	Pipelined	Sigma Delta
Method	Cascaded Comparator	Binary Search	Integration and comparator	Parallel Comparators	Modulator and filter
Encoding	Thermometer code	Successive approximation	Analog integration	Digital correction	Oversampling decimation filter
Conversion time	Constant with increase in resolution	Increase linearly with resolution	Constant with increase in resolution	Increase linearly with resolution	Tradeoff between data output rate and resolution
Resolution	Limited to 8	8 to 18	10 to 18	8 to 16	12 to 24
Size	Increases exponentially with resolution	Increase linearly with resolution	Constant with increase in resolution	Increase linearly with resolution	Constant with increase in resolution

The high-speed ADCs are pipelined ADCs and Flash ADCs. To convert the signals having the large bandwidths at high speed, flash ADCs gives the better result. Although it has low resolution and it consumes more power and that can be expensive as compared to others [20]. Sampling rates ranges between 5Msps and 100sMsps is required for pipelines ADCs. It also consumes less power as compared to Flash ADC. At last the above table 1 summarizes few of the characteristics of the commonly used ADC architectures [17-21].

B. Central Processing Unit

Central processing unit in PMD can change by a high change and more improvements in digital processor technologies. Yet there are various parameters that need to be focused while selecting the processor. The quick measurement is to decide either the fixed point or a floating-point processor is required. Main difference in these two are numeric representation of data. Whereas the fixed-point hardware performs strictly arithmetic, floating point hardware either integer or real arithmetic. For high data applications like telecom and voice the fixed-point processors are preferred. However, the implantation of fixed point in software is required for this type of processor [18
]. It
still the cost effective as compared to the floating-point processor.

III. LIMITATIONS OF PHASOR MEASUREMENT DEVICE (PMD)

As few improvements have been made over the years since the first generation of PMD, there are limitations to the second generation of PMD design. Significantly the problem related to the time for the subsystem and the capacity of the processing is making the need for the new development. There are few limitations in first and second that is needing to be resolved in the next generation of PMD.

A. Timing Subsystem Limitations

To make the phasor measurement more accurate the timing subsystem of all the generations of PMD is one of the fundamental limitations. This problem is related to the process in which every second divide into 1440 individual time periods. As the 1440 activate to convert the signals are being driven by the PWM module. Accuracy of the clock division and conversion signals are driven by the processor. Before the second-generation number of clock cycles between the last two 1PPS has been divided to find the sample

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period. Problem to this method has to do with the remainder that is ignored after the integer division operation. Furthermore, because of inevitable variation in the clock, a change of up to 100 clock cycles per second. It also translates to be 100PPM because it usually quantified by manufacturers.

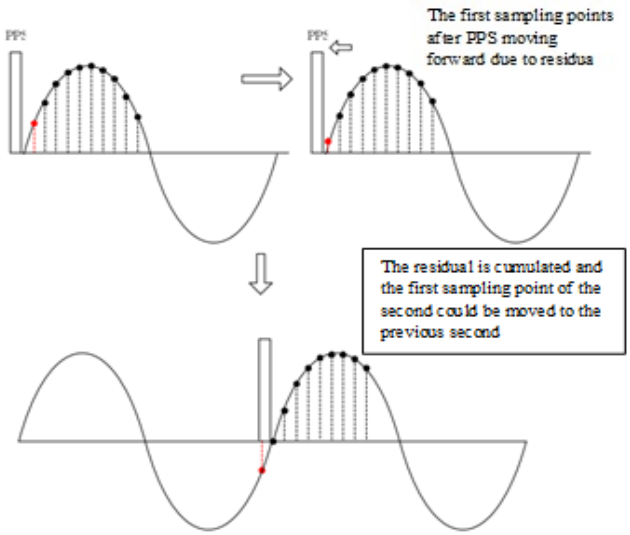

Fig. 2Effect of sampling point residues

While implementing in the software regarding the timing subsystems limitations the integer part of clock cycles is castoff. By translating towards time domain 1280 cycles is equal to sixty-four microseconds on the clock of 20MHz. These figures may seem like unimportant, but residue gathers every second leading to snowball effect. In fig. 2 this phenomenon where the first sampling point after one pulse per second to move to the last second. As the algorithm which uses 1440 sampling point to estimate the phasor calculation, another free sampling point is consequently rejected [14].

B. Computational Limitations

The second generation PMD has been improved in the
architecture but not having the increase in computation power. Additionally, it divides the computational part into two individual processors as compared to first generation PMD that uses only single processor for all the computation. The generation II PMD was very high cost and the portability issue.

C. Limitations on Voltage Level

The another more important factor is the voltage level issue, as it was made in United States therefore it only accepts 60Hz with a voltage level of 120, Since the research is for the whole world and researchers from different countries want to implement it therefore, it must be capable of operating at 240V to make it more feasible.

IV. CONCLUSION

As the timing of the sampling pulses is related to frequency and phasor angle measurement, this paper highlights matter of timing from various perspectives. High sensitivity implementation has been done for synchronized frequency and phasor estimation algorithm. Whatever the architecture of PMD used either embedded system or PC based design or a combination of both the timing analysis presented in this paper can be improved for the next generation PMD.

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