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Power Efficient Control Unit for Green Communication.

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Article Info
Volume 83
Page Number: 13422 - 13427
Publication Issue:
March - April 2020

Article History
Article Received*: 24 July 2019*
Revised*: 12 September 2019*
Accepted*: 15 February 2020*
Publication*: 20 April 2020*

Abstract
Nowadays people are getting more concerned towards the idea of green communication. In electronic world as digitalization is growing the need of power efficient devices are in more demand. In this work we are making a power efficient Control Unit (CU) by interfacing it with different Virtex and Spartan family Field Programmable Gate Array (FPGA). This experiment is performed on Xilinx 14.1 ISE Design simulator. Dynamic power, quiescent power and total power of control unit with different FPGAs of Virtex and Spartan families is analysed on X Power analyser tool. The other on chips power like clock power, signal power, input/output (I/O) power counts 0W of power in total power consumption. From the experiment it was concluded that control unit when interfaced with Spartan 6 FPGA consumes least amount of power and hence regarded as most power efficient device.

Keywords—Control Unit, FPGA, Virtex, Spartan, Power.

I. INTRODUCTION

Nowadays attention towards green communication technologies are getting more concern in people's mind [1]. Everyone is looking for those devices and products which are energy or power efficient. The field of communication network also needs to be formulated with green communication [2] technologies so in order to fulfil the challenges of communication field towards green communication, in this work a power efficient control unit is implemented on different FPGAs. The different FPGAs with which CU is interfaced is shown in figure 1.

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Figure 1. Different FPGA with which CU is interfaced.

Central Processing Unit (CPU) comprises of a vast number of electronic components and devices and control unit is one of the major part of CPU [3]. The working of CU is to direct the operation of processor which is described in figure 2.

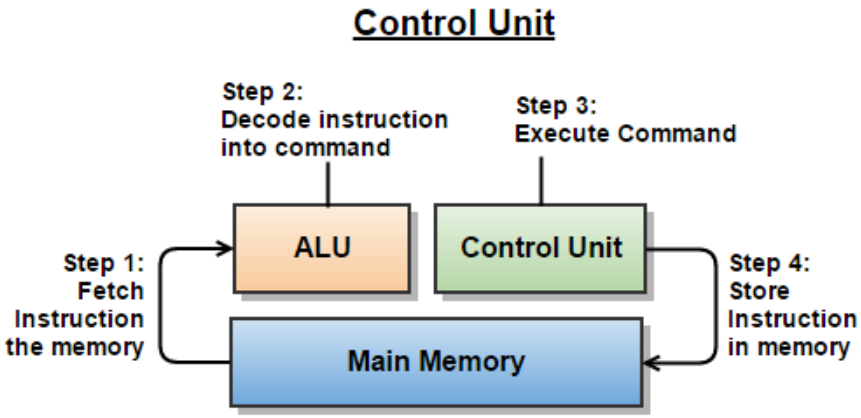

Figure 2. Working of Control Unit.

One of the major responsibilities of CU is to tell computer's memory to decide how to respond to data instruction set which is sent to the processor of CPU. The schematic of CU designed by Xilinx simulator is shown in figure 3.

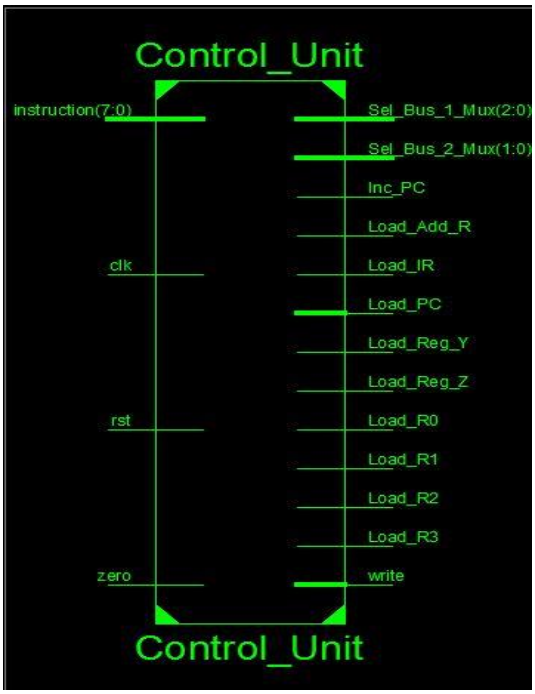

Figure 3. Schematic of Control Unit.

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The instruction signal processing process of CU is represented in figure 4.

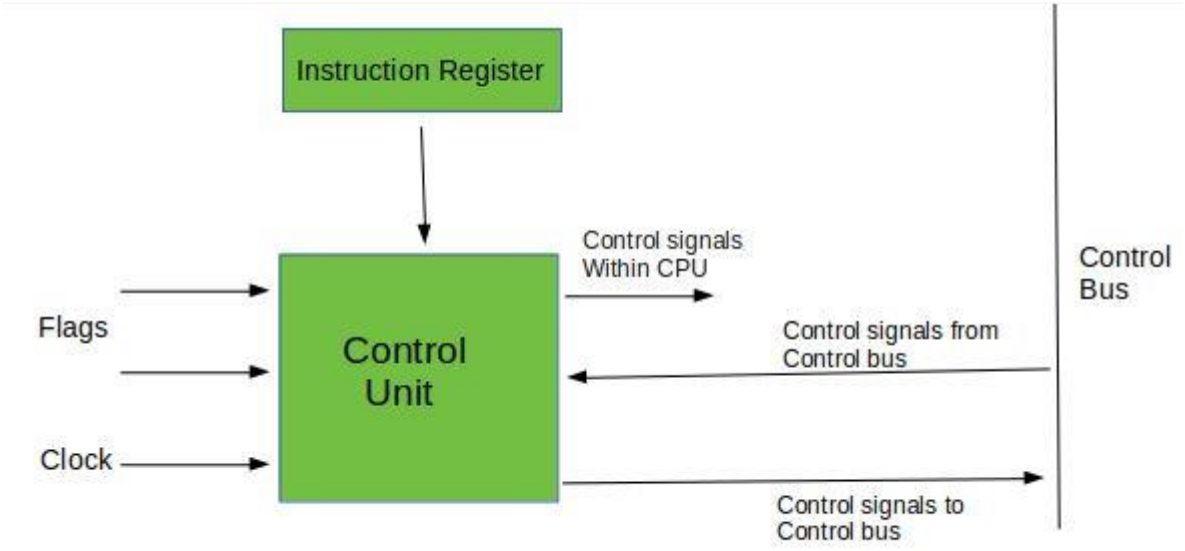

Figure 4. Signal processing of CU.

II. RELATED WORK

P. Diniz et. al. [4] designed FPGA based automatic synthesis data storage and control structure for computing engine. W. M. El- Medany et. al. [5] implemented GSM based remote sensing and control system using FPGA for home security. M. Majzoobi et. al. [6] used Virtex 5 FPGA to design FPGA based true number generator using circuit metastability and adaptive feedback control. E. Koutroulis et. al. [7] developed photovoltaic modules for real time simulation using FPGA. K. K. Shyu et. al. [8] designed FPGA based brain computer interface control hospital bed nursing system. B. Pandey et. al. [9] implemented Arithmetic Logic Unit (ALU) design on FPGA by changing frequency values. S. Gdaim et. al. [10] implemented DTC induction machine based fuzzy control on FPGA.

III. EXPERIMENTAL SETUP

The interfacing of CU with Virtex 4, Virtex 5, Virtex 6, Spartan 3 and Spartan 6 is done on Xilinx 14.1 ISE Design simulator and power observation is analysed using X Power analyser tool. For Virtex family FPGA the ambient temperature of environment is 50(^{o}C) and 25(^{o}C) for Spartan family FPGA. The code of CU is written in Verilog Hardware Description Language (HDL).

IV. POWER ANALYSIS

A. Power Analysis of Virtex 4, Virtex 5 and Virtex 6 FPGA.

The supply power of Virtex 4 is displayed in table 1. For Virtex 4 dynamic power, quiescent power and total power is calculated as 0.004W, 0.165W and 0.169W respectively.

Table 1. Supply Power of Virtex 4 FPGA.

Supply Power (W)	
Dynamic Power	0.004
Quiescent Power	0.165

Total Power	0.169

The dynamic power of Virtex 5 is 0.000W, quiescent power and total power are 0.379W. The supply power analysis is shown in table 2.

Table 2. Supply Power of Virtex 5 FPGA.

Supply Power (W)	
Dynamic Power	0.000
Quiescent Power	0.379
Total Power	0.379

For Virtex 6 FPGA quiescent power and total power are 0.756W and dynamic power is 0.000W which is shown in table 3.

Table 3. Supply Power of Virtex 6 FPGA.

Supply Power (W)	
Dynamic Power	0.000
Quiescent Power	0.756
Total Power	0.756

The total power comparison of Virtex 4, Virtex 5 and Virtex 6 FPGA is presented in figure 5.

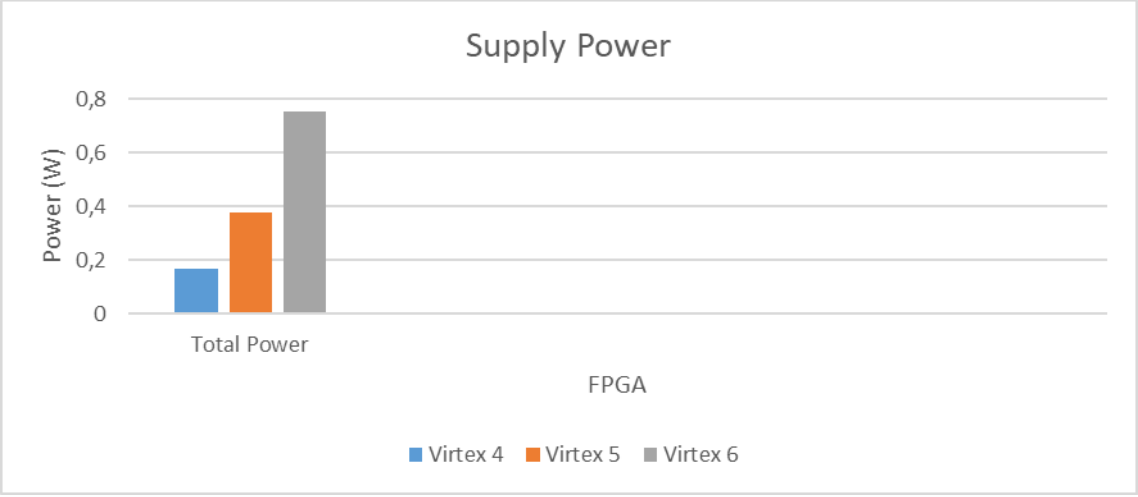

Figure 5. Power Comparison of Virtex 4, Virtex 5 and Virtex 6 FPGA.

B. Power Analysis of Spartan 3 and Spartan 6 FPGA.

For Spartan 3 and Spartan 6 FPGA dynamic power consumption is 0.000W. For Spartan 3 FPGA the quiescent power and total power are 0.027W and for Spartan 6 FPGA quiescent power and total power are 0.014W. The supply power of Spartan 3 and Spartan 6 FPGA is demonstrated in table 4 and table 5 respectively.

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Table 4. Supply Power of Spartan 3 FPGA.

Supply Power (W)	
Dynamic Power	0.000
Quiescent Power	0.027
Total Power	0.027

Table 5. Supply Power of Spartan 6 FPGA.

Supply Power (W)	
Dynamic Power	0.000
Quiescent Power	0.014
Total Power	0.014

V. RESULTS ANALYSIS

On comparing the supply power of all the above mentioned FPGAs it was concluded that Spartan 6 is most power efficient device when interfaced with CU. The percentage of total power variation of Spartan 6 with Virtex 4, Virtex 5, Virtex 6 and Spartan 3 is given as 91.75%, 96.30%, 98.14% and 48.14% respectively. Also it is concludes that Virtex 6 FPGA is the worst FPGA device for interfacing CU. The total power comparison is described in figure 6.

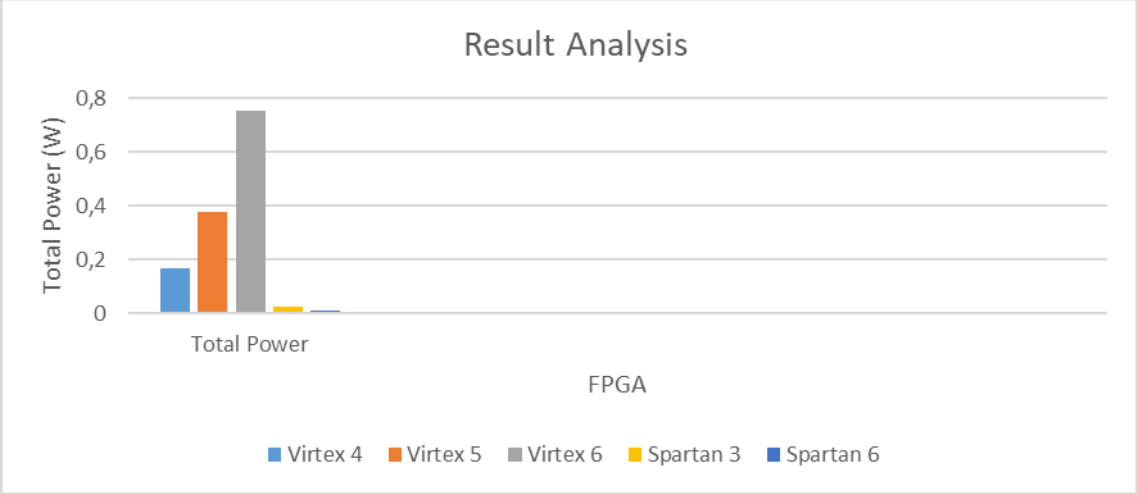

Figure 6. Power Comparison of Virtex 4, Virtex 5, Virtex 6, Spartan 3 and Spartan 6 FPGA.

VI. CONCLUSION

This paper makes the comparative analysis of interfacing CU with Virtex 4, Virtex 5, Virtex 6, Spartan 3 and Spartan 6 FPGA. And this analysis gives the clear direction to the users and researchers that Spartan 6 is most power efficient FPGA and Virtex 6 is the worst FPGA for interfacing CU.

VII. FUTURE SCOPE

In this paper the interfacing of CU is done with Virtex 4, Virtex 5, Virtex 6, Spartan 3 and Spartan 6 FPGA, but we can also perform this experiment with other FPGAs like Cyclone FPGA, Airtix FPGA, and Kintex FPGA etc. Researchers can also design the CU at different values of voltage, current and frequency that will

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help in promoting green communication. Not only can this researchers implement other electronic devices with FPGA for the welfare of society by giving valuable results towards green communication.

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