March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

Design and Implementation of Low Phase Noise, Wideband Clock Source for High Speed Data Converters

Sk Anusha[1] M.Krupa Swaroopa Rani[2], K.M.V.Prasad[3]

[1,2] Digital Electronics and Communication Systems, [3]Electronics and Communication Engineering (ECE)
[1, 2] Sri Padmavathi Mahila Viswavidyalayam. Tirupathi, [3] Sri Venkateswara University College of Engineering (SVUCE) SV University (SVU), Tirupathi.

Article Info
Volume 83
Page Number: 7394 - 7402
Publication Issue:
March - April 2020

Article History
Article Received*: 24 July 2019*
Revised*: 12 September 2019*
Accepted*: 15 February 2020*
Publication*: 07 April 2020*

Abstract

Noise is the main parameter in the Phase locked loop (PLL). The main purpose of this paper is to design and implementation of integrated VCO frequency synthesizer that achieves less noise, wideband and extremely low spurious performance using the HMC830LP6GE Fractional-N- Phased-Locked-Loop (PLL). HMC830 attributes an Integrated voltage controlled oscillator (VCO) with a necessary range of Frequency from 1.5 GHz - 3 GHz, and the divider of Integrated VCO output (divide by 1/2/4/6.../60/62), that a mutually permits the HMC830LP6GE to produce the range of Frequencies from 25MHz - 3GHz. The Integrated phase detector (PD) and Delta-Sigma modulators are having the ability of working up to 100 MHz; allow bandwidths of Wider Loop with good spectral achievement.

Index Terms; *PLL, VCO, Integrated phase detector, Serial Peripheral Interface (SPI), delta-sigma modulator, Phase noise, Spurious, HMC830*

I. INTRODUCTION

Phase noise is the critical performance parameter. The main goal of this N-Fractional phased Locked Loop with Integrated VCO is to reduce the phase noise, spurious-level performance of the given frequency with the levels of reasonable power consumption. Manufacturing leading noise of phase and spurious performances are the main features of this HMC830.Across all frequencies that support it to improve sensitivity of the receiver and spectral purity of the transmitter. This HMC830 is the best basis for a different type of applications -such as Local oscillator for RF Mixers, a Clock Source for High Speed Data Converters etc... And also it generate output of frequencies with 0Hz frequency error i.e., is where our work will be most concentrated and will result in this being a unique project. SPI is generally used the serial protocols for low/medium data transmissions for both inter chip and intra chip. SPI is a data bus of „synchronous", which means that can be uses individual lines for data and clock, which has both sides with correct sync. The PLL register will be configured through SPI protocol, that designing code is developed in VHDL using Xilinx ISE 14.7.

II. METHODOLOGY

The HMC830 is a less noise, wideband, Fractional-N- Phased-Locked-Loop, that attributes an Integrated VCO with a necessary range of Frequency from 1.5GHz - 3GHz, and the divider of Integrated VCO Output (divide by 1/2/4/6.../60/62), that a mutually permits the HMC830LP6GE to produce the range of Frequencies from 25MHz - 3 GHz. The Integrated phase detector (PD) and Delta-Sigma modulators are adept of working up to 100MHz of the wider loop band width with excellent spectral achievement. The functional figure of the Wide Band Fractional-N- Phased-

Published by: The Mattingley Publishing Co., Inc.

March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

Locked-Loop with integrated VCO is shown below figure 1.

In this, Charge pump and Phase Detector linearity‟s are most important when functioning in the mode of fractional. The phase noise, spurious performances are degraded by any non-linearity. The reference signal and the VCO Divider signals are attainable at the same time, when we define zero phase error. The linearity of Phase Detector is degraded, when the Phase Error is very less and when the Random Phase Errors are causes the Phase Detector to switch back among VCO main and reference main.

By the operating of Phase Detector with an Offset current such that either reference or VCO always leads, then this Switching non-linearity in fractional mode is removed

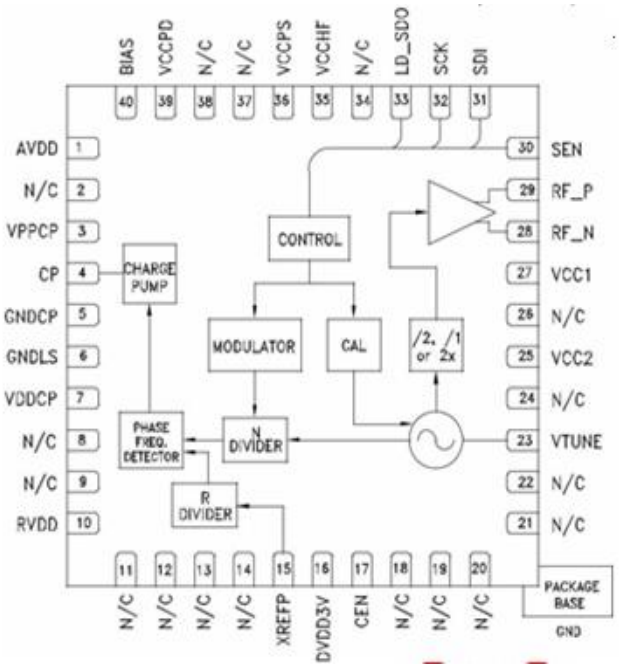

Figure (1): Functional diagram of N-Fractional PLL with integrated VCO

A. Integrated VCO sub system

VCO subsystem types are using the Step Tuned type VCO. The simple Step Tuned VCO is displayed in below figure: a;

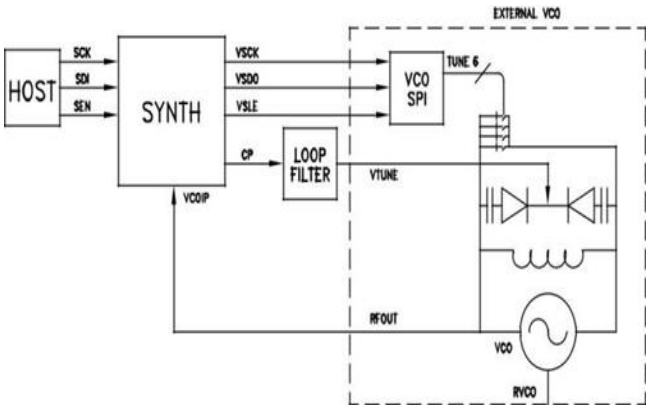

Figure (2): Simple Step Tuned VCO

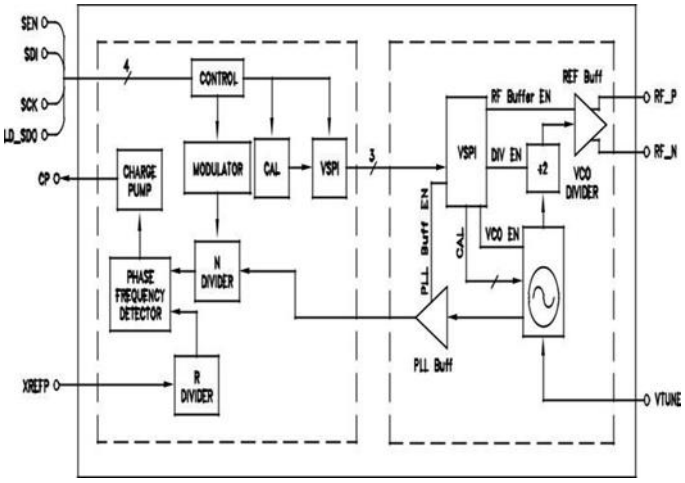

Figure (3): PLL with Integrated VCO

A Step Tuned VCO is with digitally selectable Capacitor Bank permitting the VCO normal Frequency to be attuned by Switching in or out of the VCO Capacitors. The further details of the configuration of characteristic VCO are shown figure:

b. The Step Tuned VCO permits the middle of the VCO on the essential Frequency to user whereas putting the varactor Tuning optimized voltage adjacent the mid Voltage Tuning theme of the phase-Locked -Loop with Integrated VCO charge pump.

The charge pump enables the phase locked loop Charge Pump to tune the voltage control oscillator ended the whole series of functioning with together a less sensitivity tuning and less voltage tuning.

By the using of Auto calibration feature, the

Published by: The Mattingley Publishing Co., Inc.

March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

Switches of VCO‟s are usually measured spontaneously by the using of PLL with Integrated VCO. In the interior state machine, the auto calibration will be implemented. It will be achieves the section of the VCO Sub band while the new Frequency is automated (Programmed).

B. Register Mapping

The Serial Port of VCO has the ability to connect with several Subsystems of inside IC. Every subsystem has various registers to switch the function i.e., Internal to the subsystem. Hence, each register has addresses bits of the internal register. The register mapping of the PLL is shown below.

- **Reg 00h ID Register:**

This Register Value is denoted the PLL ID for the HMC830 and wideband (PLL+VCO‟S).

- **Reg 01 enables Register:**

In this register value can be set by default. When the SPI‟s PLL is enabled, the default value set as 1, and another 9 bits are disabled.

- **Reg 02h RF DIV Register:**

These reference divider register „R" value is used in the calculation of "f_{vco}".

$$f_{vco} = \frac{fxtal}{R} [N_{int} + N_{frac}] = f_{int} + f_{frac}$$

- **Reg 05h VCO SPI Register:**

Reg05h is a superior register uses for secondary addressing of the Subsystem of VCO. To the subsystem of VCO, Writes the Reg05h. Those are automatically forwarded by the VCO SPI state machine controller.

It's not possibility to read the complete contents of the Subsystem of VCO. Simply the last content of the transferred Subsystem of VCO can be read.

Once VCO register programming has been completed, Reg05h needs to be programmed to 0 for Wideband devices or 5 for Narrowband and Tri-band devices. More accurately, only the lesser 7 bits can be needed to be set. The other bits can be set as needed:

xxxx xxxx xxxx xxxx x000 0000 for Wideband devices;

The packet data can be Written into Register 05h is Sub-divided by logic at the Subsystem of VCO will be divided into the 3 parts: The first 3 bits [2:0] are denoted the ID of the VCO subsystem. It can be either 101b/000b, that value can be based on the product. The next 4 bits are denoted te address of the internal register of the VCO subsystem. Then the remaining 9 bits are denotes the data of VCO subsystem, that data fields written into the VCO subsystem.

- **Reg 06h SD CFG:**

Fixed the Delta-Sigma modulator to work in Integer Mode, set the kernel rate, and configure the Delta sigma modulator clock scheme.

- **Reg 07h Lock Detect Register:**

In this Lock Detect Register, the amount of repeated amounts of divided VCO will be sets, this must be inside the Lock Detect

Window to state LOCK. In this Lock detector timer will be sets by the depending on the window type.

- *Reg 08h Analog EN Register:*

This Analog Enable Register is set by default value, i.e., C1BEFFh with the length of 24 bits. In this VCO buffer and prescaler biases are enabled and the pin LD_SDO will be disabled.

- **Reg 09h Charge Pump Register:** Reg 09h = Charge Pump register 2.54 mA CP current with 0 CP offset - Integer mode.

- *Reg 0Ah VCO Auto Cal Configuration:*

VCO auto Cal config - HMC830 is set by default value. This Register length is 17bits.In these bits

Published by: The Mattingley Publishing Co., Inc.

March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

Vtune resolution „R" divider cycles divide with 64 and in these wideband, the SAR bits are not used.

- *Reg 0Bh PD Register:*

This PD Register can be as default with the length of 24 bits. In this the cycle slip prevention will be disabled and the 12th, 13th, 14th bits are reserved like"100" for HMC830 and 21st and 20th bits are also reserved like "00".

- *Reg 0Ch Fine Frequency Correction Register:*

This Fine Frequency Correction Register is set as default. In this register, by the using of correction rate, the comparison frequency will be divided, must be an integer.

- *Reg 0Fh GPO_SPI_RDIV Register:*

In this GPO_SPI_RDIV Register, selects the signal output to SDO pin when enabled. The values of GPO test data, prevent automux"s are sets in this register. In this register, the LDO driver can be always ON

- *Reg 03h Frequency Register - Integer Part:*

Frequency Register-Integer part: RF path divider N which decides PFD by the using of below equation:

$f_{vco} = \frac{f_{xtal}}{R} (N_{int} + N_{frac}) = f_{int} + f_{frac}$ $f_{out} = f_{vco}/k$.

C. Frequency Tuning

Frequency tuning will be depends upon the actual subsystem in use. The VCO will restrict the possible range of operating frequencies.

In general, the control of internal fundamental frequencies of the VCO will be done automatically, when frequency registers are programmed. The user will be programmed separately for the divider output control. The wide band parts are configured via Printed circuit board connections.

The frequency tuning will be done in 2 modes, these are: 1.Integer mode 2. Fractional mode

1. Integer Mode:

In Integer Mode, the integrated VCO will be capable of operated. For this mode set the fallowing register:

1. Disable the fractional modulator Reg 06 h=0

2. Bypass the modulator circuit, Reg 06h=1.

The phase noise is less in integer mode than the Fractional Mode for a certain Phase Detector operating Frequency. The Charge Pump offset must be deactivated.

2. Fractional Mode:

The advantage of Fractional Mode is that greater phase detector frequency can be used; hereafter the low Phase Noise can be understood in fractional mode.

In the fractional mode, the Phased-Locked-Loop with integrated VCO is set the fallowing registers:

A. Enables the fractional Modulator, Register 06h=1

B. In circuit, connect the Modulator, Register 06h=0

The Fractional Mode can complete the Frequencies at Fractional multiples of the position. The Frequency of these integrated VCO, f_{vco} is assumed by

$f_{vco} = \frac{f_{xtal}}{R} [N_{int} + N_{frac}] = F_{int} + F_{frac}$ ….1

A. $f_{out} = f_{vco}/K$....*2*

Where:

Fout = Output Frequency later any possible dividers or doubles.

K = 0.5 for double, 1 for essential

Published by: The Mattingley Publishing Co., Inc.

March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

K = 1, 2, 4, 6….58, 60, 62 based on the VCO Subsystem type.

N_{int}= Division ratio of Integer, Register 03h, an Integer number in amid 20 & 524, 284

N_{frac} = fractional Part, starting 0.0 to 0.99999, N_{frac} = Reg 04h/2^{24}

R = Division ratio of reference path, Reg 02h

f_{xtal} = The reference oscillator input frequency

f_{pd} = The Phase detector operating frequency, f_{xtal}/R.

Integrated Phase-Noise and Jitter:

The deviance of VCO Signal Jitter may be expected with a simple estimation. If we assume, the Phase noise is constant for the locked VCO, $\phi 2$ (f_0) at Offsets lesser than Loop 3dB band width 20dB per decade roll XD off at greater offsets. The approximation phase noise of simple locked VCO is shown below figure 4.

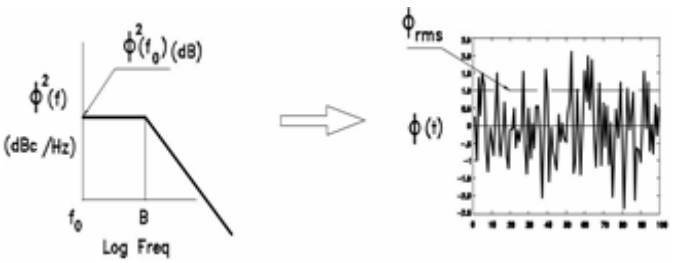

Figure (4): Phased-Locked-Loop with Integrated VCO Phase noise and Jitter

By using of this simplification, the total integrated VCO phase noise, $\phi 2$, in radian^2 in the linear form is given by

$\phi^2 = \phi^2 (f_0)/B\Pi$…….3

ϕ^2 ⟹ Single side band phase noise in rad^2/Hz Inside the band width

B ⟹ 3dB angle Frequency of the closed loop At the Frequency of Phase detector, $\phi 2pd$, the integrated

Phase- noise is just scaled by N^2.

$\phi^2_{pd} \phi^2/N^2$……4

The VCO rms phase jitter in radian"s, ϕ, is objective of the square root of Phase-Noise Integral. Hence, the modest integral of equation 3 is objective an invention of factors, we can simply integrated in the loop demine.

For example inside the loop, if the VCO phase noise is-100 dBs./Hz at 10KHz,and the division ratio is 100,then at the phase frequency detector, the integrated phase noise in dB is given by

$$\phi^2_{pddB} = 10\log(\phi^2(f_0)\, B\Pi/N^2) = -100+50+5-40 = -85 \text{ dB}.$$
$$\phi = 10^{-85/20} = 53.6\text{e-}6 \text{ rads} = 3.2\text{e-}3 \text{ degrees}.$$

After the division of the reference, the phase noise reduced by a factor of 20logN, because of increased the period of the PD reference signal. The jitter will be constant. From the phase noise, the rms jitter is given by

$T_{jpn} = T_{pd}\phi_{pd}/2\Pi$…….5

In the above example, if the Phase detector reference was 50MHz, T_{PD} = 20ns, and hence T_{jpn} = 179 femto-sec.

The last expression is becomes based upon the closed form an Integral of the entire spectrum of the phase noise of the oscillator. At the DC, this integral will be started. It is same for real system to calculate jitter over smaller intermissions of time; therefore, at the same finite frequency offset, the integral often will be started and will generate a jitter. The generated jitter is lesser than that specified by the above Full Expression.

Lastly, these Oscillators have noise floors that also added to the jitter. The Phase-Noise of a white noise floor is a Simple Integral of noise floor density times Band width to the system. The remaining noise power will be added to "f_{out}";

$F_{out}=f_{VCO}/2$=1002.5 MHz + 0.6 Hz error Get a more accurate jitter number.

Published by: The Mattingley Publishing Co., Inc.

March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

D. Reference path 'R' divider:

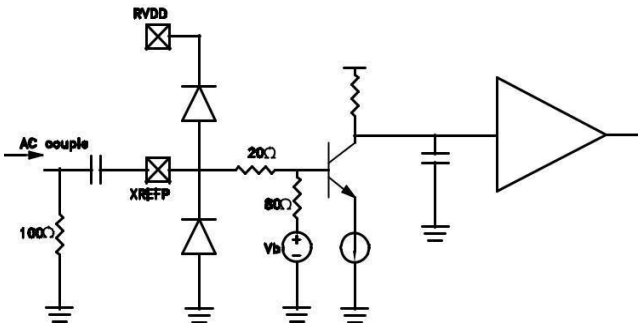

Figure (5): Reference path input stage

Based on 14-bit counter, the reference path „R" divider will be works and it can be divides the input signals by the values from 1 to 16,383 and it is organized by RDIV (Register 02h).At the Reference, the maximum pulse width input is 2.5ns.For the best spur performance when R = 1.The pulse width is must be (2.5ns+8TPS).

TPS is the time period of VCO at the presale input, when R>1 maximum Pulse Width is 2.5ns.

E. Charge Pump and Phase detector:

The Phase Detector is having 2 inputs. One is from RF Path Divider and another one is from the divider Path of the reference. These 2 inputs are locked at the similar Frequency and permanent at a constant phase Offset with respect to both. We assign the operation frequency of the phase detector as the f_{pd} . Most of the formulas are relevant to step size, Delta sigma modulation, timers, etc. Those are the functions of the operating frequency of PD, f_{pd}.. f_{pd} is also assigned as the contrast Frequency of PD.

F. VCO Serial Peripheral Interface (VSPI):

The PLL has been communicating with the Internal VCO Sub-System through an 16 bit VCO Serial Port,(see figure:3).To control the Step-Tuned VCO and other VCO Sub-System functions by using the internal serial port, if available RF output divider and RF buffer is enabled. The clock frequency of SPI cannot be better than 50 MHz

The VSPI clock rate is fix by Register 0Ah(14:13) writes to the Control Registers of VCO"S are indirectly held through written to Reg 05h of the PLL, because of the PLL subsystem can be forward the packet, MSB first, across its VCO subsystem to internal serial link, wherever it is interpreted.

The capability of the VCO Serial Port has to connect with the several Subsystems inside the IC, for this purpose every Subsystem has a Subsystem ID, Register 05h (2:0). To Control the functions from Internal to the Subsystem, each subsystem has multiple registers, which may different from one subsystem to next subsystem. Hence, every Sub-System has the addresses bits of the Internal register (Reg 05h (6:3)).

Finally, every register with in the VCO subsystems will contained in Reg 05h (15:7).

VSPI use of Reg 05h:

The Data of Packet written into Register 05h is break-down by logic at the Subsystem of VCO can be divided into the 3 fields

1) [2:0]-3bits=VCO-ID, ID of target subsystem 101 or 000b based on the used Product.

2) [6:3]-4bits=VCO_REGADDR, inside VCO subsystem.

3) [15:7]-9bits=VCO_DATA, to write the data field into the VCO Reg.

The auto Cal controller updates only the data field of Reg 05h.The VCO_ID bits and the VCO_REGADDR must also be set correctly or auto Cal will send its data to the wrong location. By initializing Reg05h (6:3) =0, to set VCO_REGADDR=0.The ID of subsystem is depends on the type of device. Set the subsystem ID to "0" (Reg 05h (2:0) =0) for wideband devices.

G. Serial Port modes of operation:

There HMC PLL with Integrated VCO Serial Port Interface can operate in different modes:

Published by: The Mattingley Publishing Co., Inc.

March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

a) HMCSPI HMC MODE-Single slaver per HMCSPI bus.

b) HMCSPI Open mode-HMCSPI Bus having up to 8 slaves.

These modes can be useful to replicate protocols found on another manufacturer"s PLL. Both modes are supports 5bits of Register Space. The Mode of the HMC can be supports up to 6bits of register, addresses.

Serial port HMC mode – Single PLL:

The Mode of HMC Serial-Port operation can only talk to single PLL and address, and compatible with PLL"s with integrated VCO"s and most HMC PLL"s. The HMC mode protocol is shown in below figure: 6, is considered for a four wire interface with a fixed Protocol containing.

1 Read/write bit-1

2 Address bits-6

3 Data bits-24

4 3 Wire for write only, 4 write for Read/Write Capability.

The HMC Write cycle is shown below figure: 6,

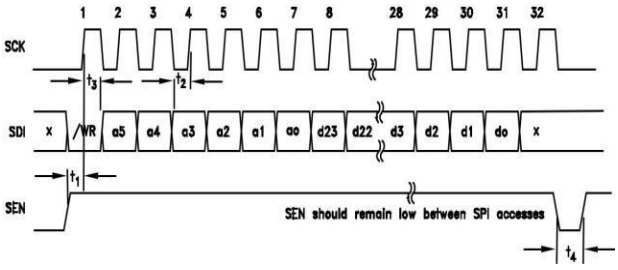

Figure: 6.HMC mode-Timing diagram of Serial port-WRITE

a) The Master Declares SEN (Serial Port Enable) and frees SDI to mark a write cycle proceed by a rising edge of SCLK.

b) The Slave (Synthesizer) reads SDI at first rising edge of SCK after SEN.

c) Host Places the 6 address bits above the next 6 falling edges of SCK, MSB first.

d) Slave changes the address bits in the next 6 Rising Edges of SCK (2-7).

e) Host places the 24 data bits above the next 24 falling edges of SCK, MSB first.

f) Slave transfer the data bits over the next 24rising edges of SCK (8-31).

g) The data is registered within the chip at the 32nd rising edge of SCK.

h) SEN is cleared subsequently a least delay of t_5.This executes the right cycle.

III. HARDWARE SETUP & RESULTS

A 10 MHz external reference frequency (Andhra Electronics OCXO 2051) is fed to HMC830 evaluation board. And DC power supply to +5.5V. To tune the PLL to desired frequency, the PLL registers should be updated over SPI during Power on Reset (POR). To configure the PLL registers, a VHDL code has been written to update the PLL registers. The complete hardware setup is shown in figure (7).

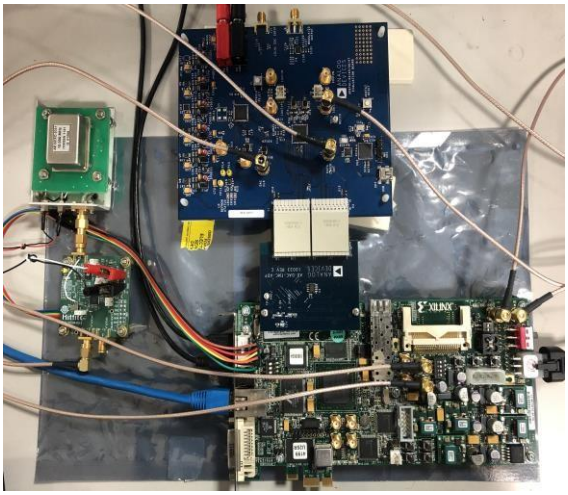

Figure 7: Hardware setup of PLL

For typical applications, only some of the registers are programmed and others left with default values. The sample registers values for 100 MHz frequency in integer mode is given below.

Published by: The Mattingley Publishing Co., Inc.

March - April 2020
ISSN: 0193-4120 Page No. 7394 - 7402

Register 00h - 0x00000000

Register 01h- 0x00000002

Register 02h - 0x00000001

Register 05h - 0x00001628

Register 05h - 0x00006F10

Register 05h - 0x00002898

Register 05h - 0x00000000

Register 06h - 0x002003CA

Register 09h - 0x00003264

Register 03h - 0x0000003C

The block diagram of the hardware setup is shown in figure (8).

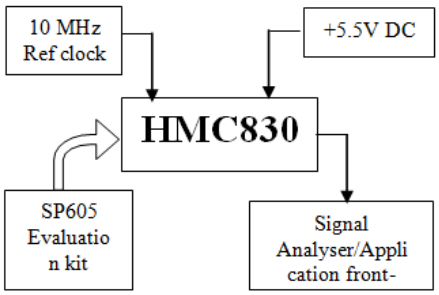

Figure 8: Hardware setup Block diagram

The PLL registers are configured for 100 MHz frequency on startup. The phase noise for 100 MHz at 1 KHz, 10 KHz, 100 KHz offset are obtained as -115 dBs/Hz, -117dBs/Hz, and -133 dBs/Hz as shown in figure 9a.

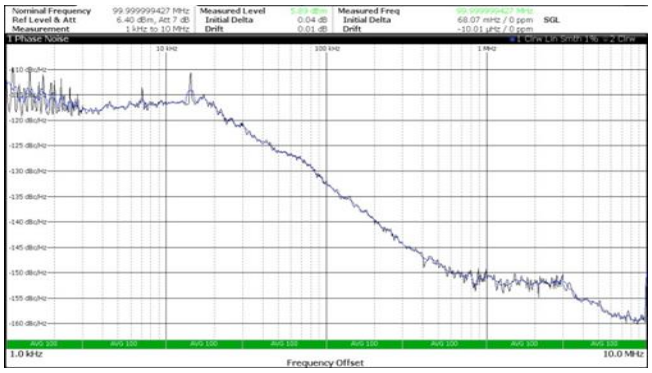

Figure 9a: Phase Noise plot of 100 MHz

And SFDR of the 100 MHz signal has been measured and it is around -100dB which clearly shows the superior performance of the device.

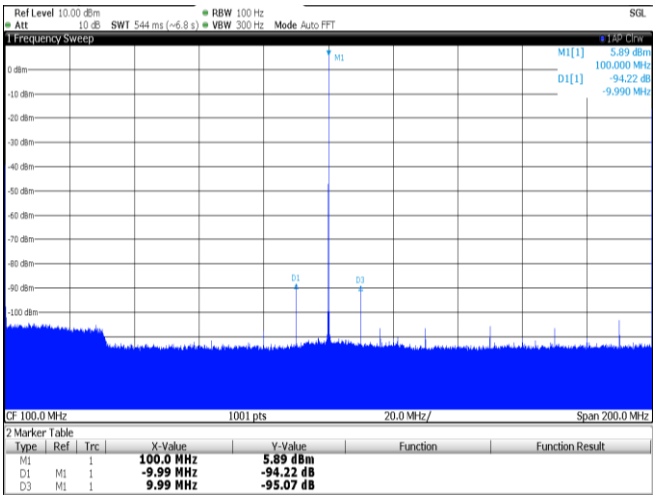

Figure 9c: SFDR plot of 100 MHz

IV. CONCLUSION

A wideband, low phase noise clock source has been implemented. The phase noise and SFDR values are clearly shows that the device is giving superior phase noise and SFDR which is very much important in applications like high speed data converters, local oscillators, radar receivers etc., The derived 100MHz clock is used as sampling clock for Digital-to-Analog converter (DAC) whose 5MHz output is having phase noise of -91 dBs/Hz at 1KHz offset. This device can produce a spectrum with frequencies from 25 MHz to 3000 MHz with superior phase noise, which will be very useful performance in wideband applications.

REFERENCES

[1]. a 1.6-10.9 ghz voltage-controlled ring oscillator for the serial interface of hi gh-speed data converters Ang Gao, Hong Zhang*, Huihui Mao, Dong Li, Mudan Zhang, Jun Cheng Department of Microelectronics, Xi'an Jiaotong University,Xi'an,71 0049, CHINA*Corresponding Author's Email: hongzhang@mail.xjtu.edu.cn.

[2]. A low-phase-noise 5-GHz CMOS quadrature VCO using superharmonic coupling, S.L.J.

Gierkink ; S. Levantino ; R.C. Frye ; C. Samori ; V. Boccuzzi
[3]. Design and Implementation of an Ultra-Wide Band, High Precision, And Low Noise Frequency Synthesizer Yas H Faculty of Electrical Engineering,Sharif University of Technology, Tehran, Iran yas.hosseini@ee.sharif.ir Nasser Masoumi Faculty of Electrical and ComputerEngineering, University of Tehran, Tehran, Iran nmasoumi@ut.ac.ir
[4]. Design and analysis of low power low phase noise vcop. Dudulwar, k. Shah, h. Le, j.Singhvictoriauniversity, Australia.
[5]. https://www.analog.com/en/products/rf-microwave/vcos-plos/wideband-vcos.html.

AUTHORS PROFILE

SHAIK ANUSHA currently pursuing Master of Technology in the department of Digital Electronics and Communication Systems from School of Engineering and Technology, Sri Padmavathi Mahila Viswavidyalayam. Tirupathi and her main research work focuses on VLSI, communication, and IOT based education. And she is the member of International Association of Engineers.

M Krupa Swaroopa Rani, Assistant Professor in the department of Digital Electronics and Communication Systems from School of Engineering and Technology, Sri Padmavathi Mahila Viswavidyalayam. Tirupathi Her main research work focuses on VLSI, communication, and IOT based education. And she is the member of International Association of Engineers

K.M.V. Prasad received his B.Tech Degree in Electronics and Communication Engineering (ECE) from Sri Venkateswara University College of Engineering (SVUCE) SV University (SVU), Tirupathi. He joined National Atmospheric Research Laboratory (NARL) in April 2014. His areas of interests include digital implementation of controllers using FPGA devices, digital signal processing, data acquisition systems and Radar systems