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Bridging Defect Detection for Fault Diagnosis of On-Chip Cache Memory

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Abstract

Effect of bridging defect and the weak resistive open defect is a plunge key in the area of research. In these smart gadgets and devices world using VDSM technology, it is of utmost importance to analyze the effect of resistive open defects in on-chip cache memory since it occupies the largest part of complex systems and devices. Technology enhancements lead to an increase in distresses with the normal operation of the system due to process variation and temperature. Sensing weak resistive open defect and bridging defect in the on-chip cache memory is needed for the reliable operation of the circuit. This paper estimates the effectiveness of the proposed pre-discharged feeble cell detection (PDFCD) technique used to detect bridging faults and weak resistive open defects in on-chip cache memory. The fault detection capabilities analyzed for a large range of resistive values at random locations in memory. The implementation of the proposed method gives a minimum area overhead of 3.87% and less time penalty of 20.48µs for 1KB of memory.

Keywords – *Bridging Defect, Cache Memory, Fault Detection, Embedded Memory, Redundant Elements, Resistive Open Defect (ROD).*

I. INTRODUCTION

Smart devices era has already started with smart technology used in almost all gadgets and applications nowadays. The smart technology era supported by a very important part of the system that is memory. Rapidly growing technology demands more reliable operations of systems used in different domains like artificial intelligence, neural networks, biomedical, space, internet of things, cloud computing, etc. Various methods had proposed to detect faults in memory were concentrating on functional fault detection. But in Very Deep Sub Micron (VDSM) technologies, resistive open defects are now becoming prominent. If the resistive value is less, it's called a weak resistive defect, which is difficult to detect. Since the presence of weak resistive defect does not nosedive read and writes operation of the cell. But it significantly hampers SNM of the cell. Eventually, by successive operations on cells, the weak resistive defect becomes a strong resistive defect, and the cell becomes unable to hold static value. The resistive defects present at the source location of pullup and pulldown transistors are more prominent. Hence there is a need fora domineering technique to detect resistive defect faults in memory. Resistive defect plagues at any location in memory, including cells and its peripheral circuitry.

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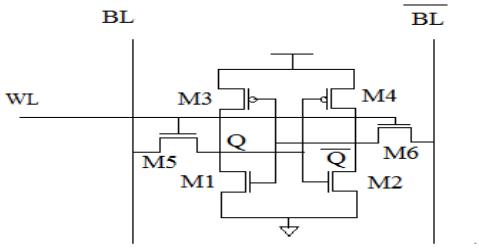

Fig. 1. Six Transistor Cell

Substantial efforts have given to detect resistive open defects in memory. But more stress needs to be given on the detection of weak resistive defects. Normal six transistor cells in the on-chip cache memory structure, as shown in Fig. 1. It consists of a pair of inverters connected cross-coupled to hold data in a cell without the need fora refresh circuit.

Various methods have projected for the detection of faults in memory. A predetermined order of read and write operations need to apply on memory cells in decided order to detect faults in memory called the March test sequence. By inserting a small current surge in the memory cell to imbalance cell and perform two read operations to detect a fault in memory is used [1].With an increase in word line activation, the detection of dynamic faults in memory is shown [2]. Read the equivalent stress method [3] is used to detect bit-line coupling faults in memory. Fault detection in memory after waking up from drowsy mode [4] explained for drowsy cache memory. In Linked fault detection using the March test [5] used by varying read-write sequence applied to cells to detect faults is shown. Pre discharged writes test mode [6], floating ground voltage is applied to bit lines for weak write operation used to detect faulty cells in memory. A consecutive read operation on the same cell prohibited for increasing reliability of the circuit is discussed in [7]. A comprehensive analysis of all types of March tests shown in [8].By analyzing SNM, the variable voltage on bit lines [9] applied by using a specific number of cells in a column to detect faulty cells in memory. The built-in Self Repair scheme is discussed in [10],which uses a bitmap to store information about defective cells. Quiescent current (I_{DDQ}) sensing method is also used [11] with Built-In Current Sensor for the detection of faults in memory. The method based on the topology that the presence of faults in memory results in the rising of quiescent current. Similar to the I_{DDQ} technique, transient current I_{DDT} technique [14] with the hardware-based approach also used to detect faults in memory. In which using the current sensor circuit and comparing output with neighborhood cells, defective cells detected in memory. But as technology has changed to the VDSM amount of leakage current is too large. So it becomes difficult to predict that change in current resulted is due to fault or not. By varying supply voltage to cells, faults in cell detected discussed in [16]. Another method based on the I_{DDT} technique [17] for the detection of faults presented. Using negative bias temperature coefficient [18] method, applying aging effect impact on resistive defect and bridging defects in memory are analyzed. Word line under drive [19] with programmable read and write timings are applied to detect faults in memory. Bridging defects in memory cells at different locations analyzed in [20,21]. The impact of resistive defects on the core cell and neighboring cells studied.

II. Resistive Defects and Bridging Defects In SRAM

A. Sources and Effects of Resistive Defect Faults

Two sets of inverters are tied in a cross way in 6 transistor SRAM cell, connected back to back. Pull-up transistors hold logic data 1, and pulldown transistors are responsible for holding logic data 0. Access transistors used to activate the cell. Resistive open defect (ROD) can ensue at any terminal of transistor or connection between two terminals. Possibility of ROD at 23 locations in the cell, as shown in Fig. 2. The resistive defect generates due to weak vias or connection. By aging effect, weak defects become stronger later. The resistive defects in pulldown transistors are easier to detect compared to pull up transistors. Since bitlines are precharged before the read operation. If there is a

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resistive defect in the discharge path of current through access or pulldown transistor, its associated bitline (BL/BL) couldn't pull down. It leads to easier detection of fault by observing the result of read operation data. In case of resistive defect present in load transistor, precharged value on bitlines remains as it is. So it becomes difficult to detect resistive defects in pullup transistors compared to pulldown transistors.

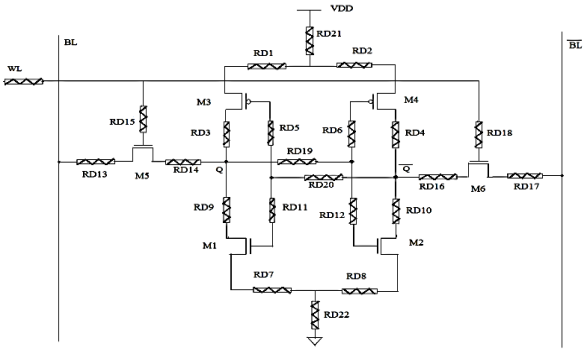

Fig. 2. Resistive Open Defects in Cell

If the time delay between two precharge cycles is more, it becomes difficult to detect faults in pullup transistors since cross-way connected inverters get enough time to overcome charge reduced due to resistive defect. Hence cell shows valid read and write operations. Similar to resistive defects at different terminals occur, a bridging defect may occur between any two terminals. Ideally, when no connection expected between terminals but because of some reason if two terminals are shorted or get coupled through the bridging defect. Fig 3 shows possible locations of bridging defects in the SRAM cell. Bridging defect stronger values does not affect the normal operation of the cell. But as bridging resistive value decreases in terms of kilo-ohms, it hampers the normal functioning of the cell. So bridging resistive defects also need to be taken care of in memory for the proper working of cells.

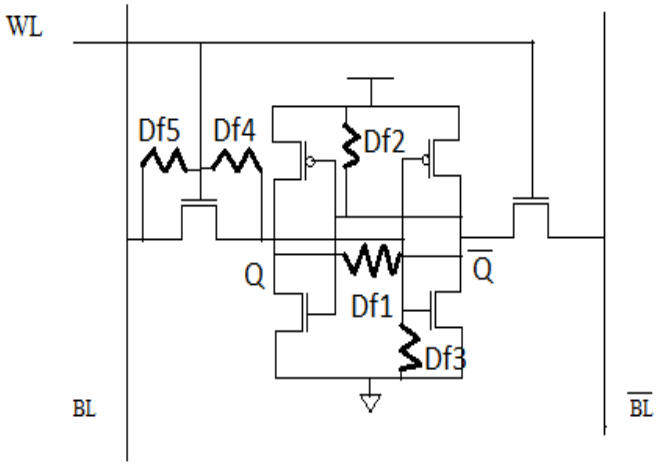

Fig. 3. Cell with Bridging-Resistive Defects

B. Methods for Detection of Resistive Defect Faults

Many methods have realized for the detection of resistive defects in SRAM memory. Out of those methods, key methods of detecting faults in memory discussed here. The initial method is based on the topology of weak write test mode and predischarged write test mode. In these methods, write operation is performed by applying floating bitline instead of charging bitlines to 1 and 0. Compared to a normal write operation, it's performed by pulling one of bitlines low to floating zero and other bitline to strong zero value. It acts such that writing data 1 into a cell will be harder, which leads to easy detection of resistive faults in the cell. The second method is the March test, which used widely. A specific sequence of read and write operation needs to be performed on cells to detect faults in memory. But it does not explore much on resistive defect detection. Also, the time taken by the March test is too high compared to other methods though it can detect maximum type of static and coupling faults in memory. Third method Read Equivalent Stress in which consecutive read operations performed on cells by applying precharged voltage on bitlines such that selected cells and unselected cells in an activated row are repeatedly attacked by the precharged voltage on bitlines. Precharge circuit is on for unselected columns in a row. So unselected cells undergo severe attack of precharge high voltage. If resistive defect fault present in a cell, it

will get easily flipped and can be detected.

C. Resistive Open Defects Models

Faults in memory are majorly divided into two types as static and dynamic fault models. Similarly, ROD represented with logical fault models. These fault models also considered based on effect by a change in threshold voltage, change in oxide thickness, and channel length [1]. ROD can occur at any terminal of transistors or between any connections of terminals. All possible locations of ROD in on-chip cache cellsshown in Fig. 2. For simulation to analyze the effects of a resistive open defect, one defect is considered at a time for simplicity, as it would be a practical case. Logical fault models that are represented by ROD shown in Fig. 2 are listed as follows [12]

- Transition Fault: This type of fault occurs in a cell if a cell is unable to shift from 0 to 1 or 1 to 0 when write cycle accomplished on cell.
- Read Destructive Fault: This type of fault occurs in a cell if the read cycle accomplished on a cell leads to flipping of stored data and gives wrong data at output terminals.
- dynamic Read Destructive Fault: This type of fault occur in a cell if the write cycle forth with followed by a read cycle accomplished on the cell leads to flipping of stored data and gives wrong data at output. The instance at which this fault may occur can vary from a 10^{th}read to 2^{nd}read operation.
- Deceptive Read Destructive Fault: This type of fault occurs in a cell if the read cycle accomplished on cell results into the flip of stored data and gives the right data at output terminals.
- Dynamic Deceptive Read Destructive Fault: This fault occurs in a cell when the write cycle forthwith followed by a read cycle accomplished on the cell results into flip of stored data but gives the right data at output terminals. The instance at which this fault may occur can vary from a 10^{th} read to 2^{nd} read operation.
- Incorrect Read Fault: This type of fault occurs in a cell when a read cycle accomplished on the cell does not flip data value but gives wrong data at the output.

III. Proposed Predischarged Feeble Cell Detection Method

Resistive defects of different values injected in an on-chip cache memory cell for the analysis. Values of ROD taken range from 0 to Tera ohm through infinity. Different locations are considered for resistive and bridging defects, as shown in Fig. 2 and 3. The proposed method based on stress given by predischarged bitline for fault detection on the cell under test activated through word line. If the cell is fault-free, it can sustain with predischarged bitline stress and maintain stable data in a cell. The cell can restore data in consecutive read operations. But the presence of resistive defect inside cell makes it unstable, and cell, therefore, becomes unable to store data and data may get flipped depending on the strength of resistive defect. For weak resistive defect fault, longer predischarged bitline stress needs to apply for detection.

Whereas for a larger value of resistive defect, it can easily get detected with shorter duration stress since the current flowing through the path of resistive defect gets immediately affected. For resistive open defect, the current flowing through that terminal gets weaker, which results in lowering bitline voltage leads to the direct detection of faults. The behavior of the circuit is observed for various values of ROD to sense the type of model for each defect location by applying a write cycle followed by consecutive read operations. The range of resistive open defects for different models is observed from no-fault condition to open defect condition. Bridging defects, as shown in Fig. 3, sensed for various resistive values in the cell. Also, the effect of bridging defect on neighboring cells observed. Earlier methods for detection of ROD incur higher area overhead as

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well as require complex timing circuitry [19]. So it is essential to design a simple fault detection circuit that can detect the faults with low area overhead and less time latency.

The different types of ROD that can occur at 23 possible locations of ROD are as shown in Fig. 2. The possible locations increased by bridging defects. So it is necessary to detect all these kind of faults in memory for smooth and reliable operation of devices. In the proposed method, PDFCD, bitlines are predischarged to a specific level analyzed based on SNM of the cell using predischarge circuit, as shown in Fig. 4.Predischarge achieved by using NMOS transistor connected to each bitline in parallel with parasitic capacitance. Cell testing is done under stress. Following read cycle and word line activation used to sense the faults in the memory.

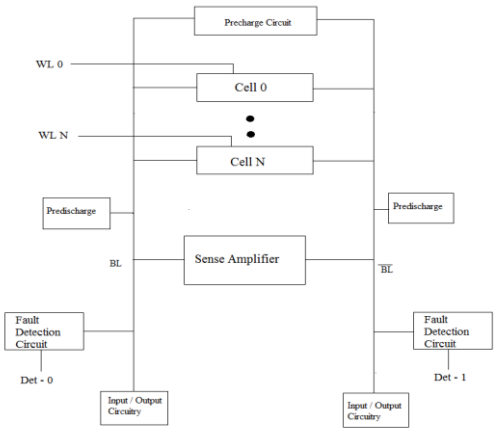

Fig. 4: Block Diagram of Predischarged Feeble Cell Detection

Fig. 5. Simulation Results of Resistive Open Defect

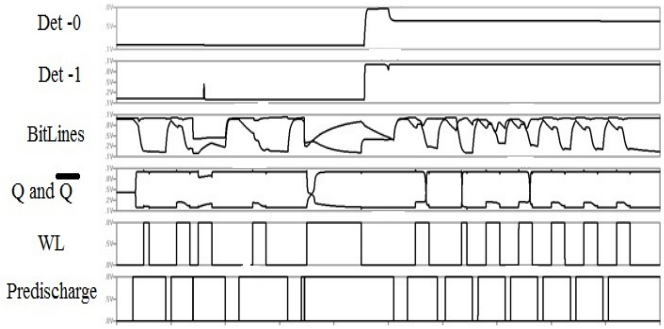

Fig. 6. Simulation Waveform of Bridging Resistive Defect

$$I_{bitline} = C_{bitline}\frac{\delta v}{\delta t} \quad (1)$$

$$I_{bitline} = \frac{C_{ox}W_a v_{dsat}(V_{DD} - V_q - V_{tha})^2}{(V_{DD} - V_q - V_{tha}) + E_{cn}L_a} \quad (2)$$

The presence of a fault in the cell may results in a flip of stored data, depending on the strength of resistive open defect. Stronger the value of ROD earlier is detection during word line stress. The method stressed for the detection of bridging defects and weak resistive defects in memory. The design of the schematic of the SRAM cell and its peripherals done by using 45nm technology. The access time obtained is 300ps verified with the simulations. During the analysis of simulation, it is observed that the access time of memory limited by capacitance associated with bitline. As shown by Equation 1, the current flowing through bitline also depends on bitline capacitance. For high-speed operation, bitline capacitance should be smaller. But the layout of memory reveals that parasitic capacitance increases bitline capacitance dramatically, which hampers access time. Equation 2 shows the dependence of bitline current, which is the drain current of the transistor also depends on threshold voltage and body effect parameter. It shows that change in process variation affects bitline current.

The circuit is checked for open defects in the memory cell as well. The simulation result of the ROD in pull-up transistor is as shown in Fig. 5.The fault is indicated by the Det-0, which is the output

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ofthe fault detection circuit. The circuit also simulated for bridging defects. Fig. 6 shows the bridging defect Df5 associated with access transistor is detected, as shown by Det-0 and Det-1 by both circuits. It also shows dynamic read destructive fault detected at second read operation immediately followed by write cycle. The fault detection circuit compares data written onto a cell with data read from the cell after stress applied to the cell under test. If a difference occurs, it will immediately be notified by the detection circuit. Given predischarged word line (WL) stress on cell, if resistive defect present in cell, the current flowing through the transistor will not be sufficient enough to hold a state of cell. For weak resistive defects, it is difficult to detect only based on current detection. The proposed method shows improvement in the values of weak resistive defects. Earlier detection of faults before becoming high values of defects helps to increase the reliability of devices or applications in which memory used. The layout of the proposed method is as shown in Fig 7. Data on bitlines read during the initial write cycle performed on the cell under test. Then next cycle data is compared with data present in the cell. Followed by the application of predischarged word line stress on cell again, data obtained from bitlines compared with previous data. If both values are the same, it means data does not flip into a cell. Hence no resistive fault present in cell. But if mismatch in data occurred after comparison, it shows the presence of resistive open defect or bridging defect present in a cell.

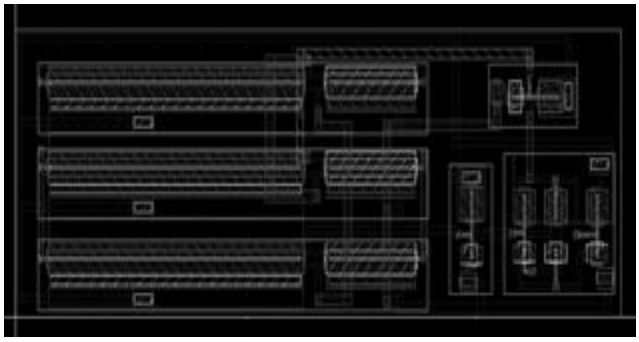

Fig. 7. The layout of Resistive Fault Detection Circuit

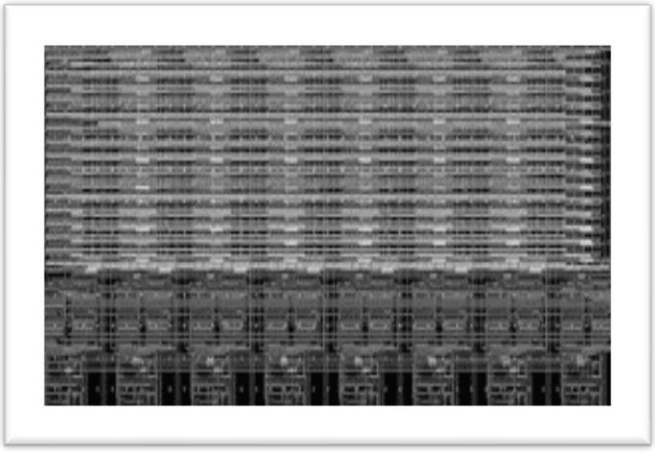

Fig. 8. The layout of 64X8 SRAM Memory Structure

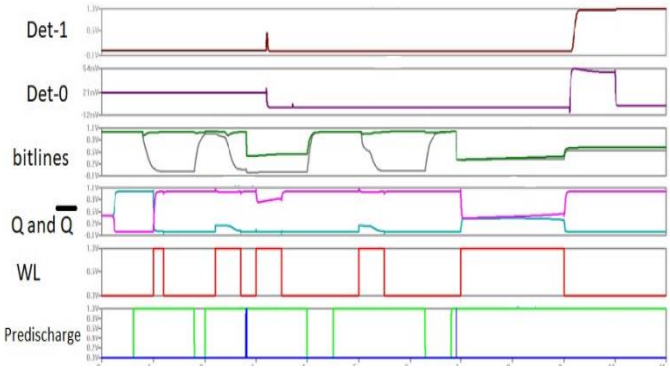

Fig. 9. Simulation Waveform of ROD Detection at V_{DD}

IV. Performance Analysis

On-chip cache memory designed using 45nm technology taking parasitic resistor and capacitor into consideration. For checking the feasibility of the proposed method, simulations are performed initially on schematic level and then onits corresponding layout. The peripheral circuits required, such as a precharge circuit, a sense amplifier, input/output circuit designed to acquire optimum performance parameters. For fault detection analysis, all possible locations of faults considered, as shown in Fig. 2 and Fig. 3. The validation of proposed predischarged feeble cell detection (PDFCD) has been performed on the schematic level to resolve issues. A redundant cell added on top of each column. This redundant row added at the top in the designed memorywill be used for the redundancy mechanism. If more than one cell is detected faulty in a row, it can be

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substituted by the redundant row. The results of fault detection verified through simulation by inserting ROD at all possible locations one at a time. Dynamic behavior of fault also verified by applying multiple read operations after a single writes cycle. Later, for layout 64X8, the memory array is designed in the Cadence virtuoso tool using 45nm technology, as shown in Fig. 8. It consists of 8 columns with 64 cells each and peripheral circuits. PDFCD circuit is also integrated with each column, as shown in Fig. 8. Designed schematic and layout is verified for normal read and write operation with the attached fault detection circuit for optimized access time. The simulations waveform for ROD present at the supply voltage terminal, as shown in Fig 9. It observed that the access time of memory largely depends on capacitive load on bitlines. Also, parasitic elements increase the capacitive load on bitlines. Therefore many cells in a column are restricted for obtaining optimum access time. Initially, faults introduced at the column-level for detection. Hard to detect fault stability fault is also tested through simulation.

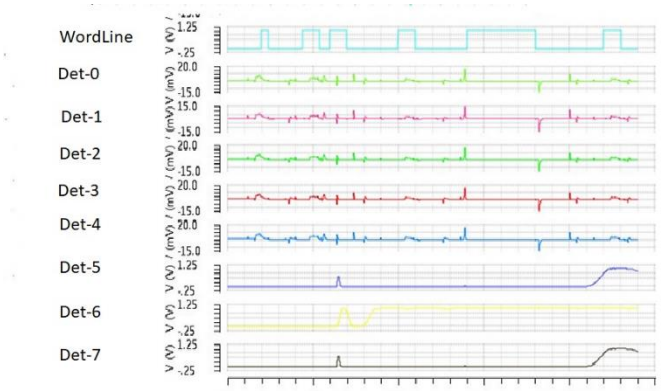

Fig. 10. Simulation Results of Layout of 64X8 SRAM

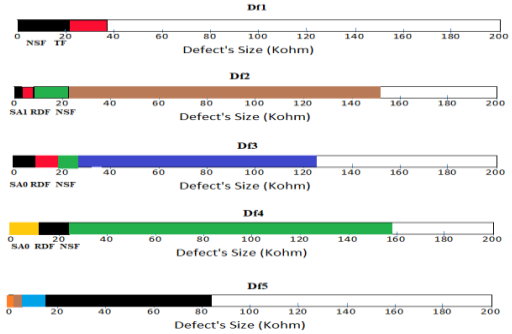

Fig. 11. Logical Fault Model of Bridging Defect

Similarly, the weak resistive open defect is detected at all terminals of 6 transistors in the cell by inserting ROD by changing its value from zero to infinity. Comparatively high values of ROD are getting detected at gate terminals of all devices since the reduction in gate current due to weak resistive open defect does not have much impact on the normal operation of cell. Later, schematic and layout extended at the byte level structure. Faults randomly generated in different columns at random locations. Simulation waveforms verified for all random location resistive defect faults in memory at different positions in columns. Itverified that the attached predischarged feeble cell detection circuit does not hamper the normal operation of the memory. Nondefective cells verified at different column levels in memory. The fault present in column 6is getting detected in the simulation waveform, as shown in Fig. 10 by Det-6.

As seen earlier, there are different logic fault models of ROD. The behavior of resistive bridging fault at different values represents which fault model depends on its position. Fig. 11 shows the logical fault model for different values of bridging defects. As it shows, all bridging fault gets detected at zero value, which is the worst-case condition for cells since it is an unwanted connection formed in a cell. Initially, Df1 shows no store fault up to 10K, after which it shows transition fault. Df2 shows stuck at 1 fault till 3.1K. Then read destructive fault till 4.5K after which no store fault. PDFCD can detect fault up till 150K. Similarly, for Df3 location, stuck at 0 fault observed up to 8.9K. Then the circuit show read destructive fault up to 27K, followed by no store fault till 125K. Fault Df4 shows stock at 0 behaviors till 10K. Later it shows no store fault. Fault Df5 has an impact on the same cell as well as a cell in the same column effects observed. Fault Df5 shows transition fault, read destructive fault, dynamic read destructive fault, and no store fault till 85K.

V. RESULTS

In earlier sections, the detection of ROD and bridging defects discussed. The design of memory

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with peripheral circuitry, fault detection circuit, and simulation is performed Cadence 45nm technology. Table I shows minimum detectable resistive open defect values of earlier methods compared with proposed predischarged feeble cell detection. Weak resistive open defect values for which circuit able to detect has improved. Hard to detect resistive defect at the source of pullup transistor gets detected at 1.5Kohm compared to other techniques. Resistive open defect value at the source terminal of access and driver transistor, as well as drain terminal of the access transistor, are also improved compared to hardware-based approach, word line under drive, and I_{DDT} method. The defect value at the word line terminal is improved compared to word line under drive. The maximum detectable resistive bridging defect values comparison shown in Table II. Bridging defects should get detected from zero, which indicates unwanted short between terminals. As the value goes on increasing, it becomes difficult to detect. Table III indicates performance analysis comparison with state of the art methods. As shown, test time latency derives very less compared to other approaches. As well as area overhead achieved with the proposed method is less compared to previous methods. Therefore Predischarged feeble cell detection shows an overall improvement in resistive defect values with lesser time latency and minimum area overhead.

TABLE I

MINIMUM DETECTABLE DEFECT SIZE OF ROD

Defect Location	[19] 2019 WLUD	[18] 2018 NBTI	[14] 2016 HBA	Proposed PDFCD
Source-Load (Ω)	119M	> 2M	16.3M	1.5K
Source – Driver (Ω)	214K	73K	6K	4K
Source – Access (Ω)	86K	90K	6K	1.8K
Drain – Access (Ω)	597K	120K	6K	3K
WL (Ω)	3.1M	660K	110K	2M

TABLE II

MAXIMUM DETECTABLE DEFECT SIZE OF BRIDGING DEFECTS

Defect Location	[19] 2012 Impact	[18] 2018 NBTI	Proposed PDFCD
Df1 (Ω)	1210K	72K	33K
Df2 (Ω)	110K	22K	165K
Df3 (Ω)	612K	178K	125K
Df4 (Ω)	156K	178K	20K
Df5 (Ω)	2.52K	4.8K	5.2K

TABLE III

PERFORMANCE PARAMETERS

Defects	[19] 2019 WLUD	[18] 2018 NBTI	[14] 2016 HBA	Proposed PDFCD
Test Time	High	> 0.205ms	0.14ms	20.48µs
Area Overhead	High	--------	5.46%	3.874%

VI. CONCLUSION

With the help of the proposed idea of Predischarged Feeble Cell Detection, the ROD and bridging defects inon-chip cache memory would exactly locate, and weak resistive defect values are improved. The dynamic read destructive fault in memory cell checked from the 5th read cycle followed by write operation on the memory cell. The PDFCD method can be used for the detection of weak ROD as well as bridging defects in on-chip cache memory. The method has no effect on the performance of the circuit under test with the integration of the PDFCD circuit. The circuit implementation gives a minimum area overhead of 3.87% and less latency period of 20.48µs for 1KB of memory.

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VIII. REFERENCES

[1] Q. Chain, S. Mahmoodi, SwaroopBhuniya, Kaushik Roy, “Efficient Testing of SRAM With Optimised

March Sequences and A Novel DFT Technique for Emerging Failures Due to Process Variations," IEEE Transaction on VLSI Systems, vol 13, No. 11, pp. 1286-1295, Nov 2005.

[2] A. Ney, L. Dillio, P. Girad, L. Virazel, M. Bastian, V. Gouin,"A New Design for Test Technique for SRAM Core Cell Stability Faults," EDAA Design Automation and Test in Europe on 20-24 April 2009 at Nice, France.

[3] Sandra Irobi, Zaid Al-Ars, Said Hamdioui, "Detecting Memory Faults in the Presence of Bitline Coupling in SRAM devices," IEEE International Test Conference on 2-4 Nov 2010 at Austin, USA.

[4] W Pei, W Jone, Yiming Hu, "Fault Modeling and Detection for Drowsy SRAM Caches," IEEE Transaction on ComputerAided Design of Integrated Circuits and Systems, Vol 26, No. 6, pp 1084-1100, June 2007

[5] Said Hamidioui, Ziad Al-Ars, Ad J. van de Goor, Mike Rodgers,"Linked Faults in Random Access Memories: Concept, Fault Models, Test Algorithm and Industrial Results, "IEEE Transaction on ComputerAided Design of Integrated Circuits and Systems, Vol 23, No. 5, pp 737-757, May 2004

[6] Josh Yang, B Wang, Y Wu, Andre Ivanov, "Fast Detection of Data Retention Faults and Other SRAM Cell Open Defects," IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Vol 25, No. 1, pp 167-180, Jan 2006

[7] J. Li, T. Tseng, C Hou,"Reliability – Enhancement and Self Repair Schemes for SRAMs With Static and Dynamic Faults," IEEE Transaction on VLSI Systems, vol 19, No. 09, pp. 1361-1366, Sept 2010.

[8] M. Linder, A. Eder, U. Schlichtmann and K. Oberländer, "An Analysis of Industrial SRAM Test Results—A Comprehensive Study on Effectiveness and Classification of March Test Algorithms," in IEEE Design & Test, vol. 31, no. 3, pp. 42-53, June 2014.

[9] A. Pavlov, M. Sachdev and J. P. De Gyvez, "Weak Cell Detection in Deep-Submicron SRAMs: A Programmable Detection Technique," in IEEE Journal of Solid-State Circuits, vol. 41, no. 10, pp. 2334-2343, Oct. 2006.

[10] C Hou, J Li, "High Repair Efficiency BISR Scheme for RAMs by Reusing Bit-map for Bit Redundancy," IEEE Trans. VLSI Systems, vol 23, No. 9, pp 1720-1728, Sept 2015.

[11] C Hsu, M Ho, C Lin, "Novel Built-In Current-Sensor-Based IDDQ Testing Scheme for CMOS Integrated Circuits," IEEE Transaction on Instrumentation and Measurement, vol 58, No. 7, pp. 2196-2208, July 2009

[12] Ad van de Goor, Mike Todgers, Zaid Al-Ars, Said Hamdioui, "Dynamic Faults in random-Access-Memories: Concept, Fault Models and Tests," Journal of Electronic Testing Theory and Applications 19, 195-205, Netherlands, 2003.

[13] E.Grosser, M. Stucchi, Karen Max, W. Daehene, "Read Stability and Write Ability Analysis of SRAM Cells for Nanometer Technologies," IEEE J. Solid State Circuits, vol 41, No. 11, pp. 2577-2588, Nov 2006.

[14] A. Gomez, F. Lavratti et al., "Effectiveness of a Hardware Based Approach to Detect Resistive Open Defects in SRAM Cells under Process variations," Microelectronics Reliability, vol. 67, pp. 150-158, 2016.

[15] L. Dillilo, P. Girard, A. Virazel et al., "Efficient March Test Procedure for Dynamic Read Destructive Fault Detection in SRAM Memories," Springer Journal of Electronic Testing: Theory and Applications, vol. 21, pp. 551-561, 2005

[16] E. Vatajelu, L. Dillilo, A. Bosio et al., "Adaptive Source Bias for Improved Resistive Open Defect Coverage During SRAM Testing," 22nd Asian Test Symposium, pp. 109-114, 2013

[17] G. Gyepes, V. Stopjakova, D. Arbet, et al., "A new IDDT Test Approach and Its Efficiency in Covering Resistive Opens in SRAM Arrays,"Microprocess. Microsyst, vol. 38, No. 5, pp. 359-367, 2014

[18] M. Martins, G. Medeiros et al., "Analysing NBTI Impact on SRAMs with Resistive Defects," Springer Journal of Electronic Testing: Theory and Applications, vol. 33, pp. 637-655, 2017.

[19] Josef Kinseher, Moritz Voelker, Ilia Polian,"Improving Testability and Reliability of Advanced SRAM Architectures," IEEE Trans. Emerging Topics in Computing, vol 7, No. 3, pp 456-467, July 2019.

[20] R. A. Fonseca et al., "Analysis of resistive-bridging defects in SRAM core-cells: A comparative study from 90nm down to 40nm technology nodes," 2010 15th IEEE European Test Symposium, Praha, 2010, pp. 132-137.

[21] R. A. Fonseca et al., "Impact of Resistive-Bridging Defects in SRAM at Different Technology Nodes," J. Electron Test,June 2012, vol28, No. 3, pp. 317-329.