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Detection of Resistive Open Defect Fault in SRAM Memory Array Structure for Reliability against Failures

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Abstract
Detection of weak resistive open defect is a thrust area of research. In VDSM technology, the effect of process variation and temperature are challenging which results in strivingfor detectionof the weak resistive open defect (ROD) in Static Random Access Memory (SRAM). For the consistent operation of the circuit, fault-tolerant memory is required to be used. This paper evaluatesthe effectiveness of the proposed pre-discharged feeble cell detection (PDFCD) technique used for the detection of weak ROD in the SRAM array. Analysis of fault detection by the proposed method for a large range of resistive values at random locations in memory is explored. The proposed method gives minimum area overhead of 3.87% and less time penalty of 20.48µs for fault detection in 1KB of memory.

Keywords – *Fault Detection, Embedded Memory, SRAM Test, Redundant Elements Resistive Open Defect (ROD).*

I. INTRODUCTION

In almost all gadgets nowadays, a very important part of the system is memory. Continue growing technology demands higher reliability in different domains like biomedical, space, internet of things, cloud computing. Legacy of functional fault detection is not sufficient for memory. Since in Very Deep Sub Micron (VDSM) technologies, resistive open defects are now becoming prominent. Also, weak resistive defects are difficult to detect. A significant amount of research work has been done to detect resistive open defects but limited research effort has been taken to focus and detect weak resistive defects. Normal SRAM cell made up of 6T is as shown in Fig. 1. The resistive defects present at the source location of pullup and pulldown transistors are more prominent. Resistive defect plagues at any location in memory including cells and its peripheral circuitry. Hence there is a need fora domineering technique to detect resistive open defect faults in memory. Many efforts have been put on the detection of faults in memory. Multiple numbers of read and write operations need to be performed in a specific sequence and such sequence as a packet required to be applied to all the cells in memory. Weak ROD is hard to detect with this traditional method. Imbalancing cells by inserting a small current surge for detection of a fault in memory is used [1] which can be combined with the

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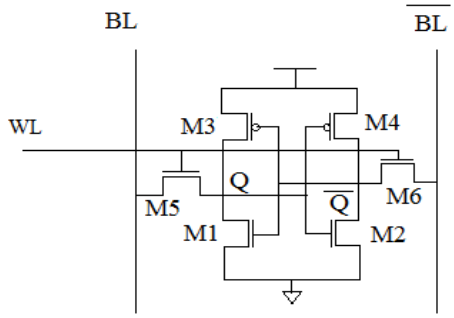

Fig. 1. SRAM Basic Cell Structure

March test. Read equivalent stress method [2-3] is used with an increase in word line activation to detect dynamic faults in memory. Predischarged write test mode [6] is used for the detection of weak resistive defects. The floating ground is applied to bitlines for implementing weak write data to detect weak cells in memory. In Programmable detection technique [9] by using a specific number of cells in a column and storing required data used as stress to detect weak cells in memory. Quiescent current (I_{DDQ}) sensing method is also used [11] for the detection of faults in memory. The topology used in this method is that the presence of faults results in the rising of quiescent current. But as technology has changed to the VDSM amount of leakage current is too large. So it becomes difficult to say a change in current resulted by the fault or not. Parallel to the I_{DDQ} technique, transient current I_{DDT} technique [14,17] with a hardwarebased approach is also used to detect faults in memory. Bias temperature coefficient method [18] can be applied to detect the resistive defect. Wordline underdrive [19] with programmable read and write time can be used for the detection of faults.

II. Resistive Defect Faults In Sram

A. *Source and Effects of Resistive Defect Faults*

Resistive defect fault can occur at any terminal in six transistor SRAM cell. It may occur at gate, source or drain terminal of any transistor in a cell as shown in Fig. 2. A resistive defect can be caused by weak contacts or connections.

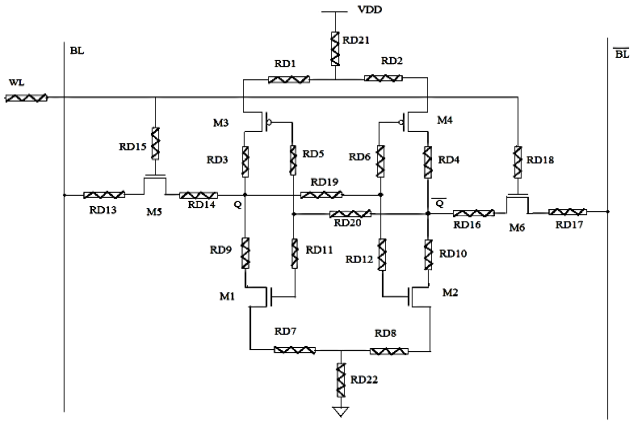

Fig. 2. SRAM Cell with Resistive Defects

The resistive defects in driver transistors are easier to detect compared to load transistors. Due to the fact that bitlines are precharged before the read operation. If there is a resistive defect in the driver transistor, its associated bitline (BL/BL) couldn't be pulled down. This leads to easier detection of fault by observing the result of read operation data. In the case of resistive defect present in the load transistor, the precharged value on bitlines remains as it is. So it becomes difficult to detect resistive defects in pullup transistors compared to pulldown transistors.

B. *Methods for Detection of Resistive Defect Faults*

Main methods for detection of resistive faults use predischarged write, read equivalent stress and high voltage read operation.

1) Predischarged Write: The write operation is performed by changing voltage levels of bitlines. Compared to a normal write operation, its performed by pulling one of bitlines low such that writing data into a cell will be harder leads to easy detection of faults in the cell.

2) Read Equivalent Stress: Consecutive read operations are performed by applying the precharged voltage on bitlines such that selected cells and unselected cells in an activated row are

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repeatedly attacked by the precharged voltage on bitlines. The precharge circuit is on for unselected columns in a row. So unselected cells undergo severe attack of precharge high voltage. If resistive defect fault present in a cell, it will get easily flipped and can be detected.

3) Insert Current Surge: Making an imbalance in the cell by inserting the current near sense amplifier used to detect faults in the cell.

C. Resistive Open Defects Models

A resistive open defect can occur at any terminal of transistors or between any connections of terminals. Performance degradation due to ROD at different location needs to be analyzed. All possible locations of ROD in SRAM cells are shown in Fig. 2. For simulation to analyze the effects of the resistive open defect, one defect is considered at a time for simplicity as it would be a practical case. Logical fault models that are represented by ROD shown in Fig. 2 are listed as follows [12]

- Transition Fault: This fault occurs in a cell when a cell is unable to switch from 0 to 1 or 1 to 0 after the write cycle is completed.
- Read Destructive Fault: This fault occurs in a cell when read cycle completed on cell results into the flip of stored data and gives wrong data at output terminals.
- dynamic Read Destructive Fault: Adynamic Read Destructive fault occur in a cell when awrite cyclestraightwaytrailed by a read cyclecompleted on cell results into flipping of stored data and gives wrong data at output terminals. The occurrence may range from a decade read to the second read operation.
- Deceptive Read Destructive Fault: A Deceptive Read Destructive fault occur in a cell when read cycle completed on a cell results into flip of stored data and gives right data at output terminals
- dynamic Deceptive Read Destructive Fault: A dynamic Deceptive Read Destructive fault occurs in a cell when a write cycle straightway followed by a read cycle completed on the cell results into flip of stored data but gives right data at output terminals. It may range from a decade read to the second read operation.
- Incorrect Read Fault: AnIncorrect Read fault occur in a cell when a read cycle completed on the cell does not flip data value but gives wrong data at the output.

III. Proposed Prediscarged Feeble Cell Detection Method

For the analysis of ROD on SRAM cells,a wide range of values are kept of resistive defects from 0 ohm to Tera ohm through infinity. Different locations considered for defects is as shown in figure earlier. Different combinations of write and read operations are performed ona cell forthe detection of faults in a cell at different positions. The proposed method is based on cell undergoes stress by predischargedbitline for fault detection. If the cell is fault-free, it can sustain with predischargedbitline stress and maintain stable data in a cell. The cell can restore data in consecutive read or write operations. But when resistive defect present inside a cell, the cell becomes unable to store data and data may get flipped depending on strength of resistive defect. For weak resistive defect, fault gets detected for longer predischargedbitline stress. Whereas if the value of resistive defect is larger, it can easily get detected with shorter duration stress. For resistive open defect, a current flowing through that terminal gets weaker and easily detection circuit can detect faults in memory. The type of model for each defect location is also observed by applying a cycle of write followed by consecutive read operations. The range of resistive open defects for different models is observed. Bridging defects are also analyzed for different locations in the cell. Previous methods for the detection of faults incur higher area overhead and latency. Some of which require complex timing

circuitry [19]. So it is required to develop the fault detection circuit which can detect the faults with less time latency and area overhead.

The different types of resistive open defects that can occur in memory have seen earlier. Each cell can have 23 possible locations of the resistive defect as shown in Fig. 2. The count will be more with short defects and bridging defects. So it is necessary to detect all these kind of faults in memory for smooth and reliable operation of devices. In the proposed method, Predischarged feeble cell detection, bitlines are predischarged to a specific level with the help of a predischarge circuit as shown in Fig. 3. Cell to be tested undergoes stress given by voltage available on the bitlines. Following the read cycle and wordline activation are used to sense the faults in the memory. Due to the presence of a fault in the cell, data may get flipped during a read or during wordline stress depending on the strength of resistive open defect. The method is stressed for the weak resistive defect faults in memory. The design of the schematic of the SRAM cell and its peripherals are verified with the simulations with access time obtained is 300ps. Fig. 4 showsthe simulation results of the defect at the source of the PMOS device.

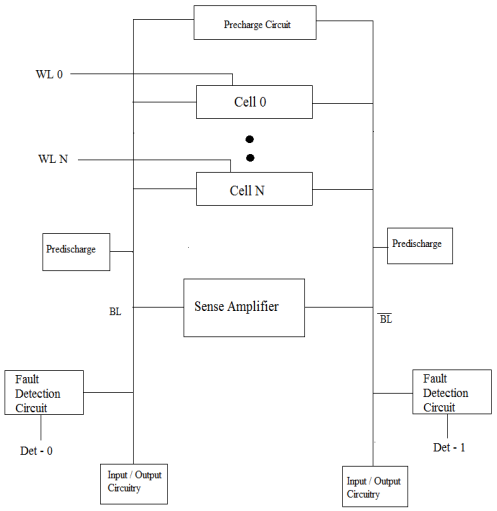

Fig. 3. Block Diagram of Predischarged Feeble Cell Detection

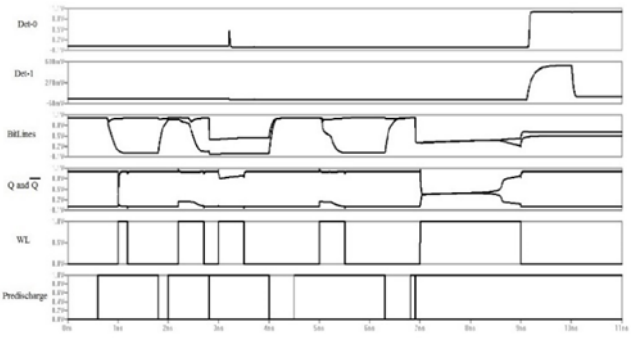

Fig. 4. Simulation Results of Resistive Defect at PMOS Source

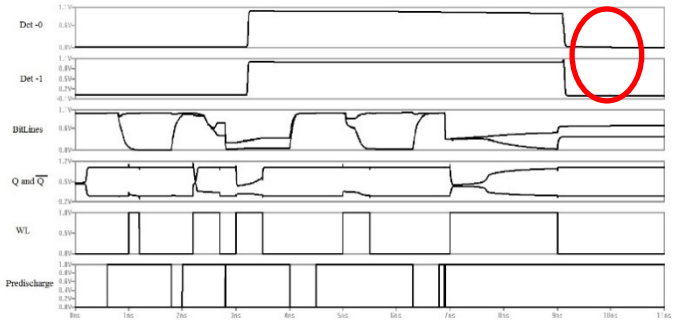

Fig. 5. Simulation Waveform of Resistive Defect at NMOS Source

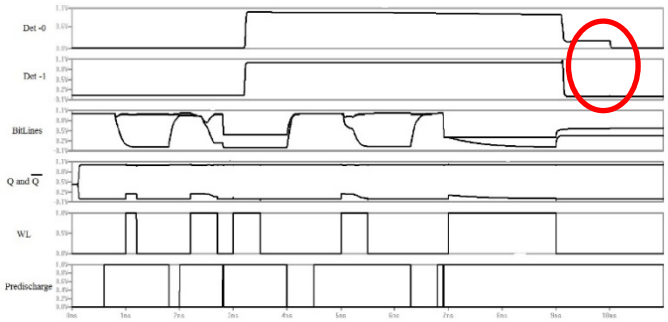

Fig. 6. Simulation Waveform of Resistive Defect at Gate of Access Transistor

The fault is indicated by the Det-0 which is the output of the fault detection circuit. Fig. 5 shows the defect present at the source of the NMOS device. Fig. 6 indicates an open defect present at the gate of an access transistor. The fault detection circuit compares data written onto a cell with data read from the cell after the stress is given to the cell. If a difference occurs, it will immediately be indicated. Given predischargedwordline (WL) stress on the

cell, if resistive defect present in a cell, the current flowing through the transistor will not be sufficient enough to hold the state of a cell. For weak resistive defects, it is difficult to detect only on the basis of current detection. The proposed method shows improvement in the values of weak resistive defects. Earlier detection of faults before becoming high values of defects helps to increase the reliability of devices or applications in which memory is used. The layout of the proposed method is as shown in Fig 7. Data on bitlines are read and then compared for the detection of faults in the memory cells.

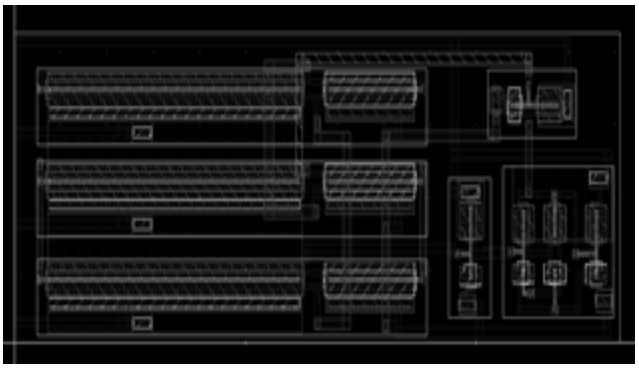

Fig. 7. The layout of Resistive Fault Detection Circuit

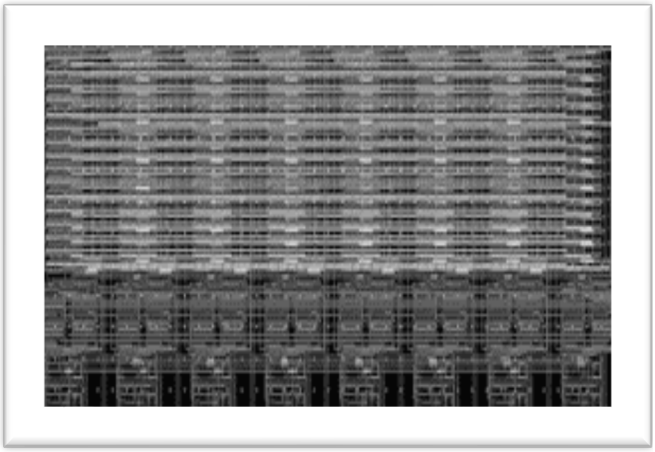

Fig. 8. The layout of 64X8 SRAM Memory Structure

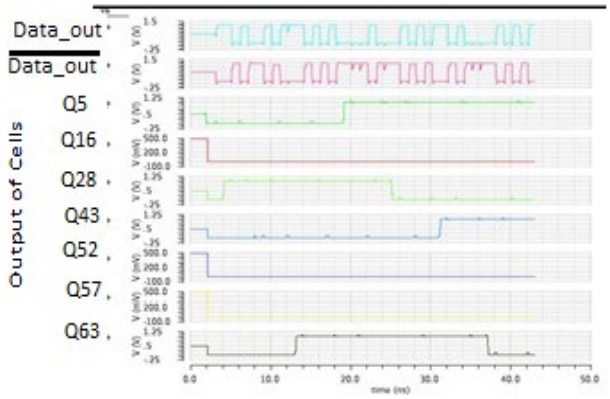

Fig. 9. Simulation Waveform of SRAM Schematic for Normal Read and Write Cycles

IV. Performance Analysis

The case study of SRAM 1KB memory cells has been developed. For checking the feasibility of the proposed method, simulations are performed on two levels viz. schematic and layout. The peripheral circuits required such as the precharge circuit, sense amplifier, input/output circuit are also designed required for adequate operation of memory structure. The location of faults is considered as shown in Fig. 2.

A. The memory of 64X8 Cells

The validation of proposed predischarged feeble cell detection (PDFCD) has been performed on the schematic level first. One redundant cell is added at top of each column. TheSRAM memory structure is designedfor 1 KB of cells in the spice tool. There are 1K memory cells in a column and such 8 columns are formed. Redundant elements are added at the top in the designed memorywhich will be used for the redundancy mechanism. If any row is found as faulty, it can be substituted by the redundant one. The results of fault detection are verified through simulation. Later, for layout 64X8 memory array is designed in the Cadence virtuoso tool using 45nm technology as shown in Fig. 8. Designed schematic and layout is verified for normal read and

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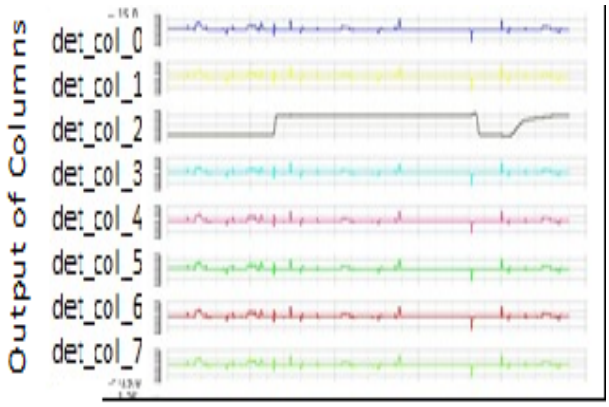

Fig. 10. Simulation Results of Layout of 64X8 SRAM

write operation with attached fault detection circuit for optimized access time as shown in Fig. 9. Simulations are performed with parasitic elements taking into consideration. It is observed that access time mainly depends on the capacitive load on bitlines. Parasitic elements increase the capacitive load on bitlines. Therefore a number of cells in a column are restricted for obtaining optimum access time. The simulations performed for multiple writes and read operations as shown in Fig. 8. The access time observed was 300ps. Initially, faults were introduced at the column level for detection. Hard to detect fault at the source terminal of load transistor which caused stability fault in a cell, is also getting detected by the proposed method for a weak resistive open defect. Similarly weak resistive open defect is detected at the drain terminal of load, source and drain terminal of the access transistor and driver transistor as well. Comparatively high values of the resistive open defect are getting detected at gate terminals of all devices since a reduction in gate current due to weak resistive open defect does not have much effect on the normal operation of the cell. As well as weak resistive open defect faults are detected by the proposed method at Vdd and Gnd terminals of the device. Resistive open defect at the wordline terminal is also detected. Schematic is extended at a byte level structure. Faults are randomly generated in different columns at random locations. Simulation waveforms are verified for all random resistive defect faults in memory at different positions in columns. It is also verified that the attached predischarged feeble cell detection circuit does not hamper the normal operation of the memory. Non-defective cells are also verified at different column level in memory.

B. The layout of Memory 64X8 Cells

Simulation results got through schematic should be verified at the layout level as well. Since in schematic, there is a null effect of parasitic components. However,in layout,the role of parasitic parameters is of utmost importance. The effect of parasitic elements hamper the read and write time as well as the performance of the system. Hence results of the layout are important to validate the proposed method. SRAM of 64X8 number of cells is taken as a case study for layout. For performance upgradation, the level of the column is kept at 64. With this structure considering the effect of parasitic elements, the access time observed is 310ps. As shown in Fig. 8, the layout of memory consists of all peripheral devices including the proposed predischarged feeble cell detection circuit. Similar to schematic resistive defect faults are detected at column level with all possible locations as shown in Fig. 2. It is assured that the effect of the attached PDFCD circuit should not affect the normal operation of SRAM. Later faults are generated at random locations in the memory structure. The simulation waveforms are verified for all possible locations of fault at random locations in memory. No-fault locations are also verified through simulations. The fault present in column 2 at load transistor getting detected in the simulation waveform as shown in Fig. 10.

V. RESULTS

In earlier sections simulation waveform of detection of resistive open defect fault at all possible 23 locations are discussed. The design of memory with peripheral circuitry, fault detection circuit and simulation is performed on 45nm technology in Cadence Virtuoso suit. As shown in Table I, with

the help of proposed predischarged feeble cell detection, weak resistive open defects can be detected at lower values. Resistive defect values for which circuit able to detect has improved. Hard to detect resistive defect at the source terminal of load transistor is also getting detected at 1.5Kohm compared to other techniques. Resistive open defect value at the source terminal of access and driver transistor, as well as drain terminal of the access transistor, are also improved compared to hardware-based approach, wordline underdrive, and IDDT method. The defect value at the wordline terminal is improved compared to wordline underdrive. Table II indicates performance analysis comparison with state of art methods. As shown test time latency is very less compared to other approaches. As well as area overhead achieved with the proposed method is too less compared to other methods. Predischarged feeble cell detection shows an overall improvement in resistive defect values with lesser time latency and minimum area overhead.

TABLE I
MINIMUM DETECTABLE DEFECT SIZE

Defect Location	[19] 2019 WLUD	[18] 2018 NBTI	[14] 2016 HBA	Proposed PDFCD
Source-Load (Ω)	119M	> 2M	16.3M	**1.5K**
Source – Driver (Ω)	214K	73K	6K	**4K**
Source – Access (Ω)	86K	90K	6K	**1.8K**
Drain – Access (Ω)	597K	120K	6K	**3K**
WL (Ω)	3.1M	660K	110K	**2M**

TABLE II
PERFORMANCE PARAMETERS

Defects	[19] 2019	[18] 2018	[14] 2016	Proposed PDFCD
	WLUD	NBTI	HBA	
Test Time	High	> 0.205ms	0.14ms	**20.48µs**
Area Overhead	High	--------	5.46%	**3.874%**

VI. CONCLUSION

With the help of the proposed idea of Predischarged Feeble Cell Detection, the ROD in the cells of memory array would be exactly located and weak resistive defect values are improved. The short and bridging defects are also get detected. The dynamic read destructive fault in memory cell get detected by a combination of read and write cycles on the memory cell. The method will have no effect on the performance of the circuit under test. The circuit implementation gives minimum area overhead of 3.87% and less latency period of 20.48µs for 1KB of memory.

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