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Performance Analysis of Combinatorial Circuits Using Complementary and Pseudo NMOS Logic

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Abstract
This paper describes area optimized combinational circuit design using complex logic structures. Domino and Dynamic CMOS logic circuits are imperative as it offers has reduced latency and lesser number of transistor requirements as compared to conventional complementary CMOS based logic circuits. The pseudo NMOS logic-based circuit proposed methodology yields less dynamic power consumption and less gate count, compared to the static CMOS circuit. Tribulations allied with Pseudo NMOS logic like it slows rise time and static power dissipation. The results show the comparison of combinational circuits like multiplexer designed in complementary, pseudo NMOS and Dynamic CMOS Logic in terms of area. Circuit Implementation of the combinational circuit has been done in DSCH 2.0 and layout part is implemented in Microwind EDA tools using CMOS 250nm Technology file.

Keywords – *CombinationalLogic,CCL,PNL,4:1 Multiplexer,DSCH,Microwind*

I. INTRODUCTION

Complementary CMOS logic is the simplest logic for implementation of any logic functions. Area overhead and power dissipation are the main concern for this logic structure. Pseudo NMOS logic is the complex logic structure is used whenever area is concerned. In proposed logic structure, as PMOS transistor is always connected to groundhence it is constantly ON which results into power dissipation. An important application of the combinational circuits is they played a vital role in designing of blocks like Arithmetic Logic Unit. Many digital signals processing application also required the basic building blocks like multiplexers, decoders and Demultiplexer. Adders and subtractor are also the basic building modules of many digital signals processing applications.

All these basic blocks can be designed using various complex logic structures.

The digital circuits are categorized into two types as shown in Figure 1.

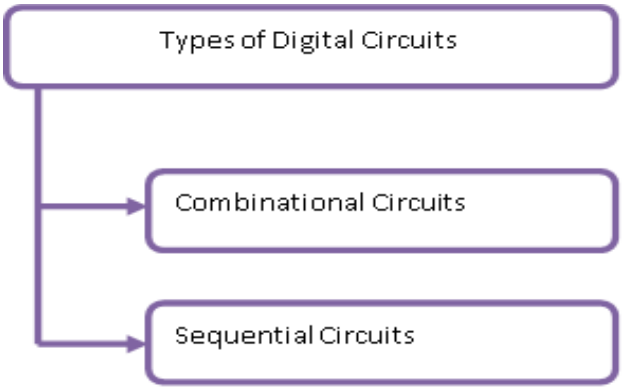

Fig. 1. Types of Circuits

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II. PREVIOUS WORK

The main complex logic structures consist of many styles which are decided by taking into consideration of the design parameter such as area, power or delay. The complex logic structure mainly categorized in five different types as shown in figure 2.

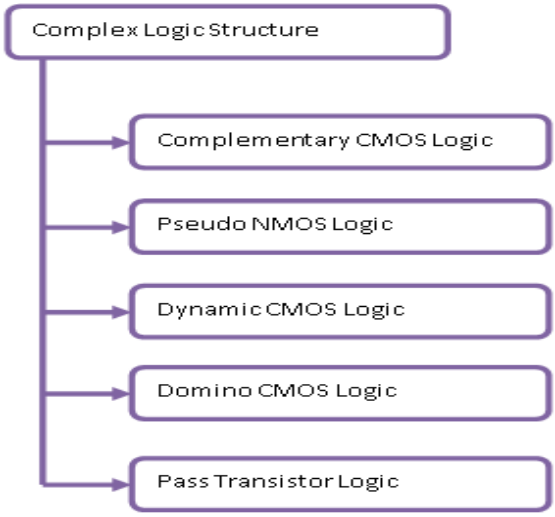

Fig. 2. Complex Logic Structures

There are various complex logic structures [1][2] which are selected on the basis of parameters like power or area.Complementary CMOS Logic is easy to implement but as far as area is concerned, this logic family is not considered. The superiority of Pseudo NMOS logic is area optimization. Pseudo NMOS based implementing the design requires less number of transistors as compared to other complex logic structures[3][4].The major disadvantage of Pseudo NMOS logic is power dissipation. This is because the pull up Transistor i.e., PMOS transistor is Grounded. Since low potential is required to ON the PMOS transistor, it is always ON [5][6]. So power dissipation is the vital issue while dealing with the Pseudo NMOS logic. Dynamic CMOS Logic is a very good option for power consideration. This is because extra constraint is provided by Clock[7]. In Precharged phase, all the inputs are provided and only in Evaluate phase, output is measured. But, again, delay is the main concerned for these types of families.

III. COMPLEX LOGIC STRUCTURES

A. *Complementory CMOS Logic*

The figure 3displays a generic n-input logic structure. The input_1, input_2 … input_nare provided to both PMOS and NMOS Logic Network. The Pull up Network (PUN) is implemented using PMOS devices, while Pull down Network (PDN) consists of NMOS transistors. Thebenefits of Complementary CMOS Logic are outputs are well defined and they do not demand Periodic signals for refreshing the voltage of nodes. The main disadvantage of Complementary CMOS Logic based design isit tax a greater number of transistors to design a module.

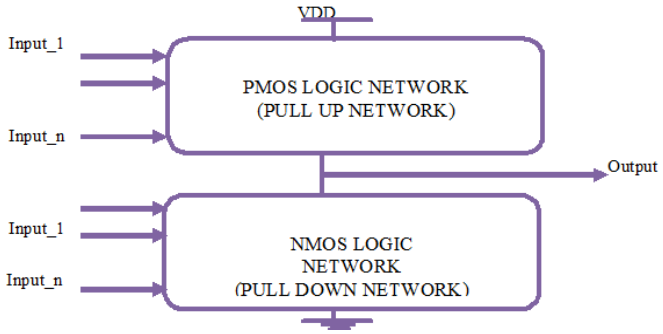

Fig. 3. Generic Architecture of Complementory CMOS Logic

B. *Pseudo NMOS Logic*

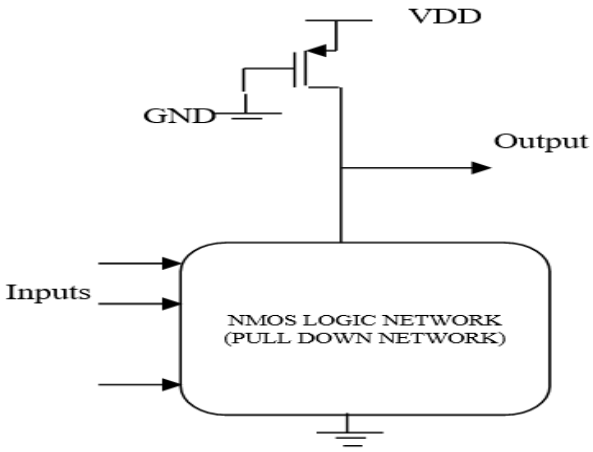

Fig. 4. Generic Architecture of Pseudo NMOS Logic

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It is solitary technique to diminish the gate count . PMOS Logic Network is connected to ground;as a result, it is ON constantly. The generic architecture of pseudo NMOS logic is shown in figure 4. The key motivation to reduce this width is to get better speed. The main purpose of PMOS pull up network is to provide qualified path in between supply voltage VDD and output, provided NMOS is put off. Pseudo NMOS logic is also known as ratioed logic. Pseudo NMOS logic is significant over other CMOS based design methods due to higher packing density and less silicon area. The main drawback of Pseudo NMOS Logics static power dissipation.

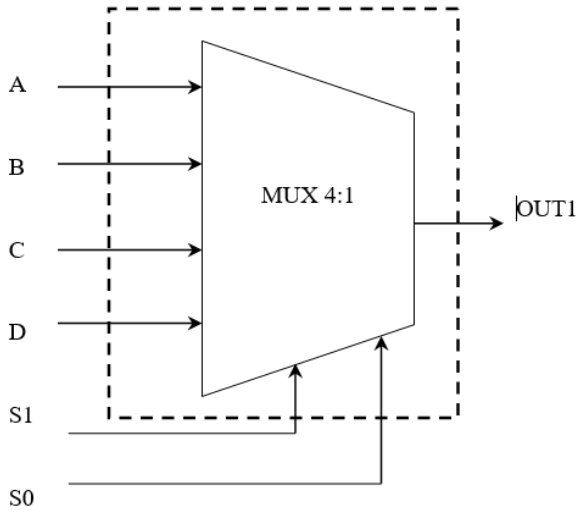

Fig. 5. Block Diagram of 4:1 MUX

IV. SIMULATION AND RESULT ANALYSIS

In this paper two combinational circuits are simulated using DSCH 2.0 EDA tool and the layouts were drawn by Microwind Layout Tool.

A. 4:1 Multiplexer

The combination digital design of 4:1 mux as shown in figure 5 is implemented using pseudo NMOS logic and its results are illustrated in figure 6 to figure 11.

The laout of 4:1 mux schematic is designed using DSCS tool and it shown in fifure 6. This schematic is designed as 4 inputs , two select lines and a output. The conditions on select input S0 and S1 are selecting one of the input and it is refected on output out2. This simulation results of complementry CMOS based 4:1 mux is shoen in figure 7.

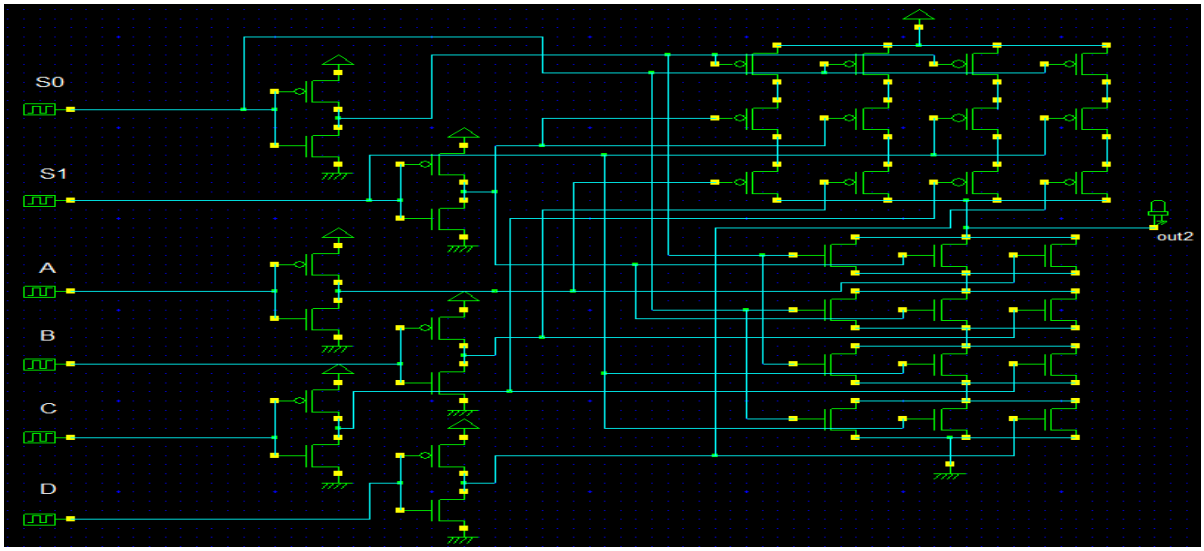

Fig. 6. Complementory CMOS based Schematic of 4:1 Multiplexer

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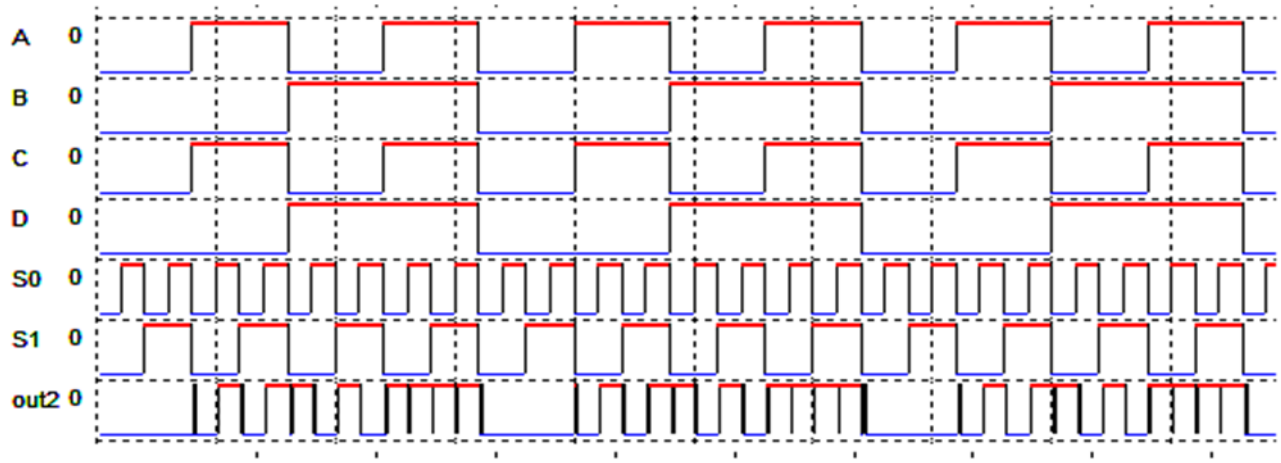

Fig. 7. Timing Waveforms 4:1 Mux

The schematic design of 4:1 multiplexer is completed using schematic entry tool. The top level diagram of the 4:1 multiplexer is as shown in Figure 5 and its resultant layout is illustrated in figure 8.

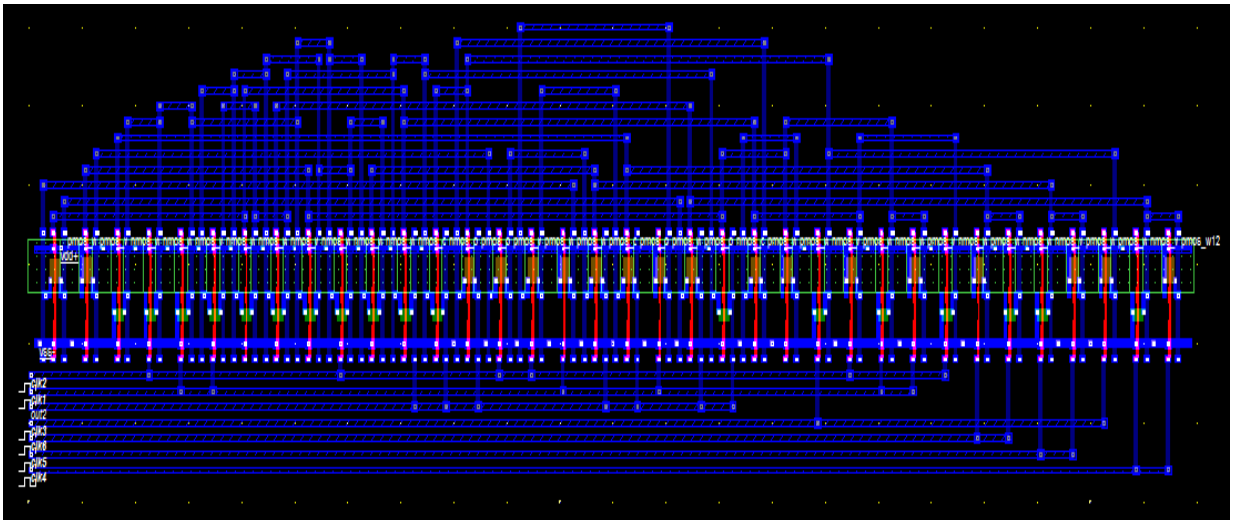

Fig. 8. Layout of 4:1 Multiplexer using Complimentary CMOS Logic

To compare results over prposed pseudo NMOS based combinational digial logic design over convential complementary CMOS based design, we designed 4:1 mux by proposed method as shoen in figure 9. The layout of pseudo NMOS based 4:1 mux is shown in figure 10. Even by visually comapring Figure 6 and figure 9, the compemenatary CMOS based 4.1 mux requires 36 gates where as pseudo NMOS based 4.1 mux mux design requires just 25 gates. On similar line 16:1 mux deign is compared where complementary CMOS needed 180 gates and pseudo CMOS baed 16:1 mux design takes only 125 gates. These reults are tabulated in table I. Thus, pseudo NMOS based design saves area drastically in both multimplexer design. This ideology is confiremd by implementing 2:4 decoder and 4:16 decoder using both complementary CMOS and pseudo NMOS . The results are compared and shoen in table II.

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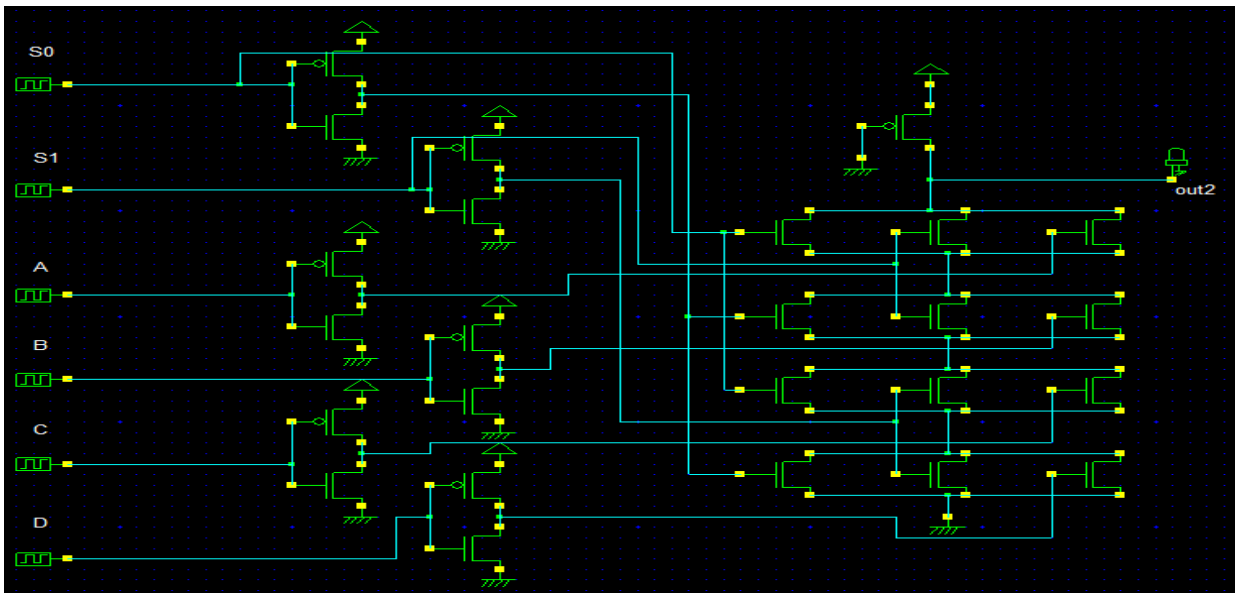

Fig. 9. Proposed Psedo NMOS based 4:1 mux Schematic

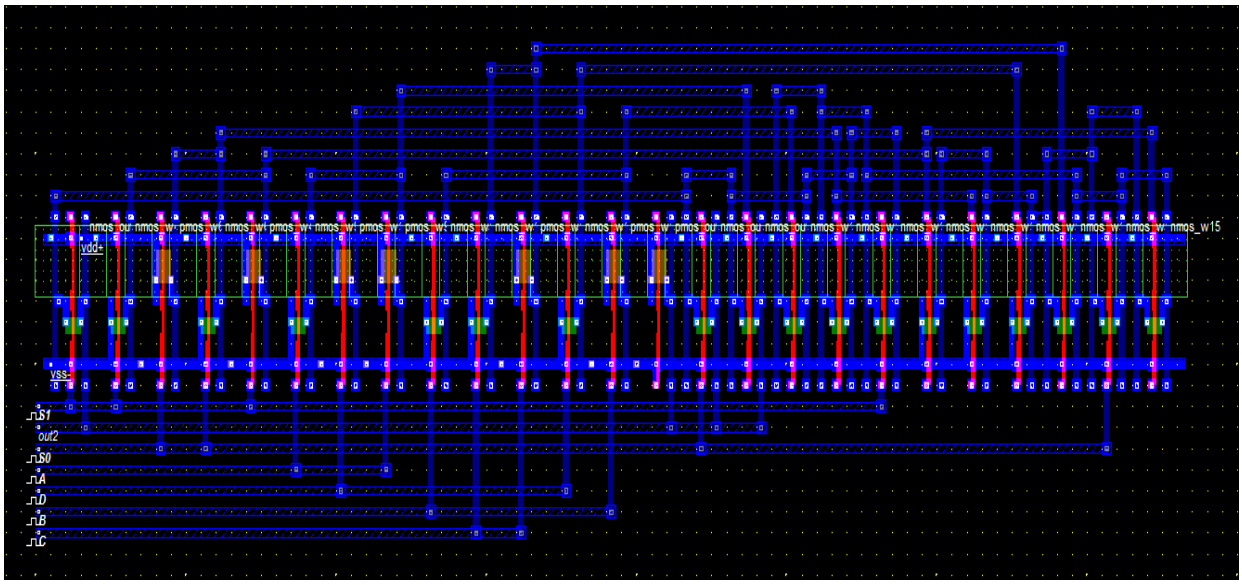

Fig. 10. Proposed Psedo NMOS based 4:1 mux Layout

TABLE I. AREA ANALYSIS-PART1 FOR MULTIPLEXER

Features	Area Analysis (In terms of Gate Count)		Power Analysis (uWatt)	
Complex logic Structures	***4:1 Multiplexer***	***16:1 Multiplexer***	***4:1 Multiplexer***	***16:1 Multiplexer***
Complementary CMOS Logic	36	180	5.12	12.08
Pseudo NMOS Logic	25	125	4.65	8.26

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TABLE II. AREA ANALYSIS-PART2 FOR DECODER

Features	Area Analysis (In terms of Gate Count)		Power Analysis (uWatt)	
Complex logic Structures	***2:4Decoder***	***4:16Decoder***	***2:4Decoder***	***4:16Decoder***
Complementary CMOS Logic	20	120	6.49	41.34
Pseudo NMOS Logic	16	96	8.26	36.47

V. CONCLUSION

In this paper, different CMOS logic structures such as Complementary CMOS and Dynamic CMOS logic isdescribed. A combinational circuit such as 16:1 Multiplexer and 4:16 Decoder are designed in various styles and the performance analysis was done on the basis oftransistor count. Among all the four technique, depending upon the specifications which are area, power and delay has been chosen. Comparative performance analysis of combinational circuits using Complementary CMOS and Pseudo NMOS Logic style has been carried out by this work. The simulation results clearly show the gate count differentiation of Pseudo NMOS Logic over Complementary. Reducing the gate count also reduces the silicon area. The proposed work in this paper will be helpful for circuit designer. It will also help designers to realize complex logic structure type of digital VLSI circuits.

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