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Hardware Implementation of Dedicated Squaring Circuit by Passing Multipliers

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Abstract
For more accuracy and easy way of obtaining output we use some basic mathematical operations. Squaring circuits are used in various semiconductor applications like FIR filters, binary calculators, animations, etc. Speed is a mandatory characteristic in squaring circuits. This mechanism of squaring circuit would improve device utilization. Basically, Design of squaring in electronic circuits are performed by multipliers. Thus no separate hardware for squaring circuits are used. In order to reduce the increasing composite of digital devices in multipliers, a separate squaring architecture is required. Also when using of multipliers it involves approximately a large number of gates and execution speed will be more. So we go for the novel and dedicated squaring circuit without using multipliers.

Keywords:Ripple carry adder(RCA), multiplexer, speed up, reduction in delay time, lessen logic elements.

1. Introduction

The technology transition from VLSI to Nano rates has termed for more composite action capabilities with quicker processing time and power usage. Some of the expansively popular VLSI signal processing devices include composite multiplication and power units; squaring units are some of the commonly used devices. Conventionally multipliers are utilized fordetect squares and higher levelfunctions. The conventional multiplier circuit need more power consumption and logic gates which consume more power.

This research proposes to develop a dedicated squaring device with squaring operation only, offering higher power consumption ascendancy and fewer gates.An activated unit would definitely work superior to a multiplier of specific purposes. Squaring process occurs most in applications such as cryptography, Euclidean distance calculation in graphics, FIRs and several other mathematical transformations etc.

The method of speed mathematics is in the field of simplifying most of the mathematical action capability into operations that can be defined as 10s, 100s and so on operations. As far as analysis process,effect ideally viewed by the entire VLSI signal handling field and is seen as successful in streamlining of intensity and computational speed of circuits and number of bits and low power consumes.

2. Motive

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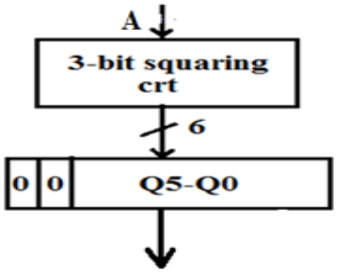
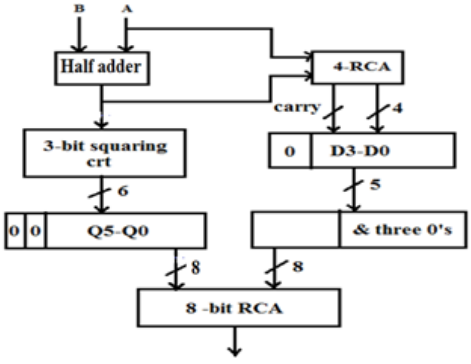
Squaring circuits has been widely used for mostfrantically operations in the field of signals and systems domain, in this work to analyze and finding the expedient of same.A higher version of this circuit will result in a better supervision of the device on its own in terms of power, location, speed. Conventional method requires the normal squaring multiplier as well as no unique dedicated circuit exists for the above. Multiplier for squaring also there is no particular committed circuit for the equivalent. All the present work condition was to update or structure squaring circuits using the algorithm of multiplication.

3. Proposed Work



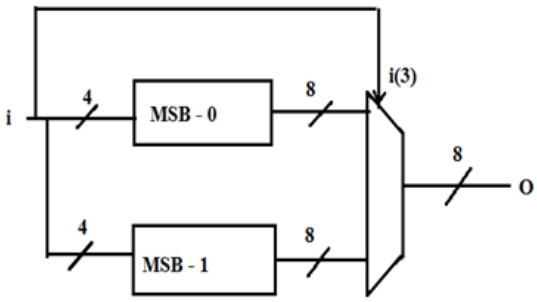
MSB - 0

Figure 1



MSB - 1

Figure 2



SQUARING - 4

Figure 3: Block Diagram of 4- Bit Squaring Circuit

4. Squaring Process

The process of this multiplication is that whatever the debt would subtract from the number and write alongside the debt. This may be impart to obtain squares of numbersnear to bases of powers of 10,100,1000 and so on.

Example-1: 92
Here we select, Base of 10
Then , debt =base – number = 10 – 9 = 1
Sq. of debt = 1^2= 1
A= Number – debt = 9-1 = 8
A alongside (Square of (debt)) = 8/1 = 81
Therefore, Square of the number = 81

Example-2: 962
Where we select, Base = 100
So, debt =base – number = 100 – 96 = 4
Sq. of debt = 4^2= 16

Figure 1
A= Number – debt = 96-4 = 92
A beside (Square of (debt)) = 92/16 = 9216
Hence, Square of the number = 9216

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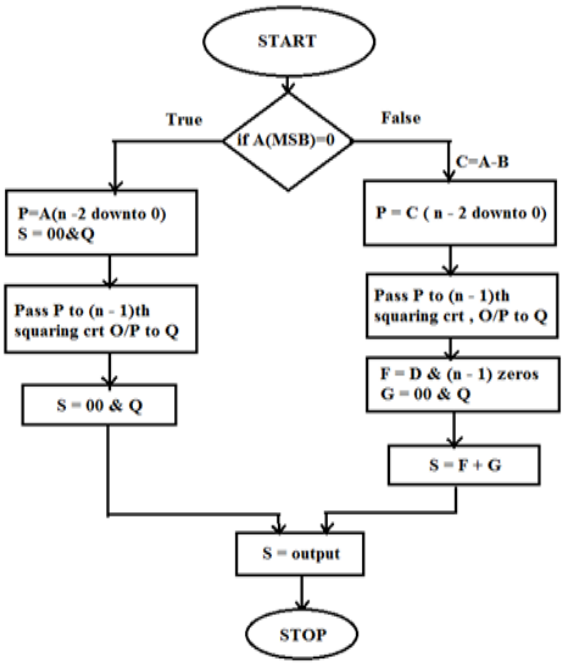

Figure 4: Flowchart of 4-Bit Squaring Circuit

5. Squaring in Binary System

For n bit squaring, the basis in binary is chosen as 2n-1 binary. For example3 bit number, it's 100. For 4 bit number it is 1000 and further. In this 4 bit squaring circuitry base is treatedas 1000. Binary numbers from 1000 to 1111 will be greater than or equal to base. While for squaring numbers between 0000 to 0111 that are less than base 1000, considering these numbers without considering its MSB that is already 0 can be considered as 3 bit number 000 to 111. So for computation of numbers below 1000 rather than using a 4 bit circuitry a three bit has implemented. Considering the squaring of debt in equation

- for e.g.,
  For binary number equal to 1001
  The base=1000 and
  The debt=0001.

By concatenating n-1 0s at LSB.In this work will use this two input AND gate and a half adder to search for a digital circuit for squaring of dual bit numbers.

Example:

1) A=1001
   B=1000
   C=0001
   D=01010

Checking A(2)=0
No, so implies P=001

So,
Q=000001
F=01010000
G=00000001
S=F+G=01010001

2) A=1111
   B=1000
   C=0111
   D=10110

Checking A(2)=0
YES, so implies P=111
So,
Q=110001
F=10110000
G=00110001
S=F+G=011100001

6. Results And Discussion

In the proposed study 2-bit to 4-bit squaring circuits are incorporated in VHDL. Logic synthesis and simulation are done in Quartus II. The result obtained and its relation with the findings currently achieved in State works. We achieve a result of the simulation as defined in figure 1 For circuit with 4-bit squaring.Table 1 presents the comparative analysis between that work and [1].So this study is measured to outperform in field, power, and time delay.

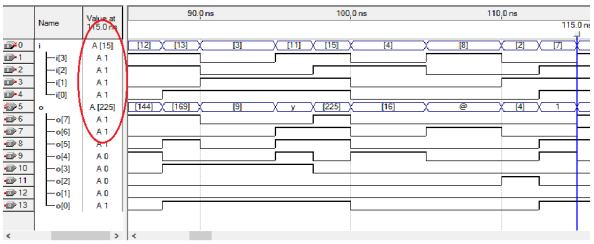

Figure 5: Simulated Output Waveform for 4- Bit Squaring Circuit

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Figure 6: Squaring Circuit hardware Implemnetation of 4-Bit

Table 1: Comparison Table

CONTENTS	EXISTING WORK	PROPOSED WORK
Logic elements	28	7
Pins	16	12
Delay	28.8ns	12.1ns

7. Conclusion

The adders used in existing type are ripple carry adder are the conventional type of adders, replacing them with a simple half adder circuit. But comparing with the conventional type of multiplier circuit this design of squaring is so optimize the area, cost & power consumption and it improve.

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