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A Competent Multiplier Architecture with Reduced Transistor Count for Radix -2 Butterfly Computation of Fast Fourier Transform

[1]Saravanakumar C, [2]Usha Bhanu N, [3]Themozhi G

[1]Department of ECE, SRM Valliammai Engineering College, Kattankulathur, Email: kanchi.saravana@gmail.com
[2]Department of ECE, SRM Valliammai Engineering College, Kattankulathur, India. Email: ushabhanu123@gmail.com
[3]Department of EEE, AMET University, Chennai, India. Email: gthemozhivijayakumar@gmail.com

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Abstract
Multiplication is the elementary process for computing the butterfly in Fast Fourier Transform. A formal multiplication task requires an extensively additonal hardware means and processing time in multiplication operation to a certain degree more than in addition and subtraction. In this work, architecture for multiplier is proposed which requires less space and works faster comparatively with other basic multiplier structures. The "UrdhvaTiryakbhyam" scheme offered by Vedic Mathematics is utilized to speed up the multiplication process. In addition, the reduction in transistor count is achieved by substrate biasing. Further the architecture is simulated in ORCAD software to analyse the area requirements of the Butterfly structure for computing Fast Fourier Transforms. The simulated results show that there is considerable reduction in transistor count and operating speed which makes the proposed multiplier a competent one with the standard multiplier architecture.

Keywords: *Butterfly structure, Multiplier, Substrate Biasing, Transistor count, UrdhyaTiryakbhyam.*

1. Introduction

A multiplier is one of the significant hardware blocks used remarkably in digital signal processing (DSP) systems. The Classical DSP applications where a multiplier encounters an invaluable role include digital filtering, digital communications and OFDM in major. Today's trendy DSP applications are exploited at convenient, free-style systems, so that power dissipation turns out to be the crucial design constraints. As adders are used for partial product generation, once the computation of multiplication increases the complexity of Adders gets increased considerable. So it is required to design a circuit which has better performance in terms of speed, size and power.

Hence we adopted two techniques, one to reduce the delay (which increases the speed) and the other to reduce the number of transistor used (to reduce the size of the circuit). Vedic Mathematics is used to compute multiplication of two numbers with reduced delay[1]. In order to reduce the transistor count in the design, we employed substrate biasing technique in MOSFET devices. Further to check the operating characteristics of the vedic multiplier with substrate biased MOSFETs[3] we utilized the radix 2 butterfly computation. For simplicity we considered the real valued logic.

In this paper we simulated the 2 x 2 bit multiplier employing the vedic multiplier based on UrdhvaTiryakbhyam sutra. The substrate biasing technique reduces the transistor count in a huge amount. The simulation is carried out in ORCAD PSPICE software to check the output of substrate biased transistors. To check the delay of the circuit, verilog programming is used and simulated with Xilinx ISE 13.These results are then verified for a butterfly structure which takes the basic element to compute Fast Fourier Transform.

2. Literature Survey

The vedic multiplier forms the basic unit for multiplication process. Being an ancient method, converting it to binary format will diminish the number of partial products as shown in [2].

The substrate biased adders require less number of transistors as compared to the CMOS logic as shown in [3].

March-April 2020
ISSN: 0193-4120 Page No. 1577 - 1581

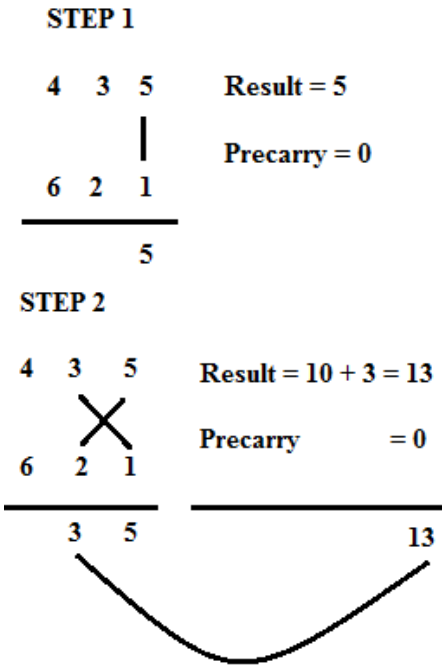
Rao et al. has shown in [4] that, in implementation of the Vedic multiplier, the time taken by the input to reach the output plays a tremendous role, as it will empower to decide on minimum delay architecture. When architecture with smallest path delay is selected, not only does it make the architecture quicker but it also makes it more stream lined among the other known architectures.

Kundu et al [5] suggested a newfangled technique to conclude the optimal moduli set that has been brought in and an efficacious RNS multiplier based on Wallace tree multiplier (for 32 bit arithmetic unit) for DSP applications is exhibited. The major drawback is higher power consumption.

Seo et al. [6] proposed a lucid architecture of multiplier-and-accumulator (MAC) for valuable speed operations. By bringing together multiplication with accumulation and constructing a combined type of carry save adder (CSA), the performance was improved.

3. Vedic Multiplication

An UrdhvaTiryakbhyam, a Vedic multiplication sutra, involves vertical and cross wise means to perform the multiplication of two numbers. The magnificent feature of this sutra is that it largely speeds up even when the numbers of bits are increased. The sutra is depicted in Fig.1a and 1b below by considering the multiplication of two decimal numbers 435 * 612.



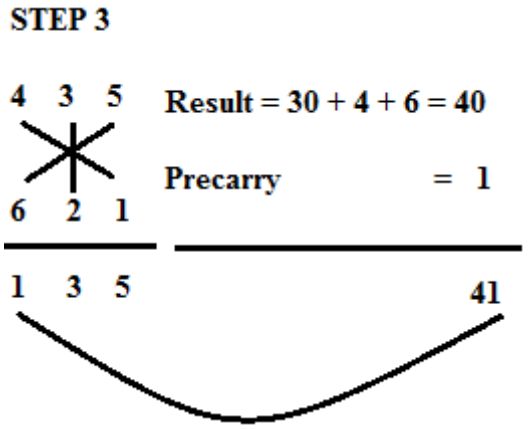


Figure 1a: Multiplication using UrdhvaTiryakbhyam Sutra

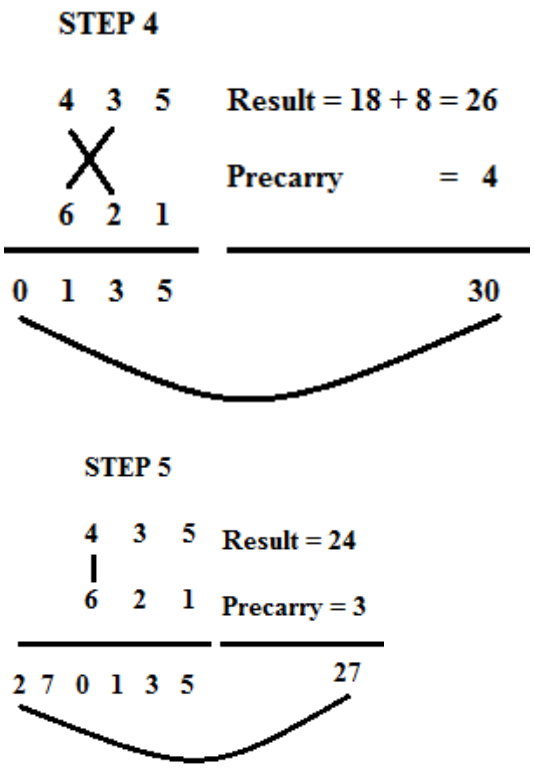


Figure 1b: Multiplication using UrdhvaTiryakbhyam Sutra

The above sutra is employed to compute multiplication of two numbers for signal processing applications. As we have to work for binary numbers, a slight change was made in the above algorithm.

Let us consider the two bit binary numbers be b1b0 and a1a0. The partial products generated with this example are a1b0 and a0b1 at level 2 and the carry generated from level 2 should be propagated to level 3 and added with another partial product a1b1.Thus the vedic multiplier reduces the number of arithmetic operations to be applied to the input values. The two bit binary vedic multiplier operation is depicted in Fig. 2.

March-April 2020
ISSN: 0193-4120 Page No. 1577 - 1581

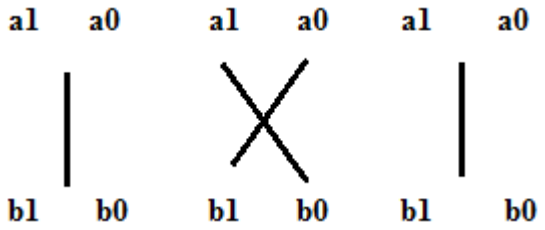


Figure 2: Generation of Partial products

With the above partial products, the multiplication is carried out as shown in the architecture below.

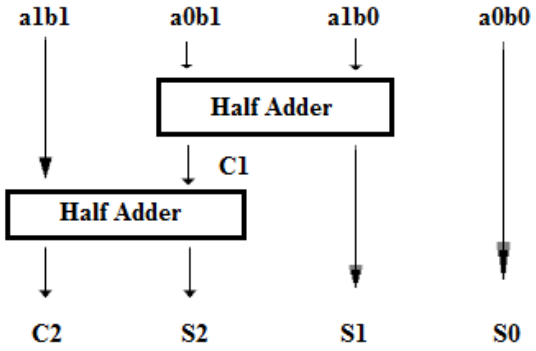


Figure 3: Vedic Multiplier Architecture

4. Substrate Biasing

Substrate biasing in PMOS biases the substrate of the MOS transistor to a voltage higher than Vdd. In case of a NMOS transistor the substrate of the MOS transistor is connected to a voltage lower than Vss. For illustration consider a Substrate biased inverter. The PMOS substrate is biased to the supply voltage Vdd, so that additional positive charge carriers are supplied to the n – type substrate. In this case, in contrast to a traditional CMOS circuit, the source is never be assigned to the body. It is not forward biased but it is again reverse biased p – n junction between source to body with an increased reverse supply. The Boolean equation for a substrate biased inverter can be given as

$$Out = (A.(B)') + (B.C) \quad (1)$$

Where B is the input to the inverter, A positive bias voltage, C negative bias voltage. The Out is the output signal from the inverter.

Further the other gates could be derived from this equation. As Multiplier is our case, it is required to design an AND gate and XOR gate. Equation (1) can be used to trace the expression for AND gate as

$$Out = (B.C) \quad (2)$$

The expression for XOR gate could be formulated as

$$Out = (A(B)')+(B.(A)') \quad (3)$$

the above equations it could be revealed that the number of transistors required to implement the “and” operation is 2 and “XOR” operation is 4. Thus the size of the multipliers and adders could be essentially reduced.

5. Results and Discussion

The Vedic multiplier is simulated with the Xilinx 13 software with Spartan 3E device. Verilog programming language is used to write the code for traditional multiplier and Vedic multiplier. Both the multipliers are executed with the same set of input to derive the critical delay. The synthesis report generated for this project shows that the Vedic multiplier has less path delay when compared to the traditional multiplier.

Table 1: Maximum Combinational Path Delay

Sl.No	Combinational Path delay	
	Traditional Multiplier	***Vedic Multiplier***
1	7ns	6.376ns

The substrate biased transistors are used to build the AND gate and XOR gate as they are required to compute multiplication and addition. The Vedic multiplier has less combinational path delay which implies that it operates fast in line with the traditional multiplier. So there is a requirement to compare the Vedic multiplier with substrate bias and without substrate bias. The simulation is carried out using ORCAD software as it should be done in device level. The output of the Vedic multiplier with substrate biased transistors is shown in Fig.4.

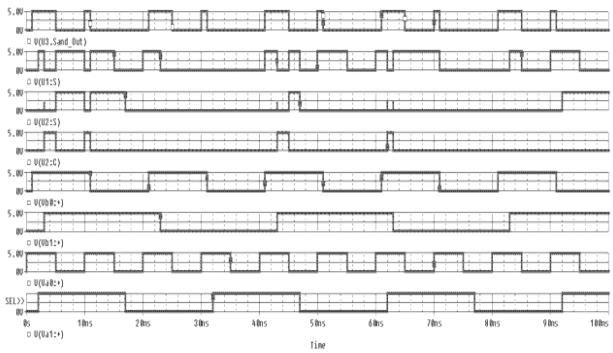


Figure 4: Simulated Output of Vedic Multiplier

The Table 2 is accumulated with the number of transistors used for a Vedic multiplier. The traditional Vedic multiplier uses totally 70 transistors whereas as the substrate biased ones requires only 20 transistors.

Table 2 : Transistor Count of Vedic Multiplier

Sl.No	Transistor Count of Vedic Multiplier	
	Without Substrate Bias	*With Substrate Bias*
1	70	20

Thus the size of the architecture could be reduced by employing substrate biasing technique.

March-April 2020
ISSN: 0193-4120 Page No. 1577 - 1581

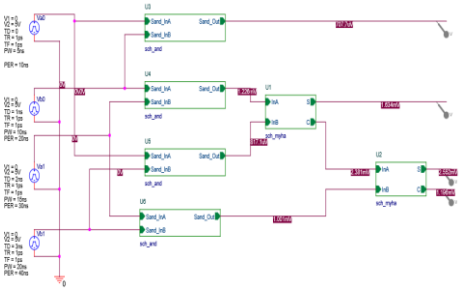


Figure 5: Block Diagram of Vedic Multiplier with Substrate Biasing

The Fig. 6 depicts the comparison of the traditional multiplier and Vedic multiplier in the dimension of path delay.

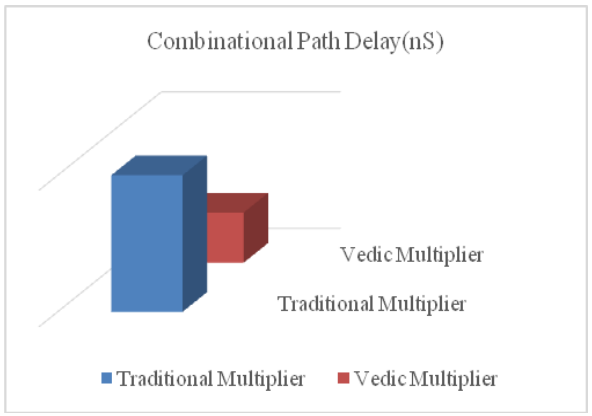


Figure 6: Comparison of Path delay

The Fig. 7 compares the transistors count with respect to Vedic multiplier with and without substrate biasing.

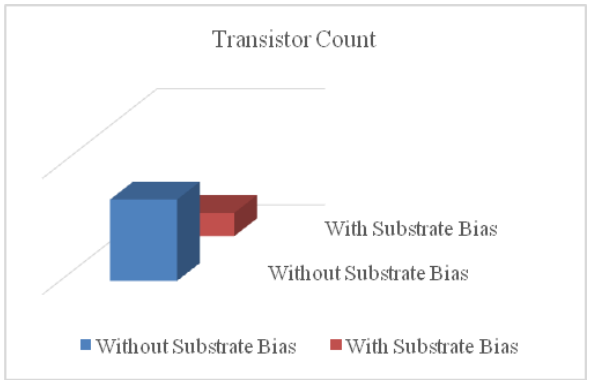


Figure 7: Comparison on Number of transistors used

Vedic Multiplier for radix 2 Butterfly

The butterfly structure is the basic building block to compute the Fast Fourier Transform. The computation requires adders and multipliers. The Vedic multiplier with substrate biased transistors are used to compute the butterfly structure as it has two folds, the fast operating multiplier and with reduced number of transistor count.

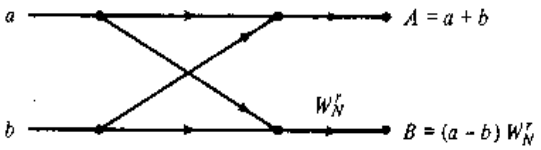


Figure 8: Radix -2 Butterfly Structure

6. Conclusion and Future scope

In this paper, a architecture for multiplier is presented which competes the other multiplier structures in speed as well as in size. Further this multiplier is utilized to compute the butterfly structure and the results are verified. This work reveals that the Vedic multiplication yields a faster operation and the substrate biasing techniques reduces the transistor count by 28%. In future this work could be developed to analyze in power reduction domain.

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Authors Profile

Saravanakumar C is pursuing his research in the Research centre, Department of ECE, SRM Valliammai Engineering College. He is a life member in IETE and ISTE. His research areas include VLSI and Signal Processing.

Usha Bhanu.N is working as Professor, Department of ECE, SRM Valliammai Engineering College. She has 20 years of experience and Her research areas are VLSI, Signal Processing and IOT application.

Themozhi G is working as a Professor, Department of EEE, AMET University, Chennai