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Implementation of Modified Low Power CMOS XOR Logic Gate using Reversible Logic

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Abstract
In modern VLSI technique, most of the adder design faces problems in four basic constraints namely power, chip area, speed and error occurrence, a modified hybrid VLSI adder 4T transistor design which integrates the logic of both Pseudo-NMOS and XOR Gate is proposed which is used to overcome the issues of accuracy, low speed and power consumption. This paper proposes a new design for 5-transistor CMOS-XOR gate which utilize less silicon area and consumes relatively lesser power than that of the existing 6-transistor and 12-transistor XOR gate designs and more accurate/good at output values when compared with the 4 and 3-transistor logics. The proposed XOR is used in full adders using Reversible gate Logic and its performance can be compared with the existing adders like conventional adder,Ripple carry Adder and Carry select Adder.This type of adders can be applied in the field of digital image processing and signal processing where importance is given to accuracy. The design will be implemented and simulated using CADENCE tool and performance will be tested. The proposed 5T full adder system using XOR logic has an accuracy of 99.988% and power consumption has reduced by more than 75%. Implementation of the 5T transistor adder using xor logic is done using the backend tool (CADENCE).

Keywords: *Front end, Back end, ETA, EDA. (EDA - Electronic Design Automation).*

1. Introduction

From the time since VLSI brought up a revolution in the electronics industry, there is a continuous effort from researchers and scholars to bring down the three major thingsin VLSI IC design, those are the silicon area, power consumption and delay in the transistors. Most of the works concentrated basicallyon reducing the size and number of transistor used in the design. We have designed a 5-transistor XOR gate and hence managed to bring down the transistor count which is nothing but the reduction in area, power consumption and delay in the circuit.

The importance given to the design of XOR gate is because of the fact that most of the systems constitutes of XOR circuits associated with other circuits. As in case of a full adder, random number generator etc., XOR gates plays a part. Hence the improvement of XOR's performance improves the performance of an adder subsystem and so on. For better observation of the output results, the gates can be connected to an adder and the performance of each can be compared.Most of the works concentrated basically on reducing the size and number of transistor used in the design. We have designed a 5-transistor XOR gate and hence managed to bring down the transistor count which is nothing but the reduction in area, power consumption and delay in the circuit.

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The XOR gates are most fundamental building blocks in various circuit especially-Arithmetic and logical gates operations like full adder, half Adder, Full Sub tractor, half Subtractor, incrementer, decrementer, multiplexer, multipliers, Compressors, Comparators, Parity Checkers, Code converters, Error-detecting or Error- correcting codes, and Phase detector

In our proposed design paper the XOR gate is compared with existing seven different logic design techniques i.e. Standard CMOS logic, PTL(Pass Transistor Logic) logic, CPL(complementary Pass Transistor Logic) logic, DPL (dual pass Transistor Logic) logic, GDI(Gate Diffusion Logic) logic and Domino logic. The performances of these techniques have been evaluated by CADENCEusing the 0.180nm CMOS technology.

2. Existing CMOS Design Techniques For XOR Gates

Static CMOS XOR gate

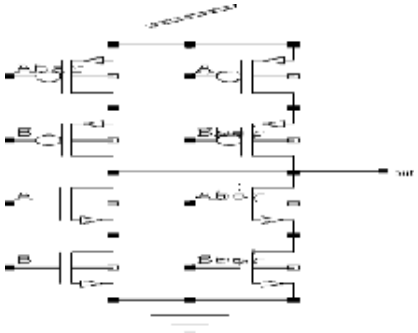

Figure 1: Static CMOS XOR GATE

Static CMOS(Complementary Metal oxide Semiconductor) logic XOR gate is designed by using serial and parallel combination of pull-up P-MOS Transistor network and pull down. NMOS Transistor network. The major Advantage of the Static CMOS logic xor Gate has a full swing voltage and there is no voltage drop to the Vth(thereshold Voltage). But major drawback it has more delay and it consumes more power and area. Because it is designed by serial and parallel combination of 4-PMOS and 4NMOS transistors. Static CMOS XOR gate is shown in Fig.1

PTL based XOR gates :-

In order to reduce the size and power they constructed the XOR gate by using PTL based logic. IN PTL logic the Source is connected with a input instead of Power supply voltage (VDD). And it requires any one combination of PMOS logic or NMOS logic to perform the XOR gate operation. The major adavantage of the PTL based XOR gate reduces the area by reducing the transistor count to four. But major drawback is it suffers in producing a full swing voltage. And it degrades the output voltage with respect to input and theres hold voltage (Vth). It has limited input driving capability.

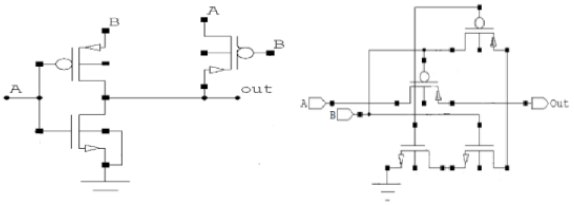

Figure 2: (a, b,) PTL XOR gates

CPL based XOR gate

In order to Resolve the supply issues like input voltage and supply voltage degradation, in later years they designed the XOR gate by using CPL(Complementary Pass transistor Logic) . In this logic they modified the entire circuit by using a combination of NMOS logic and CMOS inverter to construct a 6T XOR gate. The major advantage is it has small input capacitances because of Nmos-Logicand it produces good input and output driving capability. It is based on Pass transistor logic networks .but the combination of Nmos-logic and cmos Inverter it consumes more power when compared to previous logic and it is the major drawback of the CPL based XOR gate.

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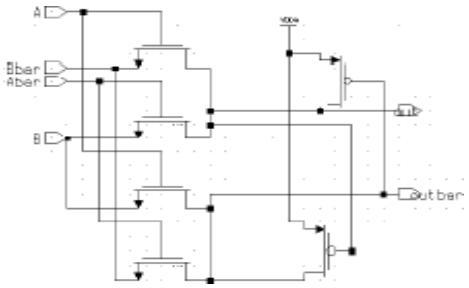
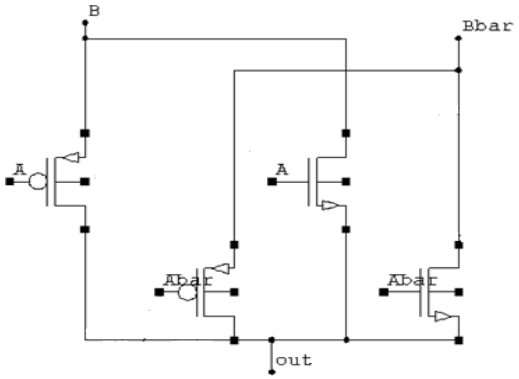


Figure 3: CPL XOR GATE

DPL XOR gates:

In order to resolve the number of transistors count ratio in previous logic .And to reduce the large short-circuit currents and higher wiring overhead problemthey started to design the XOR gate by using Double pass transistor logic. In this double pass transistor logic is a combination of NMOS and PMOS pass transistor logic. It reduces the number of transistors and more wiring overhead. It reduces the voltage drop problem across the Threshold voltage (Vth)and reduces the power. The major drawback it consumes more area because of PMOS pass transistor logic.



GDI based XOR gate

In order to resolve the power consumption consumed by PMOS pass transistor logic , they introduced a new technique called as Gate Diffusion Input logic. By using this both PMOS and NMOS will have a common gate input Terminal. it is a low power gate diffusion combination technique.

P terminal input to the source/drain of PMOS), and N terminal input to the source/drain of NMOS Logic.Bulks of both NMOS and PMOS are connected to N or P (respectively), simple GDI cell as shown in Fig6.

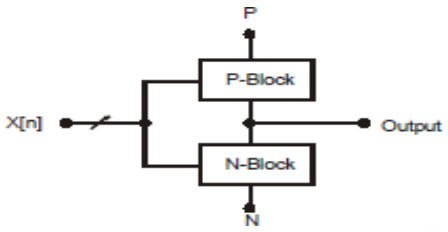


Figure 6: (n + 2) inputs GDI cell.

This GDI- XOR gate Cell technique will reduce power, propagation Delay and area. XOR gate using GDI logic is shown in Figure

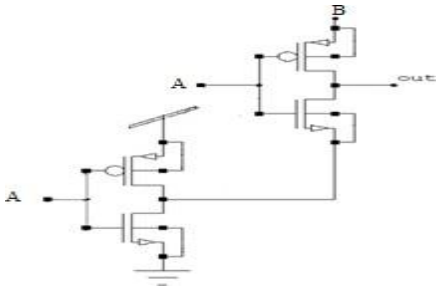


Figure 7: GDI XOR

Domino Logic based XOR-AND gate

The modified form of the above 12 transistors by reducing the number of inverters originally comes the reduced 8-transistor XOR gate structure which functions in a very similar fashion and produces nearly equal output values while reducing the silicon area. The 8transistor design using cmos transistor and its output performances are shown in figure. In domino Logic the output is connected with a cmos NOT gate. According to external inputs, during evaluation, the output of the inverter is restricted to only the transition form '0' to '1', but from logic '1' to '0' is never possible. So, when these logic blocks are cascaded, all input transistor in subsequent logic blocks will be turned off during the pre-charged phase, since all buffer outputs are equal to '0'. During the evaluation phase, each buffer output can make at most one transistor (0 to 1) and thus each input of all subsequent logic stages can also make at most one transition. XOR gates using Domino logic style are shown in Fig.8.

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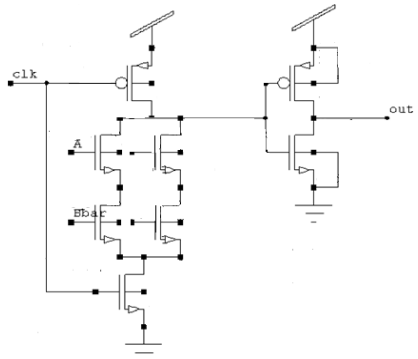
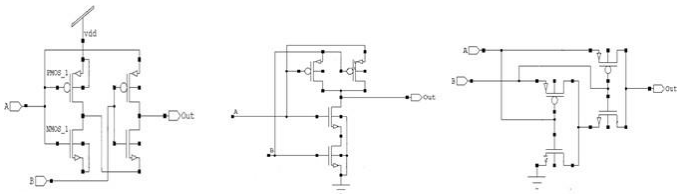


Figure 8 : Domino logic XOR gate

4-T XOR

In previous logic the XOR Gate is designed by using either 6Transistors or 8Transistors by using CMOS logic and DOMINO logic. In previos logic they find the pre charge and discharge problems faced in the DOMINO logic XOR gate. And later versions they have modified and reduced the transistor count by using Inverter logic. And they proposed a new design of 4Transistor - XOR gate. After the invension of 4Transistor based XOR gate they find the drawback that it could operate without requiring complementary inputs. And further they modified and they designed a new version of 4T –xor gate shown in fig 9.However, this XOR gates



consumed considerable silicon area for their optimum performance and but the power delay product is also large

Figure 9 (a, b, c): 4 Transistor XOR gate

Inverter based XOR Gate

Inverter based XOR gate is constructed by connecting two CMOS Inverter circuits and the output of the Cascaded two –cmos inverter is further connected to another one CMOS-inverter. The major drawback of this inverter based xor gate logic is it requires high power supply voltage to operate .it produces non-full voltage swing at all internal nodes.

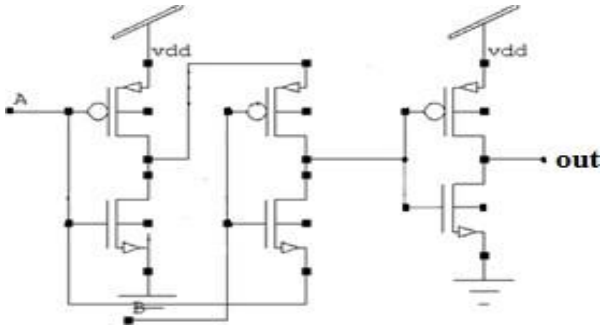


Figure 10. Inverter based XOR gate

PROPOSED DESIGN

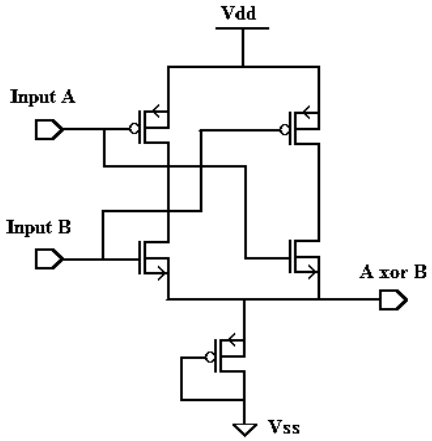
The proposed XOR design is a low power 5 transistor design, which uses 3pMOS and 2nMOS transistors. The inputs are fed to both pmos and nmos placed alternatively and between a pair forming a pseudo inverter.

The XOR logic canbe explained by thisexpression,

A+B = AB'+BA'

When both the inputs are high, both the inputs go OFF not letting the Vdd pass to the output through the nmos, though they are ready to conduct. And when both of them are low, then both the nmos go OFF making theoutput stay at logic zero.

But when the inputs are alternative, then either of the path from Vdd to Vss stays closed making the output go logic high. The schematic of this XOR is shown in Fig.11.



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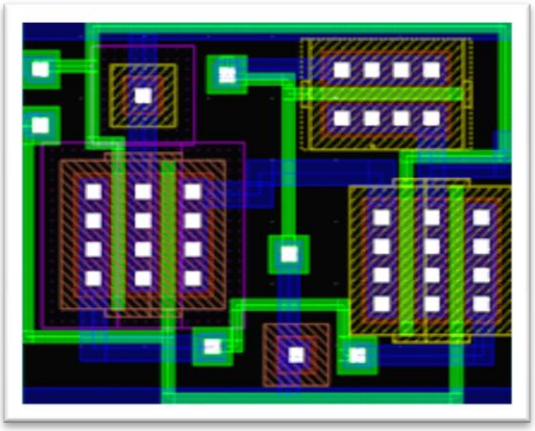

the output go logic high. The schematic of this XOR is shown in Fig.11.

Most of the other works carried out before mainly concentrated in silicon chip area reduction and power consumption. Though such designs are optimal for use in several applications, there were some problems with the output accuracy as most of the low transistor designs (3, 4 and 6-transistor cmos XOR) produced bad values at the output for some input combinations. Three transistor design produced a bad '0' (i.e., output attained a value that neared 1) when both inputs are kept logically high '1'.

Few low transistor XOR gate found in the literature are designed and simulated using 0.18µm technology and when the results are compared, the proposed design produced better results even with low excitation voltages in the range of 0.6v to 1.2v.

Also the logic designed using low power pass transistor logic and CPL (Complementary Pass transistor Logic) produced inaccurate output values for some input combinations especially when both the inputs are high.

This is due to the pass transistors feeding the part of the input into the output. Even double pass transistor logic produced bad output value for a few input combinations. With acceptable silicon area utilization and minimal power consumption the proposed XOR is better than other logics and applicable in many areas.

3. Simulation Results and Comparison

Various design techniques for XOR gate are compared based on the performance parameters like propagation delay, power dissipation. The simulation results for the existing conventional design and the proposed XOR designs are shown here. As explained with various other designs so far, this paper has one of the best circuit for an XOR gate and with all the simulations done in TSMC 0.18µm technology with voltage ranging from a mere 0.6v to 3.6 volts. For all the values, the proposed design proved to be good with more than good results. The layout in fig. shows the minimum area required by the proposed design, which is lesser when compared with previous designs of XOR gates.

Waveform outputs for the two designs are shown below.

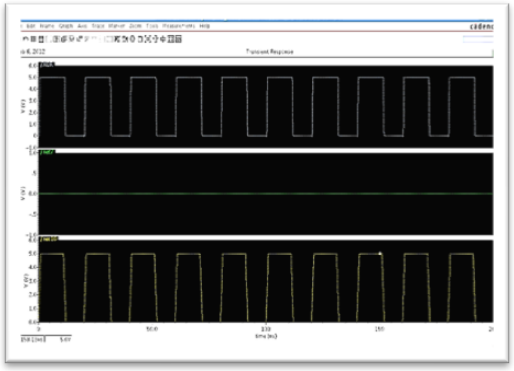

Figure 12 Simulation results of the proposed XOR gate

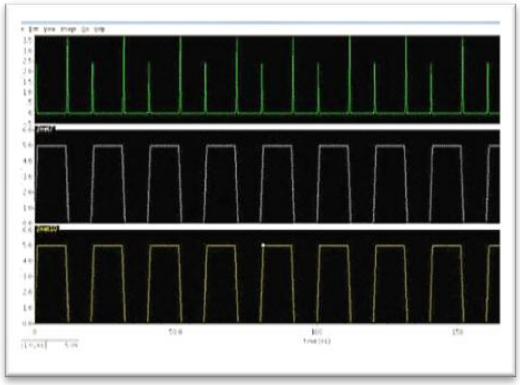

Figure 13. Simulation results of the proposed XOR gate

4. Chip Area Needed by the Proposed 5-Transistor XOR Gate

With just 5 transistors making the entire circuit that has 3 pmos and 2 nmos transistors, the

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area required is much smaller to that of the conventional 12 and 8 transistor designs. The area of the entire chip has reduced by around 65%, meaning that two XOR circuits at the cost of one's area.

When considering the designs with even lesser transistors as in case of a four transistor XOR, this is slightly bigger but still good with accurate output values when compared with those designs.

The silicon area required for the proposed design done with CADENCE layout environment is shown below.

Table 1: Comparative performance of various type of XOR gate using 0.90 nm technology

Sl. No.	Logic Styles	Transistor count	Delay (ns)	Power Consumed (nw)
1	PTL	4	76.121	298.79
2	CPL	6	24.85	469.84
3	DPL	4	26.559	10.766
4	GDI	4	26.612	460.58
5	Domino	8	54.11	239.33
6	4-T XOR	4	53.915	280.69
7	Inverter based	6	26.098	148.39
8	Proposed 5T XOR gate	5	0.6	6.02

Table 2: Comparative performance of various type of XOR gate using 0.18 um technology

S.NO	Logic Styles	No of Transistor	Delay(ns)
1	Static- CMOS logic	12	0.0725
2	Domino Logic	8	0.0695
3	Inverter based logic	6	0.0681
4	Proposed 5T XOR gate	5	0.0662

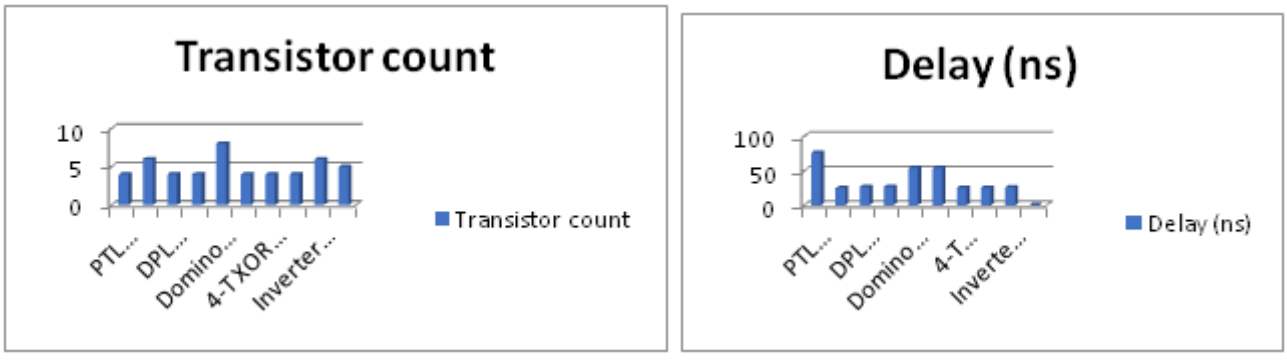

Fig.14: Comparison of various CMOS XOR Gate logic versus Transistor count , delay and Avg. power consumption in 90 nm technology .

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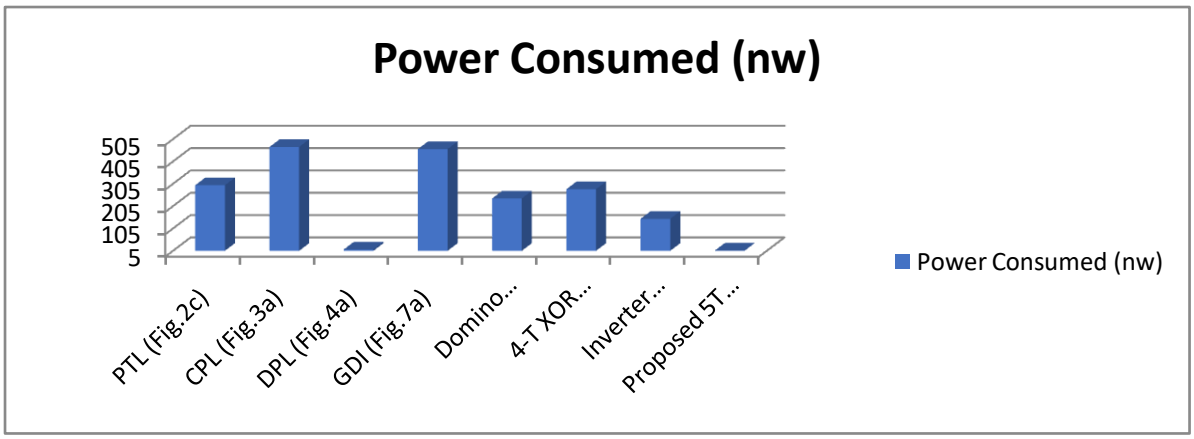
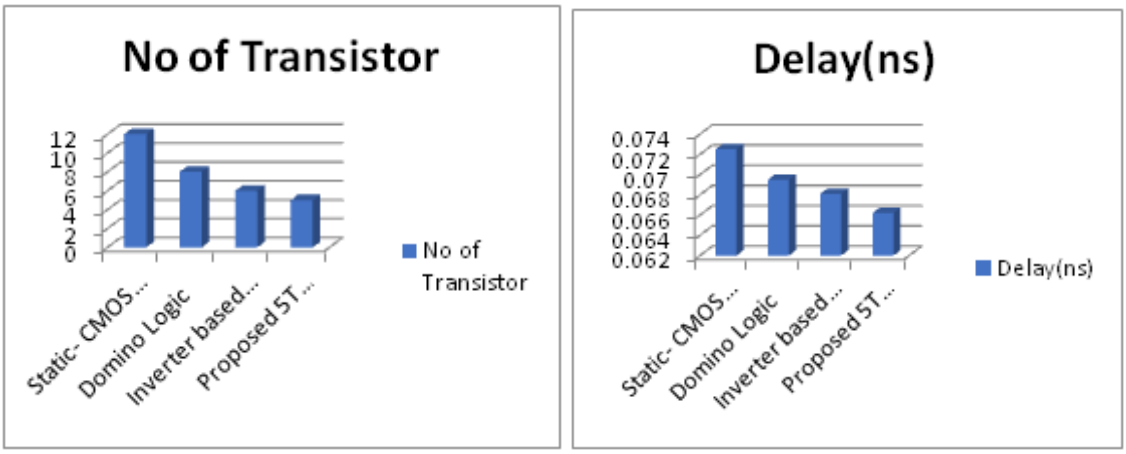


Figure 15: Comparison of various CMOS XOR Gate logic versus Transistor count, delay USING 0.18nm Technology having supply voltage.



Future Work :

PERES GATE: It is a 3*3 reversible gate i.e., it has three inputs and three outputs. The representation of Peres gate is shown below. Quantum cost of this gate is 4.

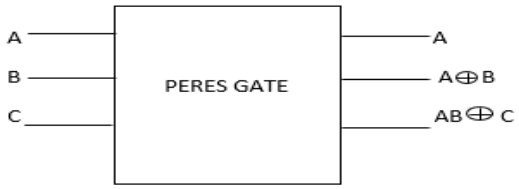


Figure 16: Peres gate.

Peres gate is one of the popular gate and used in many applications.

TOFFOLI GATE: It is a 3*3 reversible gate i.e., it has three inputs and three outputs. The representation of Toffile gate is shown below. Quantum cost of this gate is 5.

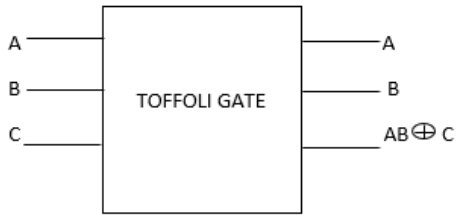


Figure 17: Toffoli gate.

BME GATE:

It is a 4*4 reversible gate i.e., it has four inputs and four outputs. The representation of BME gate is shown below. The quantum cost of this gate is 6.

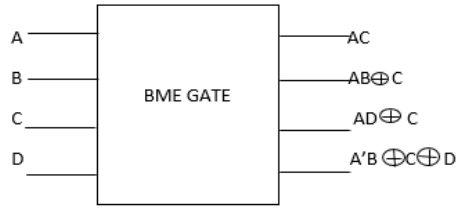


Figure 18: BME gate.

In future the proposed 5 Transistor XOR gate can be used in the reversible gate and by using this we can design the Vedic Multiplier circuit using Reversible logic gates.

5. Conclusion and Future Work

As explained with various other designs so far, this paper has one of the best circuit for an XOR gate and with all the simulations done in Cadence TSMC 0.18µm technology with voltage ranging from a mere 0.6v to 3.6 volts. For all the values, the proposed design proved to be good with more than good results. The layout in fig. shows the minimum area required by the proposed design, which is lesser when compared with previous designs of XOR gates.

As an extension of this work, we are going to implement the proposed design in a modified adder (yet to be proposed), and compare its performance and size with existing adder architectures.

References

[1] Design of High Speed low power Multiplier using Reversible Logic: Rakshith T.R.2013.

[2] G Ganesh Kumar and V Charishma, Design ofhigh speed vedic multiplier using Vedic mathematics techniques, ltn'l J. of Scientific and Research Publications, Vol. 2 Issue 3 March.

[3] M S Islam, M M Rahman, Z Begum and M Z Hafiz, 2009. Low Cost Quantum Realization of Reversible Multiplier Circuit. Information Technology Journal, vol. 8(2), pp. 208-213.

[4] Harpreet Singh Dhillon and AbhijitMithra "A Digital MultiplierArchitecture using Urdhva Tiryakbhyam Sutra of Vedic Mathematics" IEEE Conference Proceedings,2008.

[5] D. MASLOV, G. W. DUECK, AND D. M.MILLER, Synthesis of Fredkin-Toffoli Reversible Networks, IEEE Trans. VLSI Systems, 13(6), pp. 765769, 2005.

[6] P. D. Chidgupkar and M. T. Karad, "The Implementation of Vedic Algorithms in Digital Signal Processing", Global J, vol. 8, no.2, pp. 153-158, 2004.

[7] Monika Rangari et.al Design of reversible logic ALU using reversible logic gates with low delay profile international journal of advanced research in computer and communication engineering. Vol.4 issue 4. April 2015.

[8] Arokiaraj, D. (2015). A Study on Environmental Responsibility of the Stakeholders of Auto Industry in Chennai (Doctoral dissertation).

[9] Arokiaraj David (2020), "Corporate & Individual Environmental Responsibility towards Automobile" BRivers Publisher, ISBN: 978-93-88727-94-5, pp.01-194.

[10] David, A., & Banumathi, M. (2015). A Study on the Environmental Concern of the Passenger Car User in Chennai. International Research Journal of Business and Management (IRJBM), ISSN, 2322, 083X.

[11] David, A., & Banumathi, M. (2014a). A Study on Eco-Driving Behaviour of Passenger Car Users in Chennai. TIJ's Research Journal of Social Science & Management (RJSSM), 3(11).

[12] David, A., & Banumathi, M. (2014b). Factors Influencing the Purchase Decision of Passenger Cars in Puducherry. International Journal of Exclusive Management Research (IJEMR), ISSN, 2249-2585.

[13] David, A., Nagarjuna, K., Mohammed, M., & Sundar, J., (2019). Determinant Factors of Environmental Responsibility for the Passenger Car Users. International Journal of Innovative Technology and Exploring Engineering, ISSN: 2278-3075, 9(01), 210-224.

[14] David, A., & Ravi, S. (2017). The direness of cultivable land spotted on agricultural: A special reference to rice production in South India. Abhinav National Monthly Refereed Journal of Research in Commerce & Management, ISSN-2277-1166, 6(09), 55-59.

[15] David, A., Ravi, S., & Reena, R. A. (2018). The Eco-Driving Behaviour: A Strategic Way to Control Tailpipe Emission. International Journal of Engineering & Technology, 7(3.3), 21-25.

[16] David, A., Thangavel, Y. D., & Sankriti, (2019) R. Recover, Recycle and Reuse: An Efficient Way to

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ISSN: 0193-4120 Page No. 89 - 98

Reduce the Waste, International Journal of Mechanical and Production Engineering Research and Development, ISSN (P): 2249-6890; ISSN (E): 2249-8001, 9(3), 31-42.

[17] Green, W. B., & Thompson, C. (2016). U.S. Patent No. 9,390,625. Washington, DC: U.S. Patent and Trademark Office.

[18] Lagassey, P. J. (2008). U.S. Patent No. 7,348,895. Washington, DC: U.S. Patent and Trademark Office.

[19] Mazidi, M. A., Mazidi, J. G., & Mckinlay, R. D. (2000). The 8051 microcontroller and embedded systems. New Delhi.

[20] Mimar, T. (2016). U.S. Patent No. 9,491,420. Washington, DC: U.S. Patent and Trademark Office.

[21] P. Pratheepkumar, J. Josephine Sharmila & D. Arokiaraj, (2017) "Towards Mobile Opportunistic in Cloud Computing" Indian Journal of Scientific Research (IJSR), ISSN, 0976-2876.

[22] Ravi, S., David, A., & Imaduddin, M. (2018). Controlling & Calibrating Vehicle-Related Issues Using RFID Technology. International Journal of Mechanical and Production Engineering Research and Development, 8(2), 1125-1132.

[23] Ruikar, M. (2013). National statistics of road traffic accidents in India. Journal of Orthopedics, Traumatology and Rehabilitation, 6(1), 1.

AUTHORS PROFILE

Mrs. G Jyothi received B.Tech degree in Electronics and Instrumentation Engineering from Aurora's Engineering College, Bhongir, Telangana, M.Tech.inElectronics and Communication Engineering from IASE, Rajasthan. Published 9 journal publications and more than 30 conference publications.Having 15 years of teaching experience, out of which one year as Associate Professor and Head of the Department ECE, ASTRA, 3 Years as Associate Professor, Department of ECE, ASTRA and 9 Years Assistant Professor, Department of ECE, SSIT, Tumakuru. Now Currently working as Associate Professorin the Department of ECE, ASTRA, Hyderabad, Telangana.

Life Member of Indian Society of Technical Education (ISTE),Received Best Faculty Award in the Department of ECE ,ASTRA. Received Class B Award Certificate for Task Based Trainingall over Telangana region conducted by e-yantra IIT Bombay in the field of Embedded systems and Robotics. Received Merit & Winner Award Certificate for Task based Training in Teacher Competition Challenges Round conducted by e-yantra IIT Bombay.Received appreciation certificate from e-yantra, IIT Bombay for successful completion of Teacher completion in challenge round. Successfully completed Pedagogical Skills Development Training for Engineering College Teachers and Advanced Pedagogical Skills Development Training for Engineering College Teachers, conducted byTEQIP Cell-SSIT in Association with SPFU, Karnataka.

Her Research areas include Reversible Logic Design, Low power VLSI Design, Digital VLSI Design and Digital Electronics. Her research topic is Advanced techniques for designing 16 Bit Arithmetic Logic Unit using Reversible logic gates.

Dr. M. Suresh currently working as a professor in the Department of Electronics and communication Engineering, SSCIT, and Tumkur Karnataka. He is having totally twenty six years of Academic Experience. Out of that seventeen years he worked as Visvesvaraya Technological University Co-ordinator, He worked as a Head of the department for six months and five years he worked as a Warden In charge. He is a University Evaluation/ Paper setting member in the following various subjects such as DSP, ADSP, Analog and Digital Communications, Microprocessors and Microcontrollers. He is the Editorial Member in

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various International journals. He has total six publications in various Referred Journals. He conducted two days workshop on Analog and Digital IC design using cadence tool and entrepreneurship Awareness camp in the academic year 2016 and 2017. He presented and published four papers in international Conferences in the area of bio medical signal Processing. Involved in the Initialization and setting of Labs for the use of students & staff. He Involved in the student welfare and discipline as the member of College Anti-ragging Committee and Student counseling in the department in the form of staff adviser to students. He is the Member, Board of Studies in Electronics & Communication Engineering dept, Bangalore University. He is Life Member of Indian Society of Technical Education (ISTE) and Institution of Electronics and Telecommunication Engineers (I.E.T.E). His Research areas include Reversible Logic Design, Low power VLSI Design, Digital VLSI Design and Digital Electronics.

Dr. Sunil Belladi has earned a PhD in Development Communication from Dept. of Journalism and Mass Communication, Osmania University. He has more than 13 years of experience in teaching both at Post Graduate and Under Graduate level and five years of industry experience in Print and Electronic Media.

His areas of interest are Communication theories and Media Research. His research focus is on Social Change and Developmental Communication and Cultural Studies and he has presented several papers at national and international conferences. He is also empaneled as Course Writer at Dr. B R Ambedkar Open University, Hyderabad for Modules on Mass Communication.

His PhD thesis on ‘Community Radio as an agent of social change – a comparative study of Sangam and NammaDhwani’ set out to locate Community Radio in Indian context, and its practices based on the conceptual framework of Brazilian Educationist, Paulo Freire and his ideas of Conscientization and Praxis. Civil Societies in India have championed the cause of Community Radio and the study was directed to make a comparison of two CRSs, namely Namma Dhwani and Sangam CRSs operating in the state of Karnataka and Telangana and their role as agents of social change.

Sunil has an MPhil from Osmania University. His thesis ICTs In Governance focused on the eGovernance initiative by the Government of Andhra Pradesh, especially in the G2C services. It was reiterated through the study that although ICT can be a tool for decentralization, integration across departments, reduction in workload, efficiency and effective in service delivery, it cannot be the sole instrument of change