

Ambiguity Sets Determination for Fault Diagnosis of Analog and Mixed Signal Circuits

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Abstract

A Simple Binary Classifier for finding ambiguity sets or elements and potentially faulty components in analog and mixed signal circuit under test (CUT) is proposed in this paper. Node Voltages are used as features for classification. The classification criteria is based on the Euclidean distance, threshold and score metrics of the features. Threshold value for classification is estimated based on the performance metric, F1 Score of the binary classifier. Two benchmark CUTs, second order LPF and an 8-bit Digital to Analog Converter are used to evaluate the performance of the binary classifier used.

Keywords: *Fault diagnosis, analog circuits, mixed signal circuits, binary classifier, ambiguity sets.*

I. INTRODUCTION

Fault Diagnosis in Analog and Mixed Signal Circuits is to find the faulty conditions and elements of the circuit under test. It is essential in both design verification at production level and maintenance of the performance. Fault diagnosis methods are categorized as simulation before testing and simulation after testing. Simulation before testing methods are Fault Dictionary approaches and simulation after testing methods are based on set of diagnostic equations. Faults are grouped as parametric and hard. Parametric faults are due to loading effect, ageing of components and improper operating condition. They result in performance degradation of the CUT. Hard faults are modelled as open circuit and short circuit faults. These result in complete performance down of the CUT. The challenges in fault diagnosis procedure are potential faults identification, tolerance limits of the components, measurement accuracy and precision, accessibility for measuring features, etc. In this paper, methods are proposed to identify the potential faults in the CUT. Potential faults are the faulty conditions which can be classified distinguishably. Artificial Intelligence and hierarchical approach for

finding ambiguity groups and fault diagnosis is proposed in [1]. Self organized maps and Random Forest techniques are used to groups ambiguity elements to make fault diagnosis a simple. A simple simulation before technique is used in [2] to find faults in electronic circuits. Walsh-Hadamard transforms are used to extract cut-off frequency and phase shift at a frequency point. Multiple regression and genetic algorithm are used to estimate the relation mathematically between tested values and components. Integer coded faulty dictionary approach is used in [3]. The ambiguity sets are found and are assigned an integer in constructing the fault dictionary. Both time domain and frequency domain features used to locate faults. Fault detection methods require test nodes for extracting features such as node voltages or currents for detecting faults. Number of test nodes selection also importance in reducing fault dictionary size and to reduce computational cost. Test node selection based on similarity coefficient estimation is performed in [4]. This similarity coefficient is used as an fault isolation degree in finding different fault conditions of the CUT. Clustering to group ambiguity elements are done in [5]. K-means algorithm is implemented for each components of

the CUT. To improve test node selection process, a method based on multiobjective optimization is used in [6]. In [7], genetic algorithm combined with tabu search is used to find suitable minimum number of nodes for testing. Support Vector Machines are used to classify different fault conditions. QR factorization technique [8] to solve ambiguity sets identification problem in poor testable circuits. Symbolic analysis of CUT is used to build diagnostic equations for testing. Multifrequency testing is another interesting approach of fault detection in electronic circuits. Sensitivity estimate is used to find ambiguity sets in [9]. Ambiguity sets are collected at various test frequencies. Optimal test nodes selection based on entropy calculation is proposed in [10]. Node voltages for the applied sinusoidal input are measured at various test nodes and ambiguity sets are separated for fault diagnosis.

The proposed approach uses a simple binary classifier for grouping ambiguity elements based on node voltages as features and as an alternate approach to the existing techniques. Test nodes to measure node voltages are assumed as accessible for performing measurements. Chapter 2 of this paper explains the proposed system block and work flow. Chapter 3 explains the method of choosing the threshold voltage for estimating the score for ambiguity grouping. Experimental results are explained and discussed in chapter 4 and chapter 5 concludes the proposed work highlighting the specialities.

II. AMBIGUITY SETS GROUPING

The proposed work flow starts from simulating the CUT using Multisim for the measurements under fault free and faulty conditions. With the measurements made on the selected nodes, fault dictionary is constructed. Binary classification is performed by calculating the Euclidean distance of all rows, threshold estimation and score metrics. This is illustrated in the block diagram given below. (Fig.1)

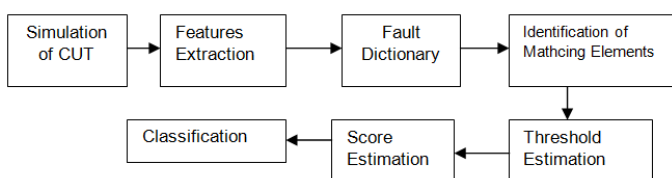


Fig. 1. Ambiguity Sets Grouping

CUT is simulated using Multisim. All the resistors in the CUT are considered to have 5% tolerance, all capacitors are with 1% tolerance and ICs are assumed as fault free. Faults are injected and the CUT is simulated by considering single and multiple parameteric and hard faults. A fault ID (F1 ,F2...) is assigned to each faulty condition and the node voltages are recorded to construct fault dictionary. A suitable stimuli (AC or DC) is applied with appropriate magnitude and frequency. Fault dictionary of the CUT consists of faulty conditions (fault ID) as row elements and node voltages called features as column elements. Ambiguity sets separation is done by calculating the Euclidean distance value of all rows in the fault dictionary to find matching rows or elements. Ambiguity set is defined as the group of faulty conditions which cannot be classified or identified uniquely. Hence this affects the fault diagnosis procedure. Therefore the purpose of finding ambiguity sets to separate the circuit faulty conditions which are uniquely detectable. Threshold value estimation is explained in chapter 3. Based on the threshold value and the distance value estimated a score value is obtained and incremented based on the criterion. Based on the score value estimated the faulty conditions are classified as ambiguity or unambiguity sets. The unambiguity sets are treated as potential faulty elements of the CUT. Classification in data analysis is to group data into single or multiple categories based on a set of characteristics or criteria. Classification problem is viewed as binary and multiple classification. Multiple classification involves more number of classes whereas binary classification involves only two categories. Generally multiple classification methods are based on the use of multiple binary classifiers.

2.1 Flow Diagram

Figure 2 explains the above mentioned method. For the input fault dictionary (of size $m \times n$), initial threshold and score values are set as zero. For each row, the matching with other row is found by Euclidean Distance (ED) measure.

$$ED = \sqrt{\sum_{j=1}^n (x_j - P_j)^2} \quad (2.1)$$

where x_i and P_j are the features. i, j are the pointers to point the rows of fault dictionary.

2.2 Classification Criteria

Threshold value for classification is estimated from the simulated and practically simulated data. The score value is incremented for $ED > \text{Threshold}$ and if the obtained score is equal to number of columns in the faulty dictionary, then the fault dictionary data belongs to ambiguity set. This procedure has been repeated for all the rows of the fault dictionary.

III. THRESHOLD ESTIMATION AND VALIDATION

Threshold for classification is estimated by finding the difference between simulated data and practically simulated data. Practically simulated data are obtained by connecting the CUT on breadboard and injecting faults into it. This is done to compensate for measurement and precision errors. It has been found that this value is in between 0 to 2 for the CUTs used for testing. The estimated threshold value is validated using the performance metric of binary classifier, F1 score. It is calculated from the precision and recall measures of classification.

$$F_1 \text{ Score} = \frac{2(PR)}{P+R} \quad (3.1)$$

where

$$\text{Precision}(P) = \frac{\text{TruePositive}(TP)}{\text{TruePositive}(TP) + \text{FalsePositive}(FP)} \quad (3.2)$$

$$\text{Recall}(R) = \frac{\text{TruePositive}(TP)}{\text{TruePositive}(TP) + \text{FalseNegative}(FN)} \quad (3.3)$$

True Positive (TP) is defined as number of correct classification as potential fault. True Negative (TN) is defined as number correct classification as ambiguity set.

False Positive (FP) is defined as error of classifying a fault as ambiguity when it is not and False Negative (FN) is the error of classifying a fault as potential fault when it is not. Threshold value for which F1 score is the highest is considered as threshold for grouping.

IV. RESULTS AND DISCUSSION

The proposed method of ambiguity sets grouping is evaluated on two bench mark circuits, second order filter and an eight bit digital to analog converter.

The threshold range for both circuits is obtained as 0 to 2 as explained in chapter 3.

4.1 Second order LPF

The second order LPF is shown in figure 3 with component values. N1, N2, N3, N4 and N5 are the circuit nodes. Since N3 and N4 gives same potential variation due to virtual ground, node 4 is not a test node. The test nodes are N2, N3 and N5. Simulation is performed for 140 faulty conditions on the nodes 2,3 and 5 and fault dictionary is built as above.

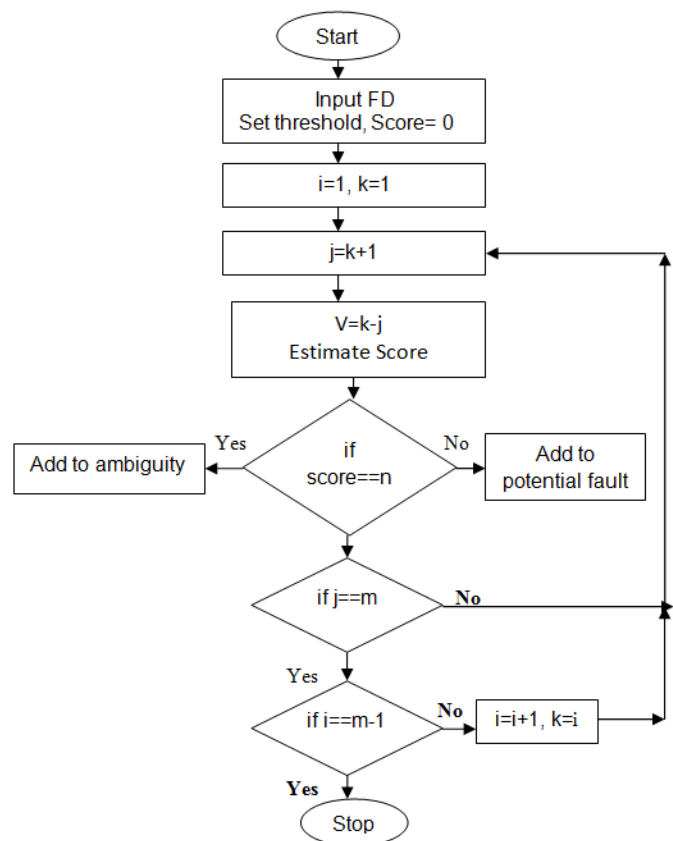


Fig.2. Flow diagram

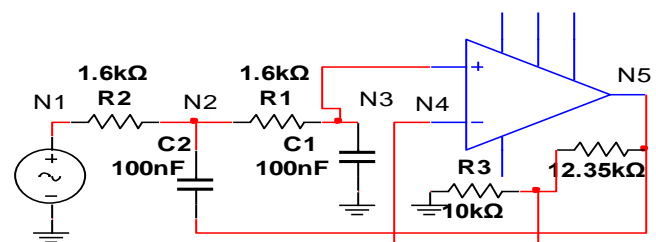


Fig.3. Second Order LPF

Table 1. Fault Samples of Second Order LPF

Fault ID	Fault Conditions	Node Voltages(Volts)
F1	R1 short	N2=1V, N3=0.7V,N5=1.566
F13	R1,R2 short	N2=1, N3=1 ,N5= 2.235
F41	R1,R2,C1(short)	N2=1.023V, N3= 0.45 , N5= 1.023

Faulty conditions include both hard and soft faults. Table 1 shows only samples. F1 score is estimated for the threshold values 0.05,0.1,0.15 and 0.2 and shown in table 2. Since the F1 score is highest for the threshold 0.05, this threshold value is used to

group ambiguity elements. The fault IDs which classified as potential faulty conditions (uniquely detectable) are F1, F3, F12, F13, F17 etc. Out of 140 faulty conditions 41 faulty conditions have been identified as uniquely identifiable.

Table 2. F1 Score for threshold values 0.05, 0.1, 0.15, 0.2

Threshold Value	True Positive	True Negative	False Positive	False Negative	Precision (P)	Recall (R)	F ₁ Score
0.05	41	97	0	0	0.95	1	0.97
0.1	41	69	0	30	1	0.58	0.73
0.15	36	99	5	0	0.88	1	0.93
0.2	35	97	7	1	0.83	0.97	0.89

4.2 8-bit Digital to Analog Converter

Figure 4 shows the circuit diagram of an eight bit DAC. The circuit consists of 8 nodes including input reference voltage node. Simulation is performed for 245 faulty conditions on the test nodes 2,4,6,7. Table 3 shows the F1 score obtained for the threshold values 0.05,0.1,0.15,0.2.

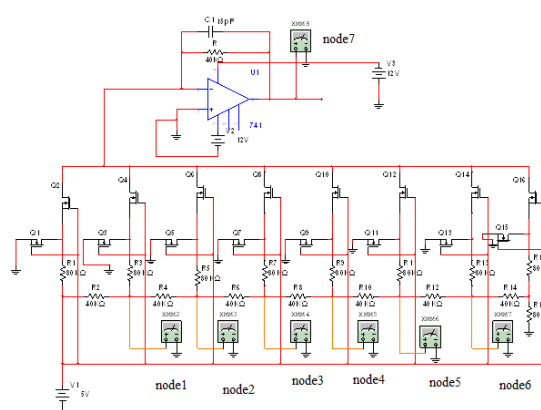


Fig. 4. 8-bit DAC

Table 3. F1 Score for threshold values 0.05, 0.1, 0.15, 0.2

Threshold Value	True Positive	True Negative	False Positive	False Negative	Precision (P)	Recall (R)	F ₁ Score
0.05	14	154	0	77	1	0.15	0.26
0.1	123	117	0	5	1	0.96	0.98

0.15	117	124	4	0	0.96	1	0.98
0.2	116	121	7	1	0.94	0.99	0.96

Table 3 shows that F1 score obtained for threshold values 0.1, 0.15 is the same and highest. Hence any of these two can be used for estimating the score value for classification. Out of 245 faulty conditions 123 faulty conditions are correctly classified as potential faulty elements (true positive).

V. CONCLUSION

A simple binary classifier for ambiguity sets grouping is implemented and verified for its performance. The approach is called binary classification because the faulty conditions are classified under two categories. In case of second order LPF, about 30% of the faulty conditions are found to be uniquely detectable with 3 nodes for testing and in 8-bit DAC, it is 50%. The results show that lower the threshold values more number of ambiguity values.

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