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Reliability Analysis of a Newly Proposed two Disjoint Path Multistage Interconnection Networks

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Abstract:
For parallel computation, various multistage interconnection networks have been discussed in the literature. But these networks always required further improvement in reliability and fault-tolerance. Fault-tolerance of the network can be achieved by increasing the number of disjoint paths as a result reliability of the interconnection networks also improved. In this paper, two new design of two disjoint paths fault tolerance MINs (2DP-FTMIN-1 and 2DP-FTMIN-2) are discussed. These new designs are inspired by the combination of banyan network, Gamma interconnection network and shuffle exchange network. Here reliability, cost and fault-tolerance of these two proposed layouts of MINs are calculated and these designs are compared with other existing MINs of this category.

Keywords*: Fault-tolerance (FT), disjoint paths (DP), multistage interconnection networks (MINs), shuffle exchange network (SEN), gamma interconnection network(GIN), reliability block diagram technique, terminal reliability(TR).*

1. Introduction

There is requirements of high computation speed and power in various applications areas like telecommunication, distribution of power, aerospace technology, automation in industry, genetic engineering and artificial intelligence. Parallel computers with many processors are used in the above stated applications and these types of multi-processor systems required interconnection networks for establish a link between processors to memory modules. As we know, the crossbars of such large size is not cost effective, hence MINs of effective cost [1-2] were developed to provide same functions at low cost. If a researcher want to connect N number of processor module to N number of memory module he can use either a crossbars or multistage interconnection networks (MINs) but complexity of these two will differ. The order of complexity of crossbar connection for such system will be $O(N^2)$ while a single layer MINs has a complexity of O(N X logN). Fault-tolerance capability and the estimation of reliability of MINs are area of interest to the researchers working in the field of parallel computing and interconnection networks. In the literature, there are a number of methods for increasing the fault-tolerance capability of MINs [3-5] have been proposed by the researchers. These methods include adding an extra stage of switches in the structure of MINs, by changing switch size, inclusion of extra links, by changing the pattern of interconnection networks, using chaining and back links to the switches. These above mentioned techniques popularly used for implementing various types of regular and irregular MINs.

This paper is discussed in five section: section 1 contains the introduction, in section two preliminaries, background and motivation of the

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research are discussed, section 3 introduces the new proposed design and its topology and last section contains conclusion and future scope of this research work followed by references.

2. Preliminaries and Backgrounds

Before discussing about our new layout first we talk about the issues of fault-tolerance capability of MINs with respect to disjoint paths and redundant paths, then we present the motivation for proposing our new layout. In addition, network structure of SEN, SEN+, SEN+2,GIN, Extra Stage Cube network, Benes network and Extra stage Benes network are presented in the subsequent sections.

There are two main class of MIN are found in literature (i) single path MINs (ii) multipath MINs. [3,8,10,11,12] Single path MINs like SEN, Baseline and generalized cube network[13-14] having low cost, but only single path between source and destination is consider as a big problem for these type of network. If any elements in this path failed then complete network will be failed. Therefore use of multipath networks can be considered as one of the solution to avoid this failure. There are various techniques are used to improve the number of paths. Some of them are providing extra stages, providing extra links, using MUX and DEMUX, using multilayer and replication of network and changing the interconnection pattern of network. A simple technique to increase number of paths is addition of extra stage [6] is used but there is simultaneous increase in the cost also. It can be verified in SEN and its variants like SEN+ and SEN+2, that increase in number of stages result in lower reliability because of increased number of component. Same result is also verified in GIN [7] also. Other technique widely used to increase number of paths is using MUX and DEMUX for connecting the basic MIN structure at input and output stages. This technique reduces the number of stages and improve the reliability and fault tolerant capability of the MINs [9]. Chaining and looping in between the switching elements of a particular stage also provide improvement in fault tolerance and reliability of the MINs. This method is widely used in various regular and irregular MINs. Gamma Interconnection networks is a widely used class of fault tolerance MINs which provide different number of path for different source destination node pair. GIN provides single path when source and destination node has same number, while for other source destination pair the number of paths is more than one. Various modification of GIN, with similar hardware cost of GIN have been discussed in literature [7] with only objective of increasing the number of paths.

There are various types of challenges faced during designing of these new layouts with more disjoint paths. Some of them are: highly reliable and fault tolerant design, routing algorithm should be fast and efficient and it should meet the expected performance quality.

2.1 Motivation for proposed design

Shuffle Exchange Network (SEN) [15] and Gamma Interconnection network (GIN) and their variants are widely used class of MINs, However their hardware complexity is quite high. Moreover Gamma Interconnection networks provides different number of paths for different tag values. Therefore using layout of SEN and GIN we construct a new class of MINs (2 disjoint path FTINs) which have better reliability than both (GIN and SEN and its variants). The hardware cost of the proposed design is lower than Gamma Interconnection networks and nearly equal or marginally higher than the SEN and its variants. Proposed designs (2 disjoint path FTIN-1 and FTIN-2) are topologically equivalent as 2 disjoint path FTIN-2 is obtained by slight rearrangement in the connection pattern of 2 disjoint path FTIN-1. These two networks provide single fault tolerance, because of availability of two disjoint paths for each source-destination pair and overall three number of available paths. Hence, they can be successfully compared with other MINs like SEN, SEN+, SEN+2,GIN, Extra Stage Cube network, Benes network and Extra stage Benes network having low cost and better performance.

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2.2 Network structure of various MINs having single path and 2 disjoint path

In literature various network structure of single path and two disjoint path are discussed here some of them are SEN, SEN+,SEN+2, Benes Network, Extra stage Benes Network, Extra Stage Cube Network and GIN.

Shuffle Exchange Network (SEN) is a single-path MIN which is shown in figure 1 which explain the block diagram of a 8X8 SEN MIN. Here every source and destination node connected through a single path therefore this is non fault-tolerant network. SEN MIN of size N ×Nconsists of N/2 SE of size 2 × 2 in each stage. There are $\log_2$Nnumber of stages are present. The overall switching complexity of SEN network is equal to the product of the number of switches in each stage to the number of stages which is given by N/2X (log2N). While in SEN+ one extra stage is added in SEN but same connection pattern are used. This increased the number of paths and reliability in SEN+ (one additional stage) as a result hardware cost of the network also increased. Which denoted by (N/2 X ($\log_2$N+1)). Similarly SEN+ is modified into SEN+2(with two additional stages). SEN+ provide two disjoint paths while SEN+2 provides four number of total path out of which two are disjoint. Figure 2 and 3 shows the topology 8X8 SEN+ and SEN+2 multistage interconnection networks.

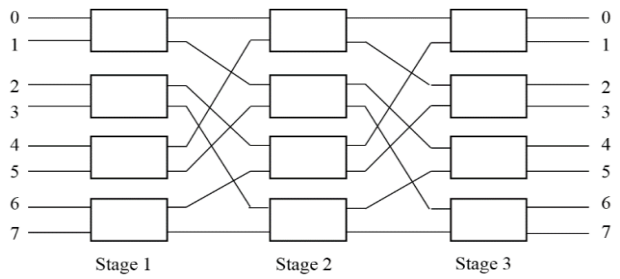

Figure 1. A 8X8 Shuffle exchange network (SEN)

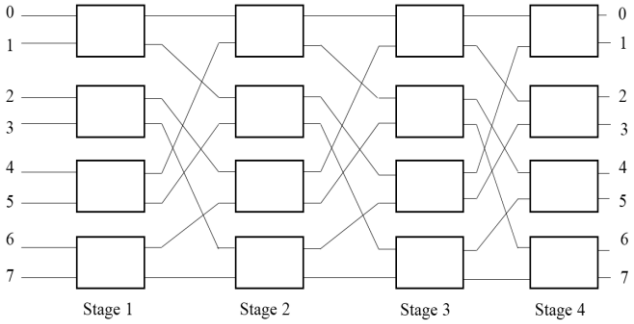

Figure 2. A 8X8 Shuffle exchange network with one extra stage (SEN+)

Extra stage cube network is also a two disjoint path networks whose topology is shown in figure 4. This network is modified form of generalized network with an extra stage at input and use of MUX and DE-MUX at input and output stages respectively.

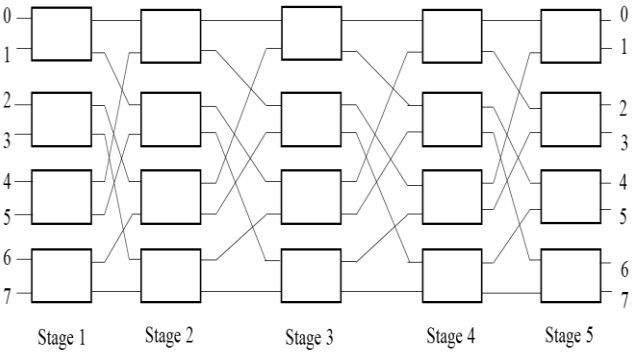

Figure 3. A 8X8 Shuffle exchange network with two extra stages (SEN+2)

A Gamma Interconnection Network (GIN) of size NxN consists of (log2N)+1 stages and each stage contains N number of switches [21,23]. This network is the modified form of the Inverse Augmented Data Manipulator (IADM) network. In figure 5 a GIN of size 8X8 is shown. As shown in figure the first and last stage of this network contains switches of 1X3 and 3X1 respectively and the other intermediate stages contains switches of 3X3 size. Each stage is connected with other stage by "power of two"[21]. DifferentSource to destination path is represented by the different tag values which is the difference between the source and destination. Benes network is also a type of network which has two or

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more than two paths. This network can be considered as a combination of a Baseline network (a blocking MIN) and an inverted Baseline network (a blocking MIN) in which the middle stages overlap. A Benes network of size NXN consists of $(2(\log_2 N)-1)$ stages and each stage is made up of N/2 switches of size 2X2. A Benes network of size 8X8 is shown in Fig. 6.

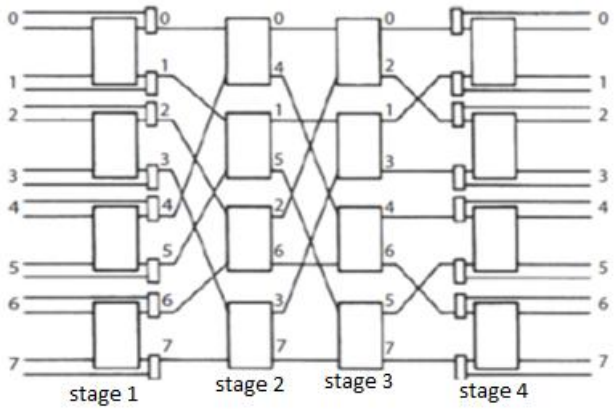

Figure 4. A 8X8 Extra Stage Cube network (ESC)

The method of "increasing the number of stages," is used in Benes network. Also, the obtained topology is named extra-stage Benes network (EBN)[24]. A Extra stage Benes network (EBN) of size NXN consists of $2(\log_2 N)$ stages and each stage is made up of N/2 switches of size 2X2.A EBN network of size 8X8 is shown in Fig. 7.

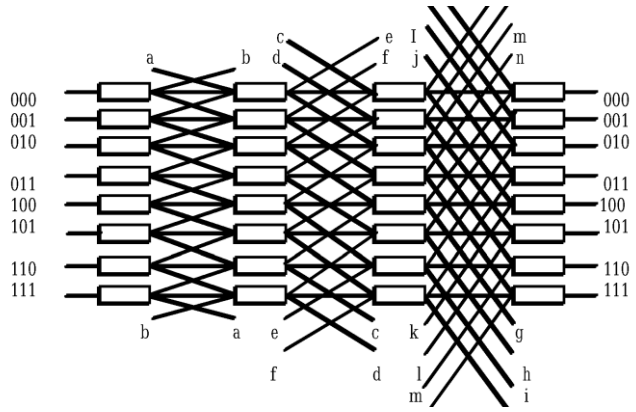

Figure 5. A 8X8 Gamma Interconnection networks (GIN)

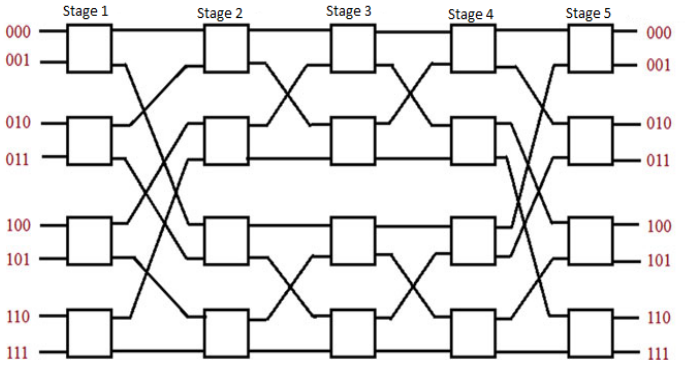

Figure.6. A 8X8 Benes network[24]

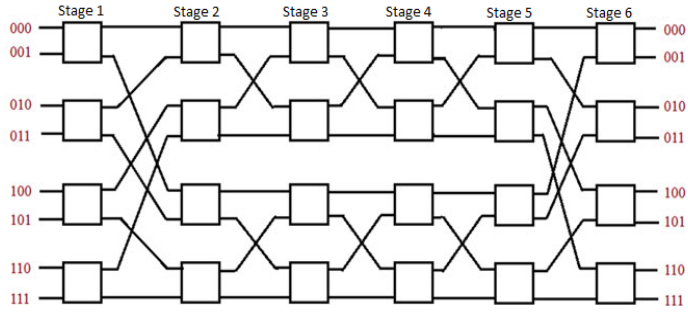

Figure.7. A 8X8 Extra stage Benes network (EBN)[24]

3. Proposed Designs: Two Disjoint Path Fault Tolerant MINs

In this section Two Disjoint path Fault Tolerant MINs are proposed. These designs contains n+1 stages which are numbered from stage 0 to n. Each stage has N/2 switching elements. First and last stage of this configuration having switch size of 2X2 and the intermediate stages contains 2X3 and 3X2 sizes switching elements respectively. Where $N = 2^n$ uses a shuffle exchange pattern connecting N inputs to N outputs at first and last stage which is similar to SEN with one additional stage while intermediate stages have Gamma interconnection networks pattern. The proposed four stage design of 2D FTMIN-1 for N = 8 is shown in Figure 8. The links between first and second stage connected by j^{th} switch is connected to the jth switch and $(j+2^i)$th switch of the next stage here i is the number of next stage. The intermediate stages of 2D FTMIN-1 contains SEs of size 2X3 and 3X2 in place of 2X2. In the second stage, each switch (j^{th}) contains 3 output links out of these three one is straight and other two is non straight (out of these two one is upward and another is downward

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link).Each straight link connected to the same number of switch in the next stage (third stage) non straight upward link connected to j-1 switch and downward link connected to j+1 switch of next stage. If obtained switch values are less than 0 and greater than 3 then 4 is to be added and subtracted respectively. 2DP FTMIN-2 can be obtained from 2DP FTMIN-1 by rearranging the links between first stages shown in Fig. 9. In design 2 first and last stage connecting in similar pattern and intermediate connection between stage 1 and stage 2 is equivalent to a GIN. Both 2DP FTMINs are topologically same, as a result both designs having similar performance and having equal reliability and hardware cost.

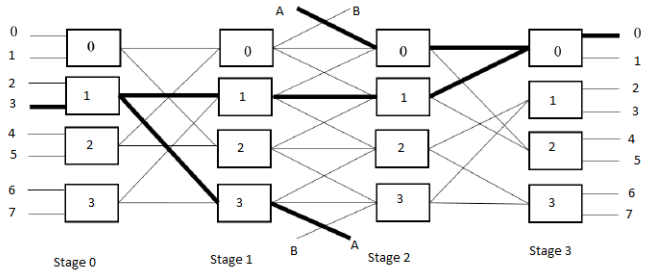

Figure 8. A 8X8 two disjoint paths fault tolerant multistage interconnection network (Proposed design -1)

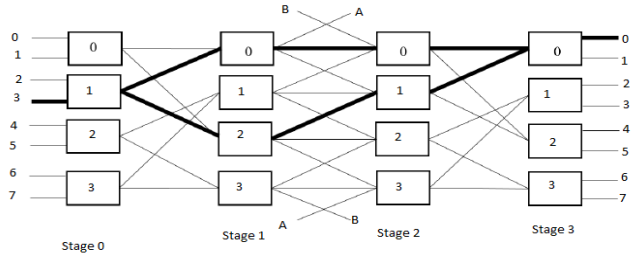

Figure 9. A 8X8 two disjoint paths fault tolerant multistage interconnection network (Proposed design -2)

4. Performance analysis and comparison

There are various performance parameters for MINs. In this paper, fault tolerance, Reliability and hardware cost are used to analyse the performance of our proposed design. Here fault tolerance is already discuss in the previous section. In this section we will discuss the reliability and hardware cost of proposed design.

Terminal reliability is considered as important parameters to improve the performance of MINs. With respect to the reported research works, reliability evaluation of MINs [16,17] can be calculated using various techniques such as the decomposition method, reliability bounds, Monte-carlo simulation, Reliability block diagram(RBD) and continuous time markov chain (CTMC). In this paper we are using reliability block diagram (RBD) techniques for our proposed design. With the help of this technique a complex MIN structure can be modelled into a combination of series and parallel arrangement of the components. In literature, the concept of Reliability Block Diagram (RBD) technique is presented in details [14,15,21-22] to evaluate the terminal reliability of SEN and its variants, Benes network, ESC, Extra stage Benes Network and GIN. Now using the relation of terminal reliability for SEN and its variants of size 8X8 from [14] where each switching element has equal reliability which is denoted by r, calculated by the following relation:

$$R_{st}(SEN) = r^{\log_2 N} \quad (1)$$

$$R_{st}(SEN+) = r^2[1-(1- r^{\log_2 N -1})^2] \quad (2)$$

$$R_{st}(SEN+2) = r^2[1-(1-(r^2(1-(1-r^{\log_2 N -2})^2)))^2] \quad (3)$$

Using the relation of terminal reliability for ESC of size 8x8 from [3] we have the following equation:

$$R_{st}(ESC) = r^2[1-(1- r^{\log_2 N-1})^2] \quad (4)$$

As discussed in literature that GIN does not provide a single relation of terminal reliability for all source and destination pairs due to availability of different number of paths for different source-destination node pairs. Now Using the relation of terminal reliability based on different tag values for GIN of size 8X8 from [23] we have the following equations:

$$R_{st}(GIN) = r^4 \text{ for tag values} = 0 \text{ and } 4 \quad (5)$$

$$Rst(GIN) = 3\, r^4 - 3\, r^5 + r^6 \text{ for tag value} = 1; 3; 5 \text{ and } 7 \quad (6)$$

$$Rst(GIN) = 2\, r^4 - r^6 \text{ for tag value} = 2 \text{ and } 6 \quad (7)$$

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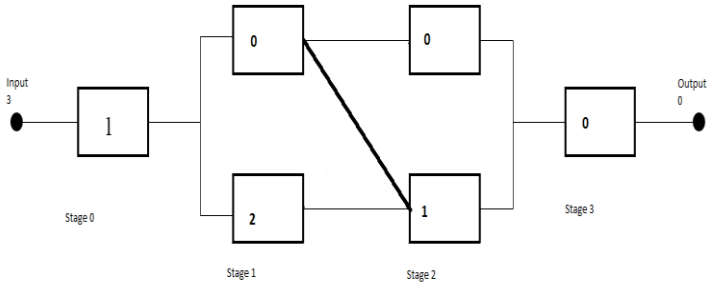
Terminal reliability of 8X8 Benes network is denoted by Rst(Benes) and calculated with the help of equation (8)

$$R_{st}(Benes)= r^2[1-(1-(r^2(1-(1-r)^2)))^2] \quad (8)$$

Using the layout of EBN the terminal reliability of 8X8 EBN is determined as below:

$$R_{st}(EBS)= r^2[1-(1-(r^2(1-(1-r)^2)^2))^2] \quad (9)$$

For evaluating the terminal reliability of Two Disjoint Path Fault Tolerant MINs (2DP FTMINs), we have to look at any source-destination node pair. 2DP FTMINs provides equal number of paths which is equal to three, for all source-destination pair, here out of three two are disjoint path hence using reliability block diagram, 2DP FTMINs can be modelled as shown by thick lines in figure 8 and 9. Using these above figure RBD for the terminal reliability expression of 2DP FTMINs is modelled as shown below in figure ___ .The shown diagram is a complex structure it is neither in series nor in parallel to obtained the expression of reliability of such RBD we used decomposition method[--]. Here we have to assume a keystone element in the structure and then calculate reliability



Using decomposition method the obtained relation for terminal reliability of the proposed design is given by equation below. (Here all SEs have same reliability = r)

$$Rst\ (2DP\ FTMINs) = r^3[1 - (1 - r)^2] + r^4\ (1- r) \quad (10)$$

Now after reliability calculation, hardware cost of the proposed design is calculated. A common method of cost analysis is to calculate the hardware complexity of the MIN. which is equivalent to the number of cross points in a switch. If we take an example of a 2X2 switch then cost of this switch will be equal to the 4 units. A MUX of size nx1 and a DMUX of size 1xn respectively correspond to n units of cost, here in table 1 hardware cost of proposed 2DP FTMINs and all other compared networks has been calculated.

Table 1: Hardware cost of proposed 2DP FTMINs and all other compared networks

No. of stages ➔	**Stage 1**	**Stage 2**	**Stage 3**	**Stage 4**	**Stage 5**	**Stage 6**	**total cost**
SEN	2x2x4	2x2x4	2x2x4				**48 units**
SEN+	2x2x4	2x2x4	2x2x4	2x2x4			**64 units**
SEN+2	2x2x4	2x2x4	2x2x4	2x2x4	2x2x4		**80 units**
ESC	(2x2x4)+(2x1x8)	2x2x4	2x2x4	(2x2x4)+(1x2x8)			**96 units**
GIN	1x3x8	3x3x8	3x3x8	3x1x8			**192 units**
Benes Network	2x2x4	2x2x4	2x2x4	2x2x4	2x2x4		**80 units**
EBN	2x2x4	2x2x4	2x2x4	2x2x4	2x2x4	2x2x4	**96 units**
2DP-FTMINs	2x2x4	2x3x4	3x2x4	2x2x4			**80 units**

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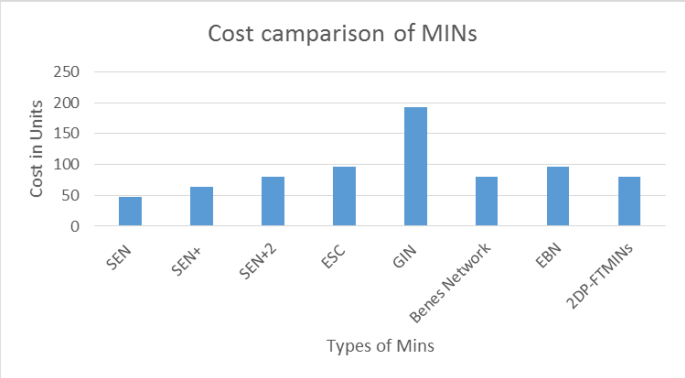

Now using the terminal reliability equation for proposed design, which has been already calculated with the help of RBD technique, reliability of the proposed designs are calculated and compared with the others MINs. Table 2 shows a comparative view of the cost, number of disjoint paths, redundant paths and reliability of proposed designs with other existing MINs.

Table 2: Reliability of 2DP FTMINs and all other compared networks

MINS TYPE	**TOTAL NUMBER OF PATHS**	**DISJOINT PATHS**	**COST**	**RELIABILITY EXPRESION(FOR 8X8)**	**RELIABILITY**		
					r=0.9	**r=0.8**	**r=0.7**
SEN	1	1	48	$r^{\log_2 N}$	0.729	0.512	0.343
SEN+	2	2	64	$r^2[1-(1- r^{\log_2 N -1})^2]$	0.78076	0.55706	0.36255
SEN+2	4	2	80	$r^2[1-(1-(r^2(1-(1-r^{\log_2 N - 2})^2)))^2]$	0.77821	0.54484	0.33956
ESC	2	2	96	$r^2[1-(1- r^{\log_2 N-1})^2]$	0.78076	0.55706	0.36255
GIN	1	1	192	r^4 for tag values = 0	0.6561	0.4096	0.2401
	2	1		r^4 for tag values = 4			
	4	1		$3 r^4 -3 r^5 + r^6$ for tag value=1and7	0.72827	0.5079	0.33374
	5	1		$3 r^4 -3 r^5 + r^6$ for tag value=3 and 5			
	3	1		$2 r^4 – r^6$ for tag value = 2 and 6	0.72171	0.49152	0.31213
BENES NETWORK	>3	2	80	$r^2[1-(1-(r^2(1-(1-r)^2)))^2]$	0.77821	0.54484	0.33956
EBN	>3	2	96	$r^2[1-(1-(r^2(1-(1-r)^2)^2))^2]$	0.775587	0.5323	0.3170
2DP-FTMIN-1	3	2	80	$r^3[1 - (1 – r)^2] + r^4 (1- r)$	0.78732	0.57344	0.38416
2DP-FTMIN					0.78732	0.57344	0.38416

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-2							

5. Conclusion and future scope

New layout of fault tolerant MINs denoted by 2DP-FTMINs are proposed. This design provide three redundant paths for every source and destination node pair out of which two are disjoint path, this makes the network single switch/link fault tolerant in intermediate stages. The results of performance analysis from table 1 and table 2 suggest that 2DP-FTMINs surpasses SEN, SEN+ and SEN+2, which are widely used in practical interconnection networks in terms of hardware complexity and reliability. Proposed designs also outperforms other MINs, namely ESC, GIN, Benes Network and Extra Stage Benes network. Hence on the basis of result the proposed design can be consider suitable for practical interconnection networks. In this paper reliability and hardware complexity is consider as essential parameters for comparison the researcher can compare these topology using other parameters like broadcast reliability, throughput and bandwidth. There are other techniques of reliability evaluation can be applied for reliability evaluation.

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