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A Novel Leakage Minimization Control Technique for Minimum Leakage and power dissipation in Deep and Ultra Deep Submicron CMOS Technology

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Abstract

Leakage current in Deep Submicron (DSM) and Ultra DSM has become a significant IC design parameter. Power losses due to leakage current increase exponentially with improvement in the technology and are probable to become the central part of whole power. The reduction of the threshold voltage, gate oxide width, supply voltage, device size and increase in the density of the circuit are causing a dramatic increase in leakage and hence power losses. Reduction in source voltage condenses leakage power which, results into reduced operational speed. To maintain the speed of operation unaffected, one has to reduce the transistor threshold voltage. But threshold voltage scaling results in a significant rise in the subthreshold leakage current. Due to this leakage current conduction, power dissipation increases exponentially. Leaky subthreshold current is a overriding factor in deep submicron whereas gate oxide channelling is a major contributor for dispersive leakage power in ultra-deep submicron design. Stating that leakage contribution increases rapidly due to numerous technical reasons, this paper identifies the problem and hints towards possible solution.

Keywords: *CMOS design, Deep submicron CMOS design, DSM, Low power VLSI design, Leakage current, Power dissipation, Ultra CMOS design, UDSM.*

I. INTRODUCTION

Energy subtle design demand has grown radically due to rapid evolution of battery dependent handy devices. Dimensional scaling expertise continues without abating, the design of subthreshold strategies has attracted considerations in low power and ultra-low energy depletion in innumerable devices. High performance and low power DSM and ultra DSM CMOS circuital design is a profound and serious task. As per Moore's rule, number of transistors have to be doubled, area reduced by half and frequency gets doubled. Hence, the new emerging technology is meant for greater complexity, increased performance, higher device density and low power dissipation. Power dispersion in CMOS is because of static and dynamic circuital behaviours. Static power dissipation is due to different leakage currents like subthreshold conduction through off transistors, tunnelling current through gate oxide, leakage current through reverse biased diodes etc. Dynamic power dissipation is due to charging and discharging of load capacitance, short circuit current while both NMOS and PMOS networks are partially on. The various existing leakage reduction techniques are: multiple threshold CMOS circuits, Sleep Technique, Sleepy keeper Technique, Stack Technique, Sleepy Stack with Keeper Technique, LCT, Zig-Zag with keeper, Domino logic circuits, Dual and Variable threshold CMOS logic circuits and so on. Reviewing the past and latest technological developments this defines new design aspects

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II. PROBLEM DEFINATION

Deep submicron, ultra deep submicron and Nano design are faster but, issues are leakage, temperature susceptibility, signal/power integrity and device parameter variations. Reduction of supply voltage reduces power dissipation but, speed of operation reduces. Scaling the transistor threshold voltage significantly increases subthreshold leakage current. Subthreshold leakage current and gate oxide tunnelling increases power dissipation in deep submicron and ultra-submicron circuits. The solution lies in reducing the area which doubles frequency of operation.

III. DESIGN CHALLENGES

- Low power, reduced leakage and high performance design
- Getting good signal quality and integrity
- Handling of Design complexity
- Packaging, testing and reliability

IV. OBJECTIVE

Objective is to design a robust CMOS architecture using a novel or new leakage minimization technique, which gives minimum leakage with improved electrical performance and reduced chip area as compared to existing in deep and ultra-deep submicron regions.

V. METHODOLOGICAL ASPECTS

Technological advancement saw an innovative jump from large and unreliable vacuum tubes in first half of 20th century to devices as small as 18nm FinFET. CMOS transistors may not work below 10 nm as per experts but, it is estimated that by 2024 the sizes may shrink up to 2 nm and this CMOS device shrink given rise to circuital problems and research is on to counter this aspect on vigorous ground. Power dissipation in CMOS is because of static (figure 1) and dynamic (figure 2) aspects of the circuit. The dynamic power leakage is due to charging and discharging of load capacitance and short circuit actions during circuit switching and static leakage is due to the following sources: PN junction reverse bias current (I1); Subthreshold channel leakage (I2); Drain induced barrier lowering effect (I3); Gate induced drain leakage (I4); Punch Through (I5); Narrow width effect (I6); Gate oxide tunnelling (I7), Hot carrier injection (I8). All these factors are depicted in the diagram shown in figure 1 below:

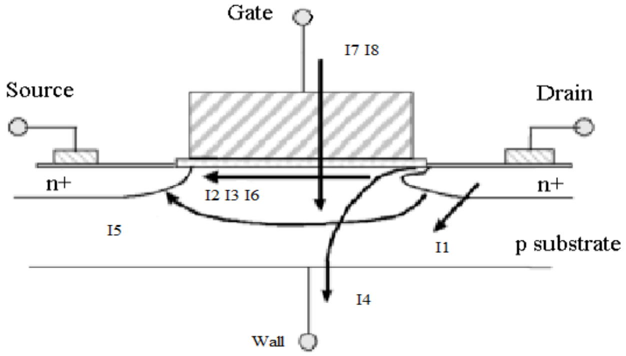

Figure 1Static Leakage sources

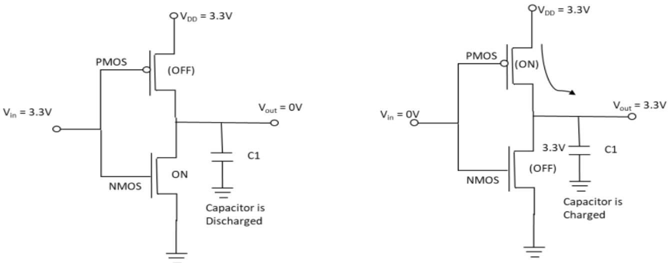

Figure 2 Dynamic Leakage sources

The overall power dissipation is described by an equation (1)

$$P_T = P_{sc} + P_{dyn} + P_{st} \qquad (1)$$

$$= I_{sc}V_{dd} + \alpha C_L V^2_{dd} f + I_{st}V_{dd} \qquad (2)$$

Where, V_{dd}-supply voltage, I_{sc}-short circuit current, C_L – Load capacitance, I_{st}-static leakage current and f –frequency and α- switching factor.

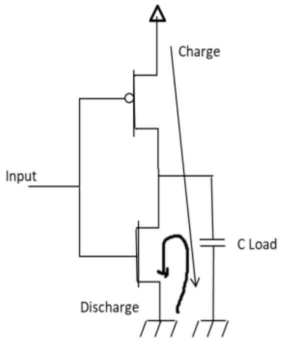

Figure 3 (a) Dynamic leakage

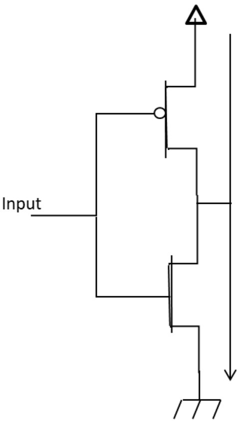

Figure 3 (b) Short Circuit Leakage

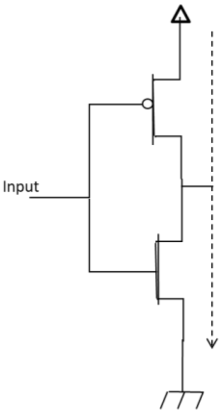

Figure 3 (c) Static Current Leakage

Most of the circuit level reduction techniques are based on subthreshold leakage current which results due to the potential difference between source and drain resulting into a flow of current through the channel. The governing equation is given as:

$$I_{SUB} = KV_T^2\left(\frac{W}{L}\right)e^{\frac{V_{gs}-V_{th}}{nV_T}}(1-e^{\frac{V_{ds}}{V_T}}) --------------(3)$$

Where, W-channel width; L- channel length; V_{ds}-drain to source voltage; V_{gs}-gate to source voltage; V_{th}-threshold voltage; V_T-thermal voltage;

$$n = 1 + \frac{C_{dm}}{C_{ox}} --------------------------(4)$$

$$K = \mu_0\sqrt{q\Delta_{si}\frac{N_{ch}}{2\phi_s}} ----------------(5)$$

Where, C_{dm} – capacitance of depletion layer and C_{ox}- capacitance of oxide layer, q- charge, N_{ch}-channel doping value, μ_0-zero bias mobility, Φ_s-potential surface and Δ_{si}- silicon oxide thickness.

Leakage power is a function of supply voltage (V_{dd}), the threshold voltage (V_t) and transistor sizes. As V_{dd} at process node shrinks or scaled, leakage becomes more significant consuming at least 30% of total power.

There are two design constraints viz., high performance and low leakage. These two constraints are judged by the difference between oxide thickness, supply voltage and threshold voltage. Oxide thickness supports low leakage high voltage and reasonable performance and at the same time smaller area (thickness) reduces active power dissipation and uses low leakage design.

Technically it has been found out that clock gating and multi voltage threshold (multi-vt) reduces dynamic power consumption and leakage current respectively. Dynamic power consumption depends on physical capacitance and the relation is linear. The capacitances may be minimum with smaller devices but, this measure makes circuit operation slower.

VI. PROPOSED METHOD

As it has been concluded by many researchers that multi threshold technique is a satisfactory method for subthreshold leakage reduction.

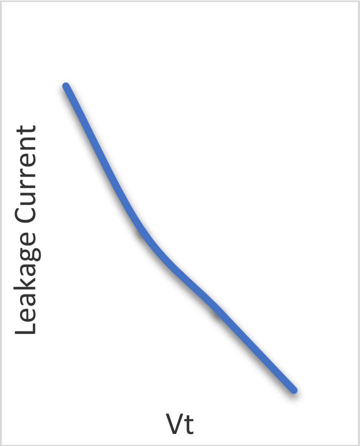

Figure 4 Threshold Voltage

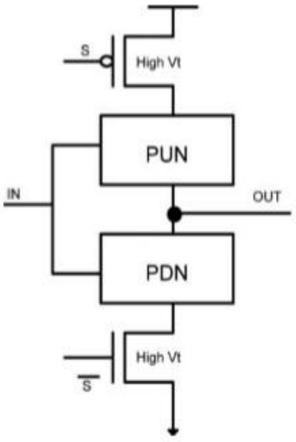

Figure 5 MTCMOS circuit

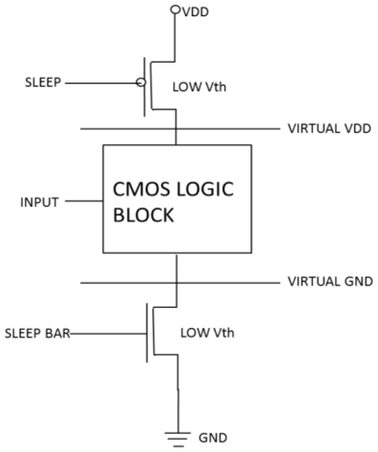

Figure 6 SCCMOS circuit vs Leakage current

Figure 4 shows that as threshold voltage increases leakage current decreases and as threshold voltage decreases leakage current increases. Prompting one has to use an optimum value of threshold voltage. The transistors with optimum threshold value are selected in the critical paths using multi threshold technology. MTCMOS (figure 5), circuit is implemented by inserting high Vth transistors between the power supply voltage and the original transistors of the circuit and in SCCMOS (Super Cut-off CMOS) (figure 6) a normal Vth transistor is used to reduce the additional delay caused due to the presence of increased threshold value in the transistor. The technology has been shrunk, the leakage power grown exponentially. Deep submicron gives rise to subthreshold leakage whereas ultra submicron gives rise to gate oxide leakages. Both of these drawbacks can be addressed by hybrid mixing of MTCMOS-SCCMOS with sleep and stack technology as these are two dominant methods to counter power dissipation in CMOS circuits.

As per once estimation, nearly 30% of power can be saved by using this technology. Thus to arrive at a reasonable speed and low leakage, a combination of MTCMOS and SC-CMOS with 10% area reduction in deep submicron and ultra submicron is proposed wherein leakage optimization on transistor level is just to modify doping profile and the dielectricity of the oxide.

VI. CONCLUSION

Most of the advances in semiconductor IC’s are related to the capability to reduce or resize device dimensions. Expertise in size change in the ultra-deep submicron region grown, exponential increase in leakage power has become major module factor as far as total power dissipated in the CMOS circuits is concerned. In today’s portable technology power consumption has become the primary concern which are characterized by high speed, low power consumption and complex functionality. The goal achieved with low power dissipation and reduced leakage is to achieve less system cost and high reliability. CMOS which is a combination of PMOS and NMOS in which the transistors are stacks of gate, oxide and silicon. Deep submicron and ultra-deep submicron technology uses transistors of miniature size with faster operational frequency, the world of design and fabrication became complex but, advantageous. This paper proposed a hybrid-mixture of MTCMOS-SCCMOS technology in order to arrive at the goal of less leakage and high performance

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