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Processor Testing Software by Implementing Rapid Self-test Technique

SantiSwarup Basa[1], Debashis Pradhan[2], Lipsa Das[3], Abhaya Kumar Panda[4], Santosh Kumar Swain[5]

[1,2,3]Department of Computer Science, North Orissa University, Baripada, Odisha, India
[4,5]Department of Computer Science Engineering, KIIT Deemed to be University, Bhubaneswar, India
cispubip@gmail.com

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Abstract

Less Complex and rapid software-based self-test (SBST) methods are frequently used for evaluating contemporary processors due to the simplicity of synthesis using developmental methods, coverage for hard to check faults, non-invasive, small hardware overheads and alike. Moreover, the amount of time it takes for the SBST test synthesis is high. In this paper, an extension of the SBST method known as Rapid SBST (RSBST) is suggested; this decreases general sample synthesis speed by reprocessing simulation answers from current sample programs of the same observability. Test instructions, created expending the evolutionary process, which generates comparable fault simulation outcomes, are reprocessed for fault assessment. The proposed system utilizes the re-processing to increase the speed and promptness of the sample synthesis. The implemented RSBST methodology accelerates by an influence of "1.35" though preserving a fault of "1.35" and retaining a fault coverage above "96.2" percent.

Index Terms: *testing, software testing technique, RSBT, SBST.*

I. INTRODUCTION

As computer technology is complicated and growing, the accuracy of incorporated processors is very vital during the chip manufacturing and deployment phases. Classification of all physical faults has always been complicated since test patterns must be adapted to IC operating frequencies, which are exceptionally large. This at-speed test function is very hard to accomplish with internal tester techniques, as tester frequencies might not reach processor frequencies. To fix this problem, software-based self-test (SBST) methodologies [1], [2],[3] have developed software-based check scripts to be implemented to processors as sample protocols. These sample sequences are a series of orders with chosen operands that could affirm the features of the processor. SBST methods are non-intrusive even though the structure of the instrument does not require any change for experiments. SBST has subsequently evolved as an efficient solution or complementary technique for the production of microprocessors and integrated processors [4]–[8]and in-system testing. Key microprocessor businesses have acknowledged the ability of SBST to implement it in their sample streams. SBST is a non-intrusive strategy that integrates a "computer tester" with the shape of a self-test program in the on-chip space of the processor. As a result, SBST has enhanced flexible characteristics that can effectively address the issue of tiny storage array in-system screening that lacks MBIST. Software-Based Self-Test (SBST) has appeared as an efficient option for construction processors and in-system monitoring. For tiny storage applications that contain BIST circuitry, including cache label panels, SBST can be a versatile and low-cost alternative for the March experiment implementation and therefore a feasible complement to hardware methods. These less complex sample cards are uploaded to storage

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places and the answers are accessed and contrasted for error detection. In addition, SBST does not involve any additional hardware that would result in a decreased sample price and null processor region penalty. This paper describes a powerful software self-test method called Rapid SBST (RSBST) where the experiment synthesis is quicker opposed to greedy oriented developmental methods and at the same moment does not reduce the fault coverage. In RSBST, redundant sample alternatives are recognized and their simulated outcomes are utilized for quicker fault coverage. This reusability system is designed to accelerate the traditional developmental sample synthesis.

II. RELATED WORK

Advances in the development of manual test patterns [9] have led significantly to the development of efficient testing programs. Intricate functional test patterns are created for the development of pipelined multi-threaded processors, vibrant command execution, and multi-core. A developmental method to automate the synthesis of auto software testing programs is described in the paper[10][11], [12]. The "μGP" self-adapting design is searching for improved sample programs. Earlier "μGP" methods utilize reporting coverage as a software usage metric. Later, the same method was expanded with "toggle, branch, expression and situation coverage"[13]. Furthermore, the testability of "corner-case faults" referred to as "hard-to-test faults" would be considerably low as they are not feasibly trackable by the synthesized test schemes. These prior "μGP" methods, could not ensure the performance of the experiment as these difficult-to-detect errors were kept unhindered and the code-based error assessment metrics do not have a rigorous connection with the gate-level error designs. These techniques could not achieve gate-level fault coverage of more than 90 percent for the synthesized match schemes[14]–[17]. These "μGP" tests progress in dozens of hours, which are fairly quick but require sufficient defect coverage. On the other side, the latest SBST automation approaches [18] have enhanced aspects of visibility but depend on effort-consuming sample production methods. Although the greedy element increases sample performance, this sample conception procedure [19][20], [21] would have to take roughly 170 hours of error assessment and contrast. Recommended in the classical SBST synthesis, the automation of processor experiment programs is carried out with the assistance of a developmental strategy that creates multiple experiment alternatives by employing genetic controllers. "SBST" strategies for target caches have also been described in some paper [22]. Almost all of them concentrate on converting "March algorithms" for in-system evaluation of caches at algorithmic stage or mitigating cost in terms of sample duration while maintaining "fault coverage"[23], whereas others continue providing pseudo-instruction patterns for "March activities" thorough experimentation outcomes of processor benchmarks[24][25]–[27].

III. PROPOSED WORK

In the suggested RSBST method, reprocessing of experiment response for similarly observable experiment programs is conducted to decrease the general sample production time. The general strategy of the RSBST processor automation system is shown in Figure. 1. In this system, the developmental core creates a sample alternative for optimum fault coverage that exploits the original population of sample schemes depicted as guided acyclic graphs (DAGs) and a training library. In the past, all the test systems were analyzed using an external evaluator. In order to decrease this expense of fault assessment, a computational complexity comparator is implemented, which contrasts and recognizes sample programs with comparable observability.

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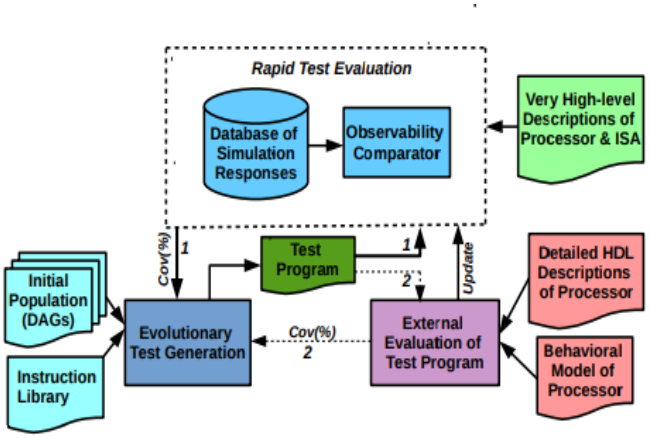

Figure 1 Block Diagram of Proposed System

Algorithm 1: Reusability of Greedy Coverage Method in RSBST Approach

Input: i^{th} generation of solutions $S_i^1, S_i^2, \ldots, S_i^{\mu+\lambda}$.
CF_i be the list of all covered faults until the generation i.
OBS_i^j be the values of observable destinations when S_i^j is executed.

Output: Modified CF_{i+1} of the $(i+1)^{th}$ generation.

1 If $OBS_i^j = OBS_i^{parent(j)}$, then the faut coverage list of S_i^j = the fault coverage list of $S_i^{parent(j)}$;
2 Else, evaluate the fault list of S_i^j using fault simulation.
3 The fitness function of S_i^j is $|F_j|$, which is the cardinality of the set of its newly covered faults, where F_j = fault coverage list of $S_i^j - CF_i$;
4 If the individual S_i^j is selected, update CF_{i+1} with CF_i and the newly detected faults: $CF_{i+1} = CF_i \cup F_j$;

The suggested technique of "reusability of fault simulation" findings is defined in Step 1 and Step 2 of the aforementioned Algorithm 1. In Figure.2, the paradigm for the proposed "rapid test evaluation" of Figure. 1, it's explained. Here, an elevated-level simulation sample program with a small timing necessity is used to obtain the components of all measurable places. Furthermore, the observability of the freshly created P testing program and its parent are contrasted to the extent of reusability.

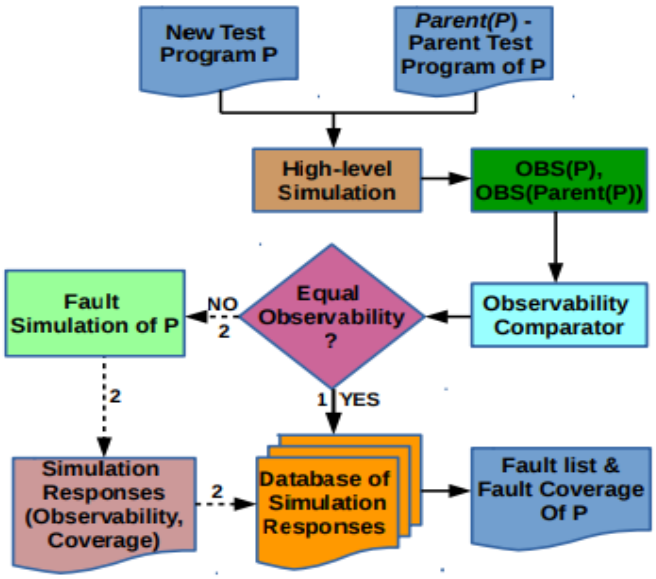

Figure 2 Test Generation in the proposed framework

IV. RESULTS

For the simulation of the proposed "RSBST test synthesis", similar kind of setup, benchmark processors, and fault models considered in is utilized. A 32-bit MIPS processor is also utilized and a "Leon3" processor model of "SPARC V8" architecture with a "7-stage pipeline" is also employed to be tested with the support of ten "behavioral fault representations" as shown in Table I.

Table 1 Behavioral fault representations

Fault Representation	Failure Type
Input stuck-at fault	Any primary input signal
Output stuck-at fault	Any primary output signal
If stuck then fault	If block is executed always
If stuck else fault	Else block is executed always
Elsif stuck then fault	Elsif block is executed always
Elsif stuck else fault	Elsif block is failed to get executed always
Assignment statement fault	Assignment of new values to a signal is failed always
Dead clause fault	A selected When clause in a case statement
Micro-operation fault	Micro-operations are failed always
Local stuck data fault	A signal object in a local expression

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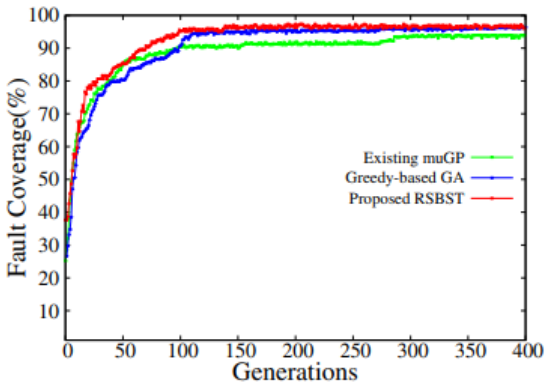
Table 2 Specifications utilized by proposed system

Specification	Value
Size of population (μ)	10
Number of offsprings (λ)	5
Number of generations	400
Selection methodology	Tournament selection
Size (τ) of the tournament	2
Steady-state threshold	40
Evolutionary methodology	ES($\mu + \lambda$) approach
Fault coverage evaluation method	Behavioral fault evaluation

The numbers of the parameters used for the suggested digital test are shown in Table II. The magnitude of the original sample "(μ)" is ten and the amount of offspring to be produced every generation is 5. The chromosomes of each batch are chosen by the "Tournament Selection Operator" in which the magnitude of the Tournament is 2. The developmental core performs a sample synthesis for four hundred generations and halts if there is no enhancement for forty generations, which is present in the steady-state limit.

The improvement in the growth of the sample synthesis using the suggested "RSBST" system is shown in Figure 4(a) for the "MIPS" processor. For the "Leon3" processor, the advancement of the error detection obtained using the "RSBST" system is shown in Figure 4 (b) of that. For the suggested "RSBST" strategy, the subsequent genes are replaced by likewise observable sibling cells together with the re-use of chosen DNA (μ= 10). Ultimately, the total reusable chromosomes would amount to 82.1 percent for the "MIPS" processor and 80.8 percent for the "Leon" processor.



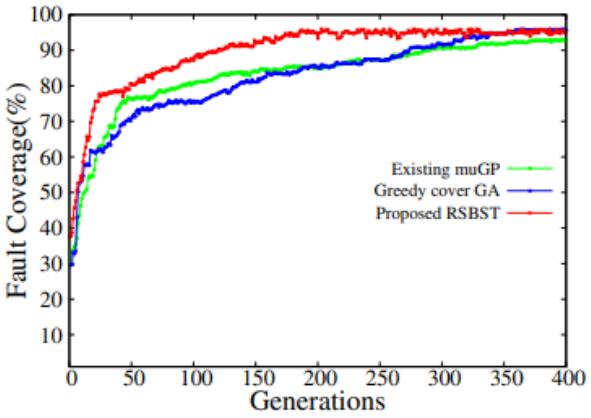


Figure 3 Outcomes of the simulation

V. CONCLUSION

In this research work, a quicker "SBST" processor fundamental synthesis is used by implementing an enhanced greedy-based developmental technique (RSBST) to develop sample schemes that could detect hard-to-detect faults. From the outcomes, consuming a more extensive fault model, the proposed approach is developing sample alternatives that could capture "97.3" per cent of the testable cognitive faults of the "MIPS" processor in "90" hours and "96.2" per cent of the sample failures of the "Leon3" processor in "98" hours. This confirms the genome (sample program) reuse of "82.1" percent for the "MIPS" processor and "80.8" percent for the "Leon3" processor. A quicker and reflective test synthesis may be implemented by utilizing the order of fragment reusability feature of the sample programs.

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