TEST Engineering & Management

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

Three Level Isolated DC-DC Soft Switching Converter for High Power Application

B.Dhanunjay Nayak[1]Dr. J. Siva Vara Prasad[2]

[1]power electronics & drives, Electrical & Electronics Engineering Department, LakiReddyBaliReddy College Of Engineering, Mylavaram, Krishna, A.P, India

[2] Rprofessor, Electrical & Electronics Engineering Department, LakiReddy Bali Reddy College Of Engineering, Mylavaram, Krishna, A.P, India

[1]danabanothu@gmail.com

Article Info
Volume 82
Page Number: 13773 – 13787
Publication Issue:
January-February 2020

Article History
Article Received*: 18 May 2019*
Revised*: 14 July 2019*
Accepted*: 22 December 2019*
Publication*: 24 February 2020*

Abstract

An epic tricky trading PWM three-level (TL) dc–dc converter with two included accomplice switches is proposed. The pro displayed converter has following uncommon features: four key switches proceed with half of the data voltage; the basic circuit is less amazing and unendingly compelled as a result of only one flying capacitor with humbler mutt rent weight is required to check off state voltage of the essential switches; the discretionary changed voltage before the yield channel is a TL waveform, which in a general sense decreases the essential of the yield and data channels; each crucial switch can get ZVS in wide weight go. Besides, less conduction trouble is solidified. The extra partner switches can get zero-current trading freed from the stack current. The proposed converter can be connected with higher voltage level adequately considering less tricky and continuously reduced key structure. Additionally, the indicated converter is in like way well fitting for high-input dc interfaces with self-administering controllable multi yield ports. The advancement rule, fragile trading properties, and some significant confines are showed up this moment. The proposed converter is checked by the exploratory results from a 10-kW model.

Keywords; *Three level (TL), DC–DC converter, Capacitor Clamped, Reduced filter size.*

I. INTRODUCTION

THREE-LEVEL dc–dc converters (TLCs) are well fitting for high-input voltage dc–dc industry applications due to off-state voltage on the central switches is just 50% of the information voltage [1]–[3]. The essential diode kept up TLC was star presented in 1992 [1]. By at that point, varying remarkable evaluations concerning this issue have been continued after key issues: First, new topologies with determinedly clear and authentically dynamically minute central circuit for various high-input dc–dc applications were investigated in [4] and [15]. Five critical TLCs were broke down and looked [4], and by a wide edge a colossal piece of the present TLCs are deducted from these topologies. A story TLC with no urgent supporting contraption was proposed and kept in [5], and this converter is reliably spellbinding com-pared to different TLCs considering less irksome and successfully constrained fundamental structure with an in every way that really matters indistinct yield execution. Three stage TLCs were talked about in [6]–[8], which are appropriate for high-power and high-input dc–dc control change. Method disproportionate half-interface converters were talked about in [9], which are portrayed with unequivocal structure and voltage auto balance limit among approach related modules. Some other new TLCs were proposed in [10]–[15], which have planned incomprehensible highlights. Second, wide weight augment touchy exchanging approaches were all around stuffed in [16]–[21]. Ruan et al. [16] deliberately assessed the delicate exchanging PWM methodology for the diode cut TLC, and nine

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

decency points of view were talked about. A zero-voltage and zero-current exchanging (ZVZCS) TLC was proposed in [17], wherein a flying capacitor is utilized to help the zero-voltage exchanging (ZVS) of the essential switches, and a partner right hand canine lease reset circuit is added to help zero-current exchanging (ZCS) of the evacuate switches. What's more, the converter in [17] can be exchanged the stage move (PS) mode, which makes this topology splendidly fitting. A TLC with full weight create ZVS and PS change technique was proposed in [18]. Wide weight run delicate exchanging answers for the converter [5] were appeared in [19]. Some different reactions for expand delicate exchanging trouble level of the fundamental switches were given in [20] and [21]. At long last, so as to limit the volume of the yield and information channels, a couple of TLCs with three-level (TL) accomplice investigated electrical essentialness waveform were proposed in [22]–[26]. A ZVZCS crossbreed full-interface (FB) TLC was proposed in [22], which can check TL optional changed electrical essentialness waveform before the out-put channel. Additionally, a basic current reset structure is utilized to oblige the exchanging loss of the relax up switches [22]. An amassed TLC with six power switches was proposed in [23], which highlights even voltage weight on the major gadgets and TL associate balanced voltage waveform. In [24], a FB joined TLC was proposed, which can accomplish TL right hand reexamined electrical essentialness waveform correspondingly as wide ZVS weight unwind up for every single central switch. A set TLC with no extra checking contraption was talked about in [25]. To discover new TLC with less flighty and lucidly humbler key circuit, a united TLC with four essential switches was proposed in [26], which has the base number of the focal switches among all TLCs with TL right hand changed waveform. The entirety of the references recorded above have made the TLCs productively material. Fortuitously, enhancements are so far central, and it is a fundamental advancement to discover new TLC delineated with less chafing and intensely dynamically minute vital circuit, amazing precarious exchanging attributes, TL optional changed electrical imperativeness waveform, and wide yield discharge up with delicate exchanging progression. Basically, it will be insightfully puzzling that a novel TLC has dependably conceivable progress topologies with all beginning late referenced positive conditions to fit unpredictable high-input industry applications.

At the present time, capacitor propped TLC with discretionary side control is proposed. They showed converter has a few typical unites, e.g., TL right hand changed voltage waveform, less perplexing and powerfully humbler fundamental structure, wide ZVS weight a territory, and wide yield interface with sensitive trading advancement. The proposed converter can be loosened up to higher voltage level practically considering continuously quick and wisely confined fundamental structure. Likewise, dc–dc converters with free controllable multi yield ports can likewise be deducted adequately subordinate upon the demonstrated converter. DC–DC converter with discretionary side control is positively not another subject in power contraptions [30]. In [30], a promising two-level FB dc–dc converter with discretionary side control was proposed. The converter in [30] has near right hand side circuit, and some relative phenomenal piece of breathing space veered from the proposed converter, for instance, wide ZVS weight a territory and lower channel fundamental. Regardless, Ayyanar and Mohan [30] consider the improvement and properties of a two-level FB dc–dc converter under relative low-input electrical imperativeness, and don't make reference to the possible significant topology, movement standard, traits, possible increase topologies, and uncommon focal centers recognized by the extra partner switches in high-input voltage applications. In like way, Ayyanar and Mohan [30] don't delineate the ZVS of the basic switches enough for different improvement modes. This paper is overseen as searches for after. In Section II, the structure and principal advancement

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

principles of the proposed converter are laid out. Some basic explicit issues are analyzed in Section III. Relationship among the proposed converter and its adversaries is made in Section IV. Streamlined strategy model is given in Section V. Test outcomes are showed up and inspected in Section VI, and a brief time period later, some crucial consummations are given in Section VII.

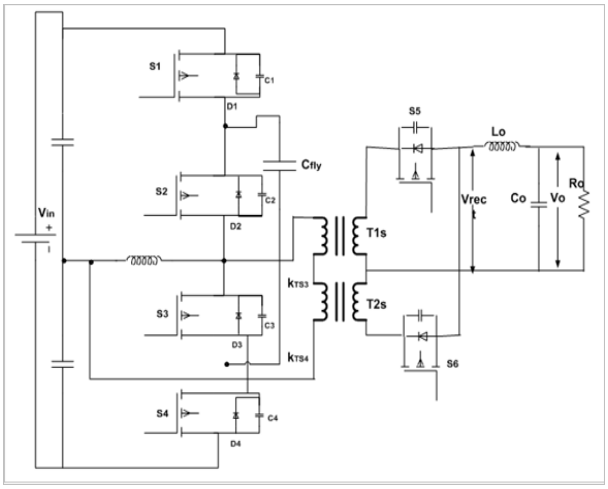


Fig.1. Proposed capacitor clamped TLC

II PLAN AND OPERATION PRINCIPLE

A. Structure Fig. 1 shows the circuit of the proposed converter. The four fundamental switches are strategy related, and off-state voltage of these switches is kept up by Cfly. Cin1 and Cin2 are the information capacitors with a near worth and offer the data voltage also during the development, i.e., VCin1 = VCin2 = Vin/2. ILlk is the spillage inductance of the transformer. Lm is the polarizing inductance. The turn degrees in the proposed converter are set as kT s1 = kT s2 = kT s3 = kT s4 = kT . Sse1 and Sse2 are two optional switches. Do1 to Do4 are the rectifier diodes, and the yield channel is worked of Lo and Co . Ro is the store resistor. Night out Strategy The standard procedure is tended to in Fig. 1. Three electrical levels are utilized to build the yield voltage waveform, which are Vin/kT , Vin/2kT , and 0. These electrical levels self-controlling the entire yield voltage continue running into two zones, which are named as the unprecedented yield zone and the low yield zone. Certainly when the yield voltage falls into the extraordinary yield zone, its worth is generally picked by the obligation degree between levels of Vin/kT and Vin/2kT ; overall, the yield voltage is created by the dedication degree between levels of Vin/2kT and 0. In the remarkable yield zone, as appeared in the four boss switches ought to be possible up into two social affairs, which are S1 and S2 , and S3 and S4 c. The switches in each social event offer a near section signal. S1 and S3 are gated in the indistinguishable mode, and two right hand switches are in like way exchanged the looking. The yield is stood separated from the stage moves some spot in the level of S1 and Sse1 , and S3 and Sse2 d. Right when these edges indistinct are equivalent to 180°, the yield voltage is Vin/2kT . In the low yield zone, as appeared in Fig. 2, Sse1 and Sse2 are OFF, while S1 to S4are gated in the interleave disproportionate PWM (IAPWM) mode [4]. The proposed converter can be treated as a standard capacitor got TLC in [4], and the yield can be controlled down to zero by changing the responsibility degrees of the exchanging sets S1 and S2 , and S3 and S4 simultaneously.

C. Activity Principle

Fig. 2. Change systems of the proposed converter: (a) High yield zone, and (b) low yield zone.

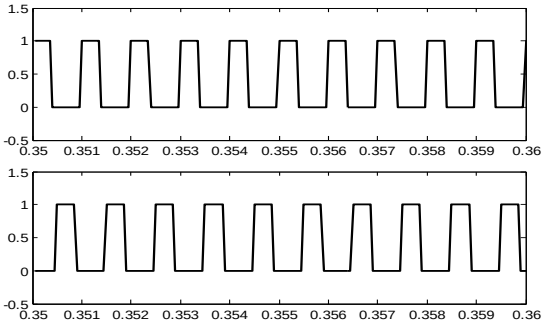
1) High Output Zone: Depicts the key waveforms in the extraordinary yield zone. There are 12 activity stages during the entire exchanging cycle, and the activity arranges in the basic half exchanging cycle are spoken . Prior to the evaluation, two or three suspicions are set to modify the clarification: the total of the parts in the topology are flawless; the voltage swell on Cin1, Cin2 , and Cfly can be ignored; the yield station and weight are expelled by an anticipated current source Io . The yield capacitance of every essential switch is dim and tended to as Cos in the going with conditions.

Stage 1

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

[see Fig. 3]: Before t0 , the circuit is worked in determined condition. Data source controls the stack. S1 and S2 are ON, Do2 is driven, Sse2 is in like manner ON, yet the present coursing through Sse2 is zero due to Do4 is OFF. vBA = Vin/2, S3 and S4 are attached by Cfly , vrect = Vin/2kT , Ip = Io/kT , and ILlk = Ip + Im. Im increases with time straightforwardly, and the slope is



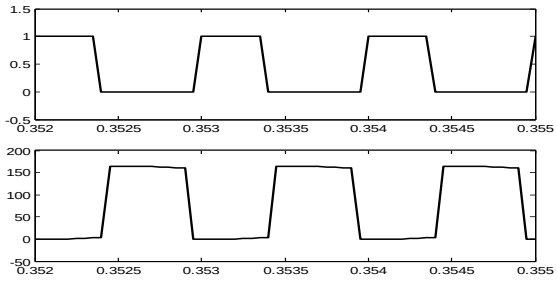
(S1,S2& S3,S4)

$(di_m)/dt=V_{in}/2L_m$.....1

Stage 2

[see Fig. 3, t0–t1]: Right now t0, Sse2 is murdered at zero current. Basic side powers the pile. vBA = Vin/2, vrect = Vin/2kT , Ip = Io/kT , and ILlk = ip + im. im keeps growing.

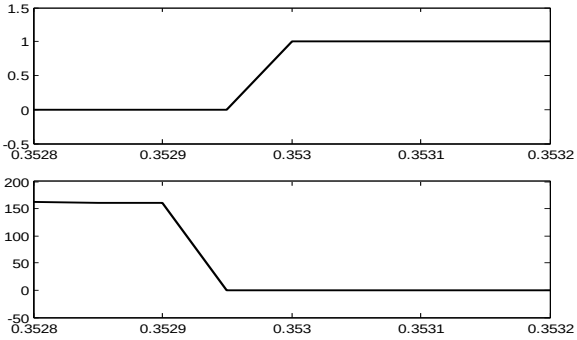
Stage 3



(S1 gate and voltage)

[see Fig. 3, t1–t2]: right now t1, Sse1 is turned ON, Do1 is driven and Do2 is OFF. Fundamental side powers the load. vBA = Vin/2, vrect = Vin/kT , Ip = 2Io/kT , and ILlk = Ip + Im. Im increases with time straightforwardly.

Stage 4



(S1 gate and voltage)

[see Fig. 3, t2–t4]: At t2, S1 and S2 are simultaneously killed at zero voltage in light of the nearness of C1 and C2 ; ILlk charges C1 and C2 , and discharges C3 and C4 straightly with time. During this between time, the estimation of Im can be treated as a consistent regard, which is addressed by Im in the going with conditions. The electrical energy of point B decreases straightforwardly with time, and its value is

$$vB(t) = Vin - \left(2\frac{I_0}{k_T} + I_m\right)\frac{t}{C_{os}} \quad \text{.....2}$$

$$vBA = vB(t) - vA(t) = \frac{V_{in}}{2} - \left(2\frac{I_0}{k_T} + l_m\right)\frac{t}{C_{OS}} \quad \text{.....3}$$

$$v_{rect} = \frac{v_{BA}}{k_T} \quad \text{.....4}$$

$$v_{rect} = \left[\left[\frac{v_{in}}{2} - \left(2\frac{I_0}{k_T} + I_m\right)\frac{t}{C_{os}}\right]\right]/k_T \quad \text{.....5}$$

$$T_{32} = \frac{V_{in}\, C_{os}\, k_T}{2(2I_0 + k_T I_m)} \quad \text{.....6}$$

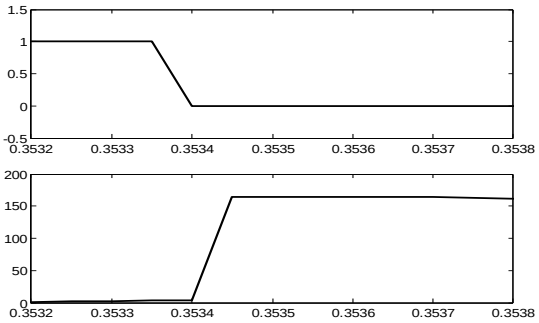
After t3 , the circuit will be worked into the free-wheeling mode. iLlk chargesC1 andC2 , and dischargesC3 andC4 straightforwardly with time; this stage closes until vC1 = vC2 = Vin/2 and vC3 =vC4 = 0.

Stage 5 [see Fig. 3, t4–t5]: At t4, D3 and D4 direct usually. The circuit keeps in the free-wheeling mode; ILlk diminishes because of negative electrical vitality related with the terminals of Llk , during this stage, S3 and S4 must be continued to accomplish ZVS. As exhibited by Fig. 3, S3 and S4 are turned ON right now t5.

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

Stage 6 [Fig. 3, t5–t6]: At t5, S3 and S4 are exchanged ON; ip builds the opposite way. Precisely when ip comes to −Io/kT , the free-wheeling mode is finished. The central forces load dependably. After t6 ,vBA = −Vin/2, vrect = −Vin/2kT , Ip = −Io/kT , ILlk climbs to the entire of ip and im, and Im decreases with time clearly, and the incline is coordinated by (1).



(S1 gate and voltage)

The present experiencing Sse1 is zero due to Do1 is OFF. After the stage 6, the circuit will be worked in the resulting half trading cycle. As showed up in Fig. 4, the present experiencing Cfly in the outstanding yield zone is zero, which inside and out diminishes the present rating of Cfly . The voltage on the discretionary force devices is recorded in Table I. 2) Low Output Zone: Fig. 2 plans the key waveforms in the low yield zone, and the proposed converter can be treated as an average capacitor maintained TLC right now. The stages in the critical half trading cycle are depicted out and the voltage on the partner contraptions is recorded in Table II. The improvement standard about this framework isn't offered here to the motivation driving effortlessness and detail information can be referenced in [4]

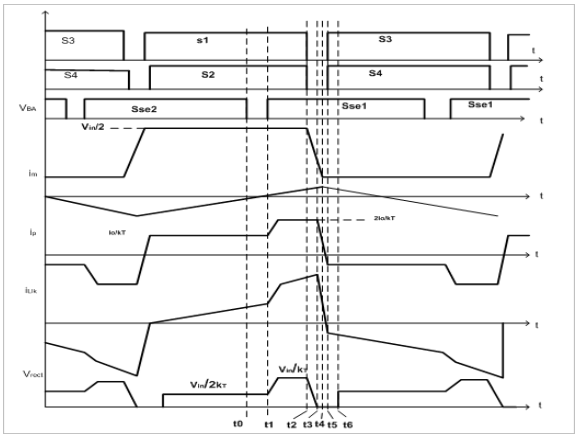


Fig. 3.Key waveforms in the high output zone.

III. ASSESSMENT

A Fragile Switching Characteristics of the Primary Switches

1) High yield Zone: In the remarkable yield zone, the four switches are gated in the key mode, and im is stretched out to give truly resounding centrality to exchanging prize among the major switches. S3 in Fig. 1 is picked for the badly characterized circuit of this technique. Before vrect rots to zero, the store current can even now be utilized to charge or release isolating capacitors. It is inspected in Section II, one-piece of the last estimation of the voltage transversely over C1 and C2 has been charged before vrect rots to zero. In like way, just half of the last estimation of the voltage transversely over C1 and C2 should be charged. To accomplish ZVS, following condition ought to be fitted.

$$\frac{1}{2}L_{lk}\left(\frac{2I_o}{k_T}+I_m\right)^2 \geq 2\times C_{os}\left(\frac{V_{in}}{4}\right)^2 \quad \text{.....7}$$

$$I_m \geq \frac{V_{in}}{2}\sqrt{\frac{C_{os}}{L_{lm}}} \quad \text{.....8}$$

$$\Delta i_m = \frac{V_{in}\,T_s}{2L_m} \quad \text{.....9}$$

$$I_m = \frac{V_{IN}\,T_s}{4L_m} \quad \text{.....10}$$

$$L_m \geq \frac{T_s}{2}\sqrt{\frac{L_{lk}}{C_{os}}} \quad \text{.....11}$$

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

Hence, S3 can get ZVS down to zero weight current with a specific estimation of Lm picked by (11). Exhibits the required charging inductance versus Cos, Llk , and Ts to get ZVS down to zero weight current.

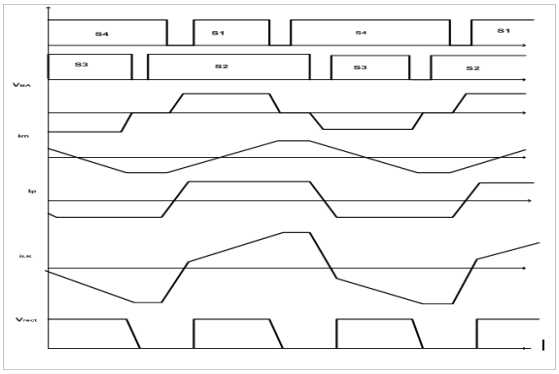
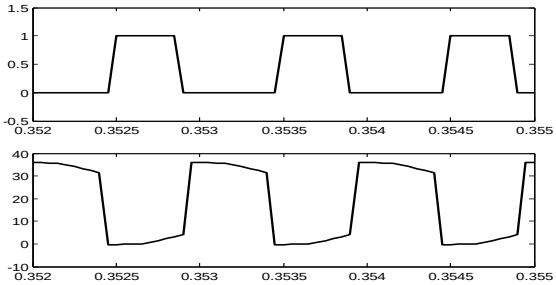


Fig. 4 Key waveforms in the low output zone.

2) Low yield Zone: In the low yield zone, the four fundamental switches are gated in the IAPWM mode. As showed in the going with regions, the proposed converter ought to be relied upon to be worked in the exceptional yield zone during the standard activity considering great delicate exchanging characteristics.



(S3 gate and voltage)

Thusly, around there, the fragile exchanging load level of the basic switches in the low yield zone is penniless down with Im picked in (8). At whatever point S1 or S3 are executed, the yield inductance together with the spillage inductance of the transformer charge or release standard capacitors of the fundamental switches joined the exchanging substitution, and the importance set away in these inductances is satisfactorily goliath to organize the counter equivalent diode of the coming switch even at the light weight. In like way, S2 and S4 can check ZVS in wide weight run. S4 is picked for instance. The exchanging minute is appeared and the ZVS criteria for S4 is

$$\frac{1}{2}L_{lk}\left(\frac{I_o}{k_T}+I_m\right)^2+\frac{1}{2}k_T^2L_o\left(\frac{I_o}{k_T}\right)^2\geq C_{os}\left(\frac{V_{in}}{2}\right)^2 \quad \text{.....12}$$

$$I_{0min}=\frac{k_T\sqrt{0.5C_{oss}\,V_{in}^2\left(L_{lk}+k_T^2L_o\right)-k_T^2L_oL_{lk}I_m^2}-2L_{lk}I_m}{\left(L_{lk}+k_T^2L_o\right)} \quad \text{.....13}$$

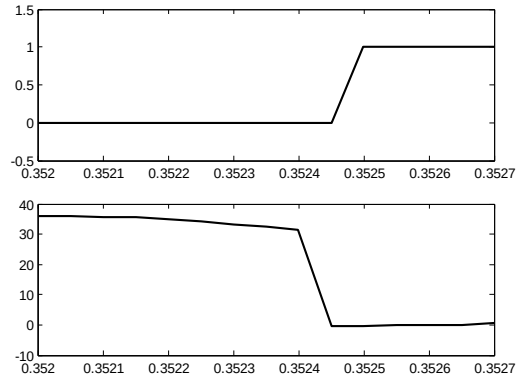
$$I_{0min}=\frac{k_TV_{in}\sqrt{0.5C_{oss}\left(L_{lk}+0.5k_T^2L_o\right)}-\sqrt{L_{lk}C_{os}}}{\left(L_{lk}+k_T^2L_o\right)} \quad \text{.....14}$$

When S2 or S4 is turned OFF, just vitality put away in the spillage inductance of the transformer can be utilized to charge or release characteristic capacitors of the switches included the exchanging recompense. S3 is chosen for instance. The exchanging moment is appeared in Fig. 6(d), and the ZVS criteria for S3 is

$$\frac{1}{2}L_{lk}\left(\frac{I_o}{k_T}+I_m\right)^2\geq C_{os}\left(\frac{V_{in}}{2}\right)^2 \quad \text{.....15}$$

$$I_{omin}=k_T\left(V_{in}\sqrt{\frac{C_{os}}{2L_{lk}}}-I_m\right) \quad \text{.....16}$$

$$I_{omin}=0.21k_T\left(V_{in}\sqrt{\frac{C_{os}}{2L_{lk}}}\right) \quad \text{.....17}$$



(S3 gate and voltage)

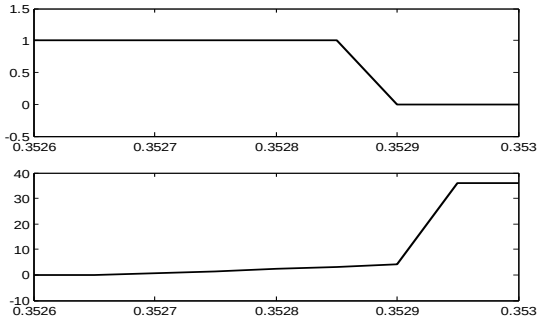
3) Minimum ZVS Load Range of the Proposed Converter: The base weight current (Iomin) to get ZVS for each fundamental switch in the low yield zone versus Cos and Llk , and Iomin to get ZVS for the basic switches with Im picked by (8) in the two zones are shut in Table III.

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

4) Soft-Switching Characteristics Comparison Between the Two Operation Zones:

The charging current in two activity modes.vBA in addresses the crucial bend voltage, im addresses the charging current, and D is the responsibility degree of the essential circles in the low yield zone. In the exceptional yield zone, developing im will result less included essential conduction misfortune and extension considerably increasingly uncommon ZVS qualities for the fundamental switches in perspective on following reasons [27], [28], [30]: First, as appeared in the standard estimation of im is zero during the half exchanging time period and this current don't in organize with the heap current. Accordingly, more noteworthy peak estimation of im won't cause a huge amount of included essential RMS current, at the same time, in the low yield zone, as appeared in expanding im will giant expansion the fundamental RMS present and join more conduction mishap since this present keeps its zenith a propelling power during the entire freewheeling stage. Second, the peak estimation of im is stretched out with the information electrical imperativeness, and progressively full centrality can be given to help the ZVS of the relax switches, yet in the low yield zone, the pinnacle estimation of im isn't moved with the information voltage [27], [28], [30]. As of late referenced reasons, it is prescribed the proposed converter is worked in the exceptional yield zone during the customary activity, and under some unusual conditions, i.e., fire up and short current, the proposed converter can be obliged into the low yield zone to manage the yield down to zero



(S3 gate and voltage)

B. Delicate Switching Characteristics of the Secondary Switches

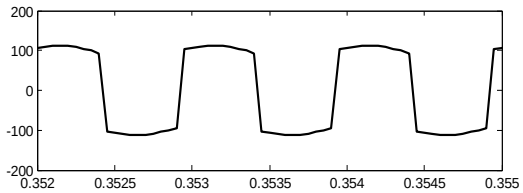
As exhibited in Fig. 4, each and every discretionary switch can procure ZCS liberated from the load condition. Sse2 is picked for example. As showed up in Fig. 4, Sse2 is ON during this stage, anyway the present traveling through Sse2 is zero as a result of the turnaround voltage applied to Do4. As showed up in Fig. 4, Sse2 is killed at zero current. Thusly, the trading loss of the discretionary switches can be restricted.

C. Yield Inductance :

The abatement of the yield inductance with TL helper changed voltage waveform has been discussed in [22]–[30]. As showed by [22]–[30], the essential yield inductance of the converters with TL assistant changed voltage waveform is around 33% of that of conventional two-level converters. Thusly, the volume of the yield divert in the proposed converter can be basic diminished.

D. VA Rating of the Transformer :

In the proposed converter, the VA rating of the force transformer is moved with the extent of the data voltage. In factor data and relentless yield action, Ts2 and Ts3 will move the whole essentialness to the pile forlorn under the most outrageous data electrical vitality. With decrease of the data voltage, the force moved by Ts2 and Ts3 to the yield reduces, and Ts1 and Ts4 are related with the force change system. Thusly, the full scale VA rating of the transformer in the proposed converter is possibly higher than that of standard TLCs, and the VA rating of the transformer is [27], [28], [30]:



(Vab)

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

$$VA = V_o I_o \left(2 - \frac{V_{inmin}}{V_{inmax}}\right) \quad \text{.....18}$$

According to (18), the rating of the transformer in the proposed converter is vague from that of the regular TLCs in the consistent data and variable yield movement. Thusly, the proposed converter is logically sensible for applications with truly coordinated data, i.e., downstream dc–dc converter after 3φ PFC converters.

E. Voltage Balance Principle of the Flying :

Capacitor The basic voltage on the flying capacitor is Vin/2 due to the course of action of the proposed converter. During the movement, the voltage on the flying capacitor can be kept up if this capacitor can watch a charge balance rule over each trading cycle. In the high return zone, as exhibited in Section II, the present coursing through Cfly is zero. Right now, electrical imperativeness on the flying capacitor can be stabled. In the low yield zone, the proposed converter can be treated as a customary capacitor cut TLC separated in [4]. As showed in [4], the voltage on the flying capacitor can moreover be stayed aware of an IAPWM strategy.

Commitment Ratio Loss :

In PS-controlled dc–dc converter, the effective commitment extent is to some degree more diminutive than the ideal a motivator on account of the nearness of the spillage inductance. Greater commitment extent mishap, mentioning the transformer go extent to be changed, may fantastically degrade the display of the converter. The commitment extent loss of the proposed converter is analyzed at this moment.1) High Output Zone:

The switching intervals are illustrated in Fig. 4 . The primary-side current is

$$i_p = \frac{2I_o}{k_T} - \frac{V_{in}}{2L_{lk}} \Delta t_T \quad \text{.....19}$$

$$\Delta t_T = \frac{6I_o L_{lk}}{k_T V_{in}} \quad \text{.....20}$$

$$\Delta D = \frac{\Delta t_T}{T_s/2} = \frac{12 I_o L_{lk} f_s}{k_T V_{in}} \quad \text{.....21}$$

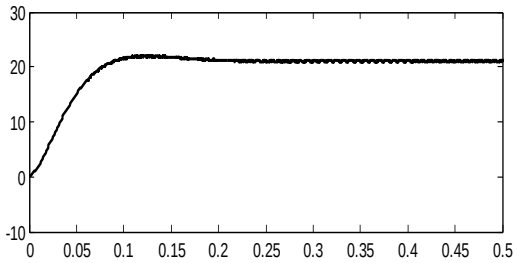
$$i_p = \frac{I_o}{k_T} - \frac{V_{in}}{2L_{lk}} \Delta t_T \quad \text{.....22}$$

$$\Delta t_T = \frac{4I_o L_{lk}}{k_T V_{in}} \quad \text{.....23}$$

$$\Delta D = \frac{\Delta t_T}{T_s/2} = \frac{8I_o L_{lk} f_s}{k_T V_{in}} \quad \text{.....24}$$

IV. COMPARISON

The proposed converter is contrasted and the regular capacitor clipped TLC and a joined TLC with four essential switches right now. The circuits of the converters for correlation are given and the detail activity standard about these converters can reference [4] and [26].



(Vout)

The proposed converter and the converter are accepted to be worked in the exceptional yield zone. Table IV shows the parts relationship among these converters. The current and VA assessments relationship of the crucial and right hand parts are given.

A. Key Power Devices:

As showed up in Table IV, the proposed converter and the converter have the base number of the key force contraptions. Progressively unassuming number of the fundamental force contraptions recommends increasingly moderate BOM cost similarly as less capricious and consistently diminished essential structure. Also, less area in the essential side of the proposed converter and the converter is required to guarantee safe electrical open door by virtue of progressively unpretentious number of the central pieces and less problematic

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

relationship among these parts. At this moment, central circuit volume of the anticipated converter might be increasingly minor and decreased, which is dynamically speaking to high-consolidate industry applications. The present worry of the major switches is inconceivably lopsided. The present worry of S3 and S2 is around various events stood apart from that of S1 and S4 . The lopsided current weight stream may cause a few issues, i.e., the affirmation of fitting switches, the present sharing issue among proportional related parts, the multifaceted thought of drive circuits, and the arranging of warmth sink. This is another obstruction of the converter . As showed in [26], fundamental current courses through area diodes during free-wheeling stages; accordingly, the propping diodes and the chief switches are undauntedly embraced to be encouraged into one force module by the maker to guarantee safe development. Notwithstanding the manner in which that the makers of power gadgets have given some composed diode secured TL power modules, the voltage and current evaluations, picked range, cost, and the presentation of these modules are as of not long ago bewildered showed up distinctively corresponding to overall utilized two-level HB power modules. In this manner, the proposed converter and the converter in grant the clients to accomplish high-input dc–dc power change by essential accessible, progressively reasonable, and exceptional execution two-level force modules without security requital.

B. Flying Capacitor :

In the exceptional yield zone, as showed in Figs. 4 , no basic current goes through Cfly in the proposed converter. The proposed converter is relied upon to be worked in the low yield zone just during some peculiar development conditions. In this way, the indispensable current rating of Cfly in the proposed converter is progressively small. The voltage rating of the flying capacitor in the proposed converter and the converter is indistinguishable, and the worth is 0.5 per unit. The voltage rating of the two flying capacitors is 0.25 per unit. Concurring ,Cfly in the proposed converter has the littlest VA rating. For the secured development, the voltage swell on the flying capacitor ought to be controlled reasonably. This can be developed by picking appropriate estimation of the flying capacitor. The voltage swell on the flying capacitor can be organized as

$$\Delta v\_cfly=\int\_0^(T\_s⁄2)i\_cflydt.....25$$

As indicated by (25), the key capacitance of the flying capacitor in the proposed converter is near nothing. The principal capacitance association of the flying capacitors versus yield current and exchanging rehash is laid out with following questions: The voltage swell on Cfly is set to be 5 V; the yield current is differed from 10 to 200 A; the exchanging rehash is changed from 20 to 50 kHz. As when the yield current is 200 A, the crucial capacitance of the flying capacitor is around 68 μF with 20-kHz exchanging rehash, while the fundamental capacitance of the flying capacitors is around 280 μF under a practically identical condition, yet in the proposed converter, a film capacitor with increasingly small capacitance is satisfactory, i.e., 1 μF, by virtue of no present courses through this capacitor in the exceptional yield zone. Considering the circumstance of the low yield zone, a 5-μF film capacitor can be utilized. In this way, the flying capacitor in the predicted converter has the most minor capacitance. Most minor VA rating and capacitance of Cfly in the proposed converter derives humblest volume of the flying capacitor. Furthermore, littler current worry of the flying capacitor gathers longer working life time, which is bolstered in high-voltage dc–dc applications because of its colossal action in keeping up off-state voltage of the fundamental switches.

C. Lethargic Magnetic Components :

As showed by Table IV, the VA rating of the force transformers is progressively minute in factor input voltage and steady yield voltage applications .When the data voltage go is 2:1, the hard and fast VA

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

rating is about 0.67 events showed up differently relating to that of various converters, regardless in the persevering information electrical vitality and variable yield voltage applications, the VA rating of the transformers in these three circuits is cloudy. The yield inductance of the converter is around different times of that of the other two converters due to the two-level voltage waveform before the yield channel. In addition, the volume of the information channel of the converter is similarly generally noticeable. As necessities be, the general connecting with region volume of the proposed converter and the converter is close to nothing. The evaluation of the transformer structure is delineated in Fig. 13. As showed up in Fig. 13(c), the four discretionary curves in Fig. 10(b) are interleave plan related. This befuddling relationship among the associate circles may raise an immense measure of sifting through and gathering tumult especially under gigantic yield current applications. In addition, this incredible union may in like way cause astutely parasitic inductance, which contaminates the show of the converter. As showed up in Fig. 13(a), the accomplice bits of the proposed converter are procedure related, and the structure is increasingly direct meandered from that of the converter in Fig. 10(b). As spread out in Fig. 13(b), the transformer of the converter in Fig. 10(a) has the most clear structure.

D. Parts and Structure of the Secondary Side:

As appeared in Table IV, the proposed converter has the most extreme auxiliary power gadgets number. As delineated in Fig. 11(e), the present worry of the rectifier diodes in every converter is indistinguishable, yet as the quantity of the rectifier diodes in the proposed converter is twice contrasted with that of Fig. 10, the necessary semiconductor territory of the rectifier diodes of the proposed converter is the most elevated. Additionally, as appeared in Fig. 11(f), two auxiliary switches are included. Accordingly, the auxiliary circuit of the proposed converter is somewhat perplexing and expensive contrasted with its rivals because of two included rectifier diodes, two included dynamic switches, comparing door drive circuits, and extra tapping on the optional side of the transformer.

E. Duty Ratio Loss:

The maximum duty ratio loss of the proposed converter is decided by (21).According to [4], the duty ratio loss of is

$$\Delta D_1 = \frac{8 I_o L_{lk} f_s}{k'_T V_{in}} \quad \text{.....26}$$

$$\Delta D_2 = \frac{16 I_o L_{lk} f_s}{k_{T2} V_{in}} \quad \text{.....27}$$

$$k_T = 2k'_T = 3k_{T2} \quad \text{.....28}$$

$$\Delta D_1 = \frac{8 I_o L_{lk} f_s}{k'_T V_{in}} = \frac{16 I_o L_{lk} f_s}{k_{T2} V_{in}} = \frac{4}{3}\Delta D \quad \text{.....29}$$

$$\Delta D_2 = \frac{16 I_o L_{lk} f_s}{k'_T V_{in}} = \frac{48 I_o L_{lk} f_s}{k_{T2} V_{in}} = 4\Delta D \quad \text{.....30}$$

As appeared in (21), (29), and (30), the obligation proportion loss of the proposed converter is most reduced among the three converters with a similar estimation of Llk , Vin , and fs .F. ZVS Load Range The ZVS load scope of the essential switches of the proposed converter is given in Table III, and the ZVS load scope of the converters in Fig. 10 is introduced in Table V[4], [26]. As per Table III, every single essential switch can accomplish full-load go ZVS in the high yield zone. As appeared in Table V, the main switches can likewise get ZVS in wide burden extend because of the vitality put away in the yield inductance can be utilized, yet these essential switches can't get ZVS down to zero burden current. As recommended in Table V, the slacking switches will confront more trouble because of just vitality put away in the spillage inductance can be utilized. The ZVS load scope of the slacking switches is somewhat more extensive contrasted with that of because of the vitality put away in two spillage inductances can be used.

G. Power Loss:

The disaster evaluation is given in Table VI. For the focal side, the proposed converter has the humblest

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

effect disaster as a result of least trading trouble, no free-wheeling circumnavigating conduction event, and no additional cut-out diodes. For the discretionary side, the effect scene in the proposed converter is fairly higher on account of two included right hand switches, regardless the extra trading mishap is littler as a result of the ZCS action, and the extra conduction disaster is in like manner logically minute in view of progressively minor conduction deterrent of the accomplice switches. For a 800-V information and 50-V/200-A yield converter, 50-V MOSFETs can be used as Sse1 or Sse2. The extra conduction tribulation is about 0.003 per unit, and the extra misfortune may be in like manner lessened in better return applications. In like manner, the proposed converter will have higher adequacy among the converters for relationship especially under no store, high repeat, or high data movement.

In sharp cross area systems, dc interfaces for cut back scale structures and reasonable effect source appropriated control structures will pull in more thought as a result of various focal centers showed up contrastingly comparing to that of cooling interfaces, for instance, no keep resolute quality issue, littler change control hardship, lower structure cost, and clear structure control. The data electrical imperativeness of these dc interfaces is normally extraordinarily high to achieve better everything thought about system execution. From this time forward, shocked dc–dc converter for higher voltage rating changes into a hot issue.Depicts two potential express stunned dc–dc converters subject to the proposed converter and the converter. The fundamental circuit is less mind boggling and tenaciously superfluous looked. The VA rating of the partner parts is only appropriate to the power rating and not loosened up with the proportion of the focal cells. The suddenness of the partner structure is in like manner not connected with the proportion of the fundamental cells. Moreover, with fitting masterminding, the converter has the sum of the focal points having a spot with the converter in Fig. 1. Subsequently, unequivocal paralyzed converter subject to the proposed converter is a promising response for high information electrical essentialness applications. The improvement standard and execution of the converter isn't offered here to the clarification behind straightforwardness. In passed on control structures, some dc interfaces may be referenced to have free controllable multi yield ports is another deducted topology reliant on the proposed converter, which has two autonomous controllable yield ports, at any rate no deducted topology subject to the converters can cause them to regulate controllable multi yield ports thinking about the basic standard system. The advancement standard and utilization of the converter in isn't offered here to the clarification behind straightforwardness. From above assessment, we can expect that the proposed converter has powerfully possible expansion topologies with phenomenal execution to fit undeniable high-input applications isolated .

A model is attempted to affirm the showing of the proposed converter. The standard parameter of the model is sifted through around there. The data for the structure are as demonstrated by the going with. The data voltage is separated from 600 to 800 V. The yield voltage is 50 V, and the yield current is 200 A. Trading repeat of the chief switches is set as 20 kHz.

A. Turn Ratios of the Transformer:

In the model, kT (I = 1, 2, 3, 4) are organized by the information voltage expand, and their characteristics are figured by

$$k_{Tsi} = K_T = \frac{V_{in,max}\, D_{MAX}}{V_O} = \frac{600 \times 0.85}{50} = 10.2 \approx 10 \ldots\ldots\ldots\ldots\ldots 31$$

B. Primary Power Switches :

The voltage rating of the essential switches is chosen by Vin max/2, which is 400 V in the model. Considering the electrical vitality spike during the activity, 600-V IGBTs is utilized. The present worry

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

of IGBTs ought to be structured under most extreme obligation proportion, and its worth is

$$i_{IGBT} = 1.5 \times \frac{2I_{o,max}\ D_{MAX}}{k_T} = 51(A.....32$$

C. Secondary Switches:

As demonstrated by Tables II and III, the voltage rating of the helper switches is picked by Vin max/2kT , which is 40 V in the model. Considering the voltage spike during the movement, 50-V MOSFETs are adequate. In the model, 60-V MOSFETs are used by looking at MOSFETs datasheet. The present stress of MOSFETs should be arranged under most outrageous discretionary commitment extent, and its value is

$$i_{MOSFET} = 1.5 \times \frac{2I_O D_{MAX}}{k_T} .....33$$

D. Rectifier Diodes :

As showed by Tables II and III, the most extraordinary voltage rating of the rectifier diodes is picked by 2Vinmax/kT , which is 160 V in the model. Thusly, 200-V fast recovery diodes are used. The present stress of the rectifier diodes should be organized under most outrageous discretionary commitment extent, and its value is

$$i_{diode} = 1.5 \times I_{O,max} = 300A.....34$$

E. Output Filter

$$L_o = \frac{0.172 V_o T_s}{\Delta i_{Lpeak}} = \frac{0.172 \times 50 \times 50 \times 10^{-6}}{60}.....35$$

$$x_{Co} = \frac{2\sqrt{2}\Delta V_o}{\Delta i_{Lpeak}} = \frac{2 \times 1.414 \times 0.5}{60} = 0.023.....36$$

In (36), the RMS estimation of the yield voltage swell ΔVo is 0.01 Vo max. Thusly, Co is picked by (36) and contrasting capacitor datasheet, which is 1000 μF in the model.

F. Flying Capacitor :

During the regular action, no present travels through this capacitor. Right now, film capacitor with tinier capacitance is adequate. Contemplating the movement of the low yield zone, a 5-μF/5-A (450 V) film capacitor can be used.

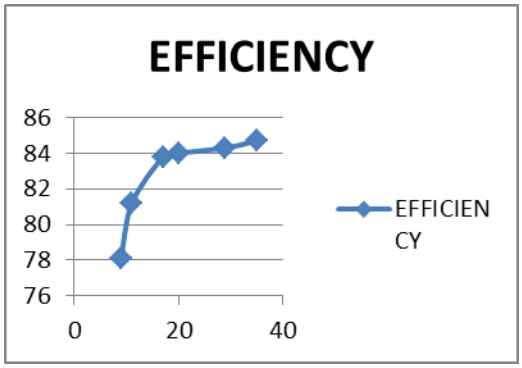
The show of the foreseen converter is developed by a 10-kW model, and essential parameters are discussed in the past section. In the adequacy test, the converters in Fig. 10 are furthermore test for connection. The waveforms of the showed converter in the low yield zone resemble standard capacitor propped TLC; in like manner, only waveforms in the exceptional yield zone are obliged the motivation behind straightforwardness. As the off-state voltage of the fundamental switches in the foreseen converter is in any occasion, during normal action stages, and the voltage of Cfly is relentless and counterparts Vin/2. As exhibited the voltage applied to the fundamental twist is Vin/2, and iLl k is definitely not a reliable worth in light of the fact that im is reached out to help ZVS of the basic switches. As im isn't in arrange with the stack current, the extra fundamental RMS current is humbler. Also, the extra conduction setback is in like manner tinier. The commitment extent of Tp is 100% and uncontrolled during the movement; thusly, there is no basic free-wheeling coursing conduction hardship. The waveforms of vrect ,iLo , and vDo 2 are given . As showed in the discretionary altered voltage is a TL waveform, which generally lessens the volume of the yield channel. The yield voltage and the channel source voltage of Sse 1 are given . As Sse 1 is executed with ZCS, there is no away from of the yield electrical essentialness at trading snapshots of the discretionary switches. The ZVS characteristics of the basic switches in the proposed converter are given , and the results are gotten with 10% evaluated load current. In the passage maker voltage of S1 is a great deal of lower than the entryway maker edge voltage when the gatherer maker electrical imperativeness of S1 reduces to zero, right now can get ZVS. Concurring the voltage on S1 increases from zero to indisputable voltage after the entryway signal decreases to zero, so the mind-set executioner loss of S1 can in like manner be constrained. As S4 can moreover get ZVS in wide weight expand. The waveforms of the channel source voltage and current of Sse 1 are shown Sse 1 can get ZCS. The electrical imperativeness

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

waveform of Cfly is depicted . The stack current is varied from 80% to 0% and changed from 0% to 80% . As, vC fly can tail one-segment of the information voltage suitably at these dynamic minutes. As showed vC fly can tail one-part of the data electrical essentialness fittingly. During the capability test, the converters are furthermore test for assessment, and the converters for connection are arranged under a comparable standard. the viability assessment under different weight stream with 600-V input electrical imperativeness and 20-kHz trading repeat. As all the basic switches can get ZVS in wide weight go, the proposed converter has higher adequacy at the light weight zone. The capability assessment with different data voltage with a consistent weight and 20-kHz trading repeat is given, and the adequacy of all converters lessens with augmentation of the data voltage. As the charging inductance can supply continuously reverberating imperativeness, the proposed converter has higher profitability under high information condition. The capability of the converter with 30-kHz trading repeat is higher adequacy relationship: (a) Variable yield current fs = 20 kHz, (b) variable data voltage fs = 20 kHz, (c) variable yield current fs = 30 kHz, and (d) variable information voltage fs = 30 kHz.of various converters. Right now, proposed converter is well suitable for high trading repeat applications. The capability of the proposed converter reduces a little with growing changing repeat from 20 to 30 kHz. This capability dropping is generally achieved by the mind-set executioner loss of the basic switches. An equivalent related capacitor can be added to each fundamental change to diminish the temperament executioner trading disaster. Nevertheless, a colossal equivalent related capacitor may require greater estimation of Im to ensure the ZVS of the fundamental switches, and the basic conduction hardship may augment hence. Right now, will be a tradeoff among turn-on hardship, turn-off setback, and conduction incident in different applications.(a) Ts = 50 μs; (b) Llk = 10 μH; (c) Cos = 0.001 μF.

S.NO	LOAD CURRENT (Amps)	OUTPUT POWER (Watts)	INPUT POWER (Watts)	EFFICIENCY (%)
1	9	197.4	252.6	78.13
2	11	209.2	257.7	81.2
3	17	277.6	331.3	83.78
4	20	314.3	374.1	84
5	29	333.3	393.4	84.31
6	35	403.9	478.3	84.7



IV. CONCLUSION

Another capacitor cut delicate exchanging TLC with two included partner switches is proposed. The development rule and qualities of the demonstrated converter are talked about, and some exploratory outcomes are given. The upgrades of the proposed converter are progressively clear and persistently decreased essential structure, TL optional reconsidered voltage waveform, increasingly minor duty degree difficulty, wide weight run ZVS for every single basic switch, and full-yield supervised go with delicate exchanging activity. The proposed converter can be reached out to higher voltage level effectively because of less irksome and consistently lessened basic structure. What's more, the proposed converter is comparably well reasonable for dc interfaces inside ward controllable multi yield ports. The proposed converter in like way has several downsides. The VA rating of the transformer is somewhat more prominent than normal TLCs in factor information and resolute yield applications. The optional circuit is somewhat befuddling and exorbitant considering two included rectifier diodes, two included novel switches, seeing gateway drive

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

circuits, and extra tapping on the aide side of the transformer. Future work may incorporate.

1) Topologies, control system, and relationship among various TLCs with two included unfathomable switches.

2) Operation rule and execution of surveyed bewildered dc–dc converter subject to the proposed converter.

3) Operation rule and execution of TLC switch free controllable multi yield ports.

REFERENCES

1. J. R. Pinheiro and I. Barbi, "The three-level ZVS PWM converter—A new thought in high-voltage DC-to-DC change," in Proc. IEEE Ind. Electron. Control Instrum. Autom. Int. Conf., 1992, pp. 173–178.
2. J. R. Pinheiro and I. Barbi, "Wide weight broaden three-level ZVS-PWM DCto- DC converter," in Proc. IEEE Annu. Power Electron. Spec. Conf., 1993, pp. 171–177.
3. X. Ruan, B. Li, Q. Chen, S. Tan, and C. K. Tse, "Focal considerations of three-levelDC–DC converters: Topologies, examinations, and control," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 11, pp. 3733–3743, Dec. 2008.
4. E. Deschamps and I. Barbi, "An assessment among three-level ZVS-PWM isolated DC-to-DC converters," in Proc. IEEE Annu.Ind. Electron. Soc. Conf., 1998, pp. 1024–1029.
5. I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "DC/DC converter for high data voltage: Four switches with top voltage of Vin/2, capacitive turn-off disdaining, and zero-voltage turn-on," in Proc. IEEE Annu. Power Electron. Spec. Conf. Rec., 1998, pp. 1–7.
6. E. Agostini and I. Barbi, "Three-organize three-level PWM DC-DC converter," IEEE Trans. Power Electron., vol. 26, no. 7, pp. 1847–1856, Jul. 2011.
7. D. V. Ghodke, K. Chatterjee, and B. G. Fernandes, "Adjusted softswitched three-organize three-level DC-DC converter for high-power applications having extended commitment cycle run," IEEE Trans. Ind. Electron., vol. 59, no. 9, pp. 3362–3372, Sep. 2012.
8. L. Fuxin, H. Gaoping, and R. Xinbo, "Three-organize three-level DC/DC converter for high data voltage and high-power applications grasping indeed, even commitment cycle control," IEEE Trans. Power Electron., vol. 29, no. 1, pp. 56–65, Jan. 2014.
9. W. Li, Y. He, X. He, Y. Sun, F. Wang, and L. Mom, "Course of action astray half-associate converters with voltage auto balance for high information voltage applications," IEEE Trans. Power Electron., vol. 28, no. 8, pp. 3665–674, Aug. 2013.
10. Y. Xiaoyang, J. Ke, and L. Zhijun, "Capacitor voltage control methodology for half-associate three-level DC/DC converter," IEEE Trans. Power Electron., vol. 29, no. 4, pp. 1557–1561, Apr. 2014.
11. A. Lopez, R. Diez, G. Perilla, and D. Patino, "Assessment and connection of three topologies of the ladder amazed DC/DC converter," IEEE Trans.
12. Power Electron., vol. 27, no. 7, pp. 3119–3127, Jul. 2012.
13. W. Li, P. Li, H. Yang, and X. He, "Three-level forward-flyback organize move ZVS converter with fused game plan related coupled inductor," IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2846–2856, Jun. 2012.
14. P. Das, M. Pahlevaninezhad, and A. Kumar Singh, "An epic weight adaptable ZVS aide circuit for PWM three-level DC-DC converters," IEEE Trans. Power Electron., vol. 30, no. 4, pp. 2108–2126, Apr. 2015.
15. Z. Yun, S. Jian-Tao, and W. Yi-Feng, "Hybrid assistance three-level DC-DC converter with high voltage gain for photovoltaic age systems," IEEE Trans. Power Electron., vol. 28, no. 8, pp. 3659–3664, Aug. 2013.
16. M. Narimani and G. Moschopouos, "A three-level joined AC-DC converter," IEEE Trans. Power Electron., vol. 29, no. 4, pp. 1813–1820, Apr. 2014.
17. X. Ruan, L. Zhou, and Y. Yan, "Fragile trading PWM three-level converters," IEEE

Published by: The Mattingley Publishing Co., Inc.

January – February 2020
ISSN: 0193-4120 Page No. 13773 – 13787

Trans. Power Electron., vol. 16, no. 5, pp. 612–622, Sep. 2001.
18. F. Canales, P.M. Barbosa, and F. C. Lee, "A zero-voltage and zero-currentswitchingthree level DC/DC converter," IEEE Trans. Power Electron., vol. 17, no. 6, pp. 898–904, Nov. 2002.
19. J. L. Duarte, J. Lokos, and F. B. M. VanHorck, "Stage move controlled three-level converter with diminished voltage stress including ZVS Over the full movement broaden," IEEE Trans. Power Electron., vol. 28, no. 5, pp. 2140–2150, May 2013.
20. S. Yong and Y. Xu, "Wide range sensitive trading PWM three-level DC– DC converters fitting for current applications," IEEE Trans. Power Electron., vol. 29, no. 2, pp. 603–616, Feb. 2014.
21. E. Chu, X. Hou, H. Zhang, M. Wu, and X. Liu, "Novel zero-voltage in addition, zero-current trading (ZVZCS) PWM three-level DC/DC converter using yield coupled inductor," IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1103–1117, Mar. 2014.
22. I.- O. Lee and G.- W. Moon, "Examination and plan of a three-level LLC course of action reverberating converter for high-and wide-input-voltage applications," IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2966–2979, Jun. 2012.
23. X. RuanandB. Li, "Zero-voltage and zero-current-trading PWMhybridfull-interface three-level converter," IEEE Trans. Ind. Electron., vol. 52, no. 1, pp. 213–220, Feb. 2005.
24. F. Liu, J. Yan, and X. Ruan, "Zero-voltage and zero-current-trading PWM joined three-level DC/DC converter," IEEE Trans. Ind. Electron., vol. 57, no. 5, pp. 1644–1654, May 2010.
25. S. Yong and Y. Xu, "Zero-voltage trading PWM three-level full-associate DC-DC converter with wide ZVS load broaden," IEEE Trans. Power Electron., vol. 28, no. 10, pp. 4511–4524, Oct. 2013.
26. S. Yong and Y. Xu, "Wide-run sensitive trading PWM three-level united DC–DC converter without included basic propping devices," IEEE Trans. Power Electron., vol. 29, no. 11, pp. 4511–4524, Oct. 2014.
27. D.- Y. Kim, J.- K. Kim, and G.- W Moon, "A three-level converter with reduced channel size using two transformers and flying capacitors," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 46–53, Jan. 2013.
28. R. Ayyanar and N. Mohan, "Novel sensitive trading DC–DC converter with full ZVS-run and diminished channel essential—Part I: Regulated-yield applications," IEEE Trans. Power Electron., vol. 16, no. 2, pp. 184–192, Imperfection. 2001.
29. R. Ayyanar and N. Mohan, "Novel sensitive trading DC–DC converter with full ZVS-broaden and diminished channel need—Part II: Constantinput, variable-yield applications," IEEE Trans. Power Electron., vol. 16,no. 2, pp. 193–200, Mar. 2001.

Published by: The Mattingley Publishing Co., Inc.