FPGA Based Control of Single Phase Three-Level Soft Switching Isolated DC-DC Converter

J.Sivavara Prasad[1], G.Nageswara Rao[2], K.R.L.Prasad[3]
[1,2,3]Professor, EEE Department
Lakireddy Bali Reddy College of Engineering
Mylavaram, Krishna Dt, A.P, India
e-mail: janapatisivavaraprasad@gmail.com

Article Info
Volume 82
Page Number: 11593 - 11599
Publication Issue:
January-February 2020

Article History
***Article Received**: 18 May 2019*
***Revised**: 14 July 2019*
***Accepted**: 22 December 2019*
***Publication**: 21 February 2020*

Abstract
The single phase three level isolated DC-DC converter consists of four control switches operate under ZVS However, the single-phase three-level isolated DC-DC soft switching converter has been proposed in order to reduce voltage and current stresses. This converter topology requires less number of control switches and operates with an asymmetrical duty cycle control. The proposed three level DC-DC converters provide two- level voltage waveform before dc output filter, which significantly reduce the size of dc output filter. The proposed work has been implemented using MATLAB/SIMULINK and the performance of the proposed converter is verified experimentally by using FPGA controller.

Keywords: *Isolated DC-DC Converter, Switching losses. Zero voltage Switching(ZVS), FPGA Controller and Three-Level*

I. INTRODUCTION

The astonished power converters have heap of thought because of reasonableness for high data voltage applications [1]. The dc–dc converters and astonished inverters are executed with semiconductor contraptions evaluated at a humble amount of dc voltage, which are consistently more beneficial and more moderate than their high-voltage-surveyed associates. Since the multifaceted thought of astounded converters is reached out on an extremely essential level by the measure of levels, which limits the advantages of paralyzed converter, most of endeavors in dc–dc dazed converter have been bargains on three-level converters. Basically, dc–dc three-level converters outfit control change with semiconductor gadgets surveyed at one-portion of the information dc voltage. The specific confined three-level dc–dc converters have been appeared in [2]–[5]. To besides improve their presentation, the four-basic gadgets worked under delicate exchanging. In particular, the topologies in [2]–[4] gives zero voltage exchanging, anyway the topology in [5] gives ZVS and ZCS. The colossal evaluation among the topologies exhibited in [2]–[6] is in the control of gadgets. The topologies in [2] and [3] utilize tireless recurrent beat width balance control, anyway the topologies in [4]-[6] utilize unsurprising rehash sort out move control.

DC-DC converters store essentialness in accomplice degree contraption, device or every all through action. This imperativeness is then coursed to the pile over a measure of some time. This transport of the hold tight imperativeness is drilled with capability by factor the charging time for the essentialness storing device, dependent upon the pile, for each time period[2]-[5]. The charging chief measure identifies with the change movement of the flexibility contraption that is obliged by accomplice degree external apparatus. Dependent upon whether or not relate degree yield device is used, high-repeat DC-DC modification converters

TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 11593 - 11599

zone unit assigned isolated or non isolated [6]-[8]. For isolated DC-DC converters, the superior styles of converters district unit as seeks after: buck, support, buck-lift and Cook. Regardless, in an enormous segment of the sharp applications, partition is required for the DC-DC converters, that encapsulate some wide used topologies, much equivalent to the fly back, forward, push-pull, half-augmentation and full framework converters[8]-[10].

Astounded diode-clipped converters are of basic since they have less number of capacitors than flying-capacitor converters and are not required free different voltage sources when stood apart from dazed course converters. The zero voltage zero current exchanging (ZVZCS) and ZVS three-level half development converters have been considered, at any rate these converters face the issue that they just gives half of the dc input voltage to the essential of transformer proposed in [7], [8]. High control move can be given a full-interface topology, yet it is a basic errand to build up a genuine changing course of action to give touchy changing activity to all the power switches. Starting not very far in the past, this has been able for ZVS three level full stage acknowledged in [8] and for three-sort out three level ZVZCS converter made in [9].

To make the full dc input voltage to the central of transformer, a solitary stage three level isolated DC-DC converter is proposed. The single stage three level isolated DC-DC converter contains four control switches work under ZVS.

II. SINGLE PHASE THREE-LEVEL ISOLATED DC-DC CONVERTER:

The Figure 1 shows the circuit structure of single-organize three-level DC-DC converter. The four switches S1-S4 work under ZVS. The DC-DC converter change contains two phases to be express, dc-cooling stage and cooling dc organize. The high recurrent transformer in the circuit is utilized to make electrical limitation among load and source. The optional turning of high recurrent transformer is an inside tapped one and it requires altering diodes to change over

The high recurrent transformer in the circuit is utilized to make electrical partition among load and source. The optional bending of high recurrent transformer is an inside tapped one and it requires auditing diodes to change over transformer aide cooling voltage into dc voltage. The Figure 3 gives the operational waveforms of the proposed converter.

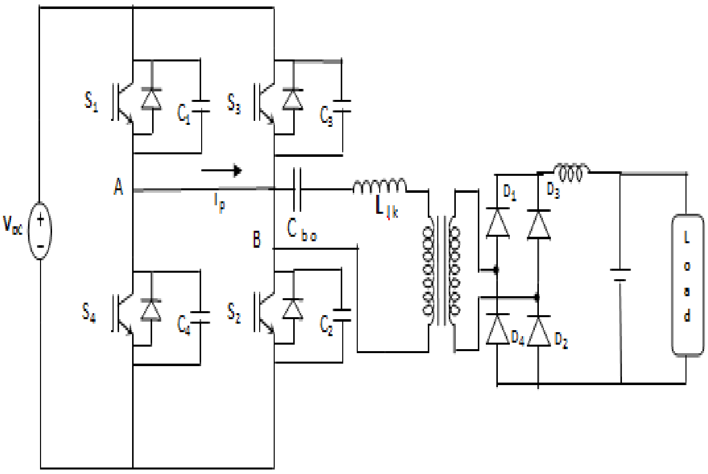

Fig.1. Single Phase Three-Level ZVS DC-DC converter Topology

Fig. 2 shows the entry beat time of proposed converter. Here, the reference wave is separated and triangular wave.

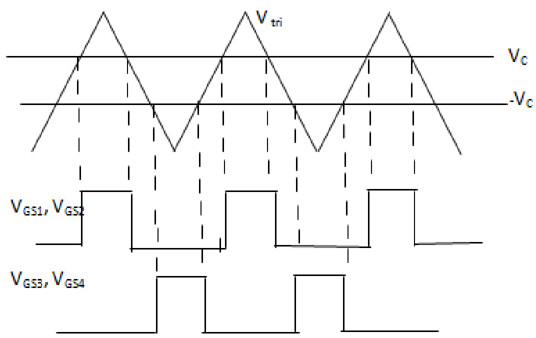

Fig. 2 : Gate Pulses generation

The control switches (S1,S2) and (S3,S4) are getting same gateway beats. On the off chance that the control switches S1 and, S2 are working then +Vdc shows up transversely over essential of the transformer. On the off chance that the switches S3 and S4 are working, by at that point - Vdc shows up transversely over fundamental of the transformer. Precisely when no switches are on then the central of transformer gets zero. The best dead time is made between the switches S1&S3, S2&S4 to source block. The transformer spillage inductance and intermingling capacitances are utilized to make touchy exchanging system the essential side of transformer. The curing diodes D1 - D4 are utilized to change over cooling input voltage from optional of transformer into dc yield voltage. The dc channel parts Lf and Cf are utilized to make rectifier yield voltage waveform into unadulterated dc voltage with good cutoff motivations behind wave content.

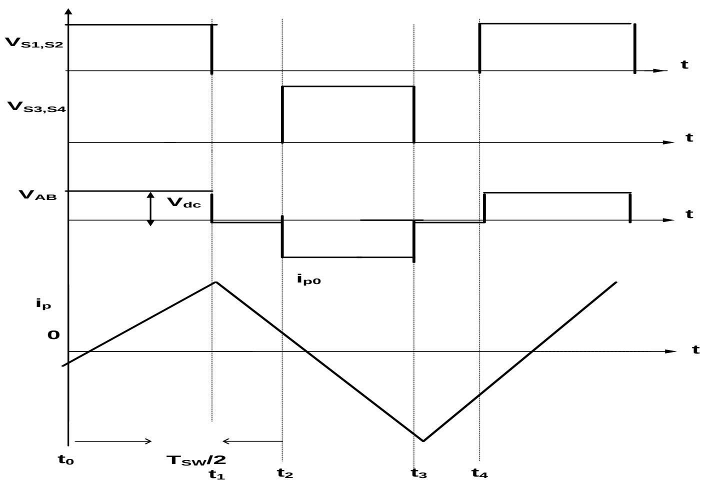

Fig 3. Operational waveforms

2.1 OPERATION MODES

Theoperational procedures for the proposed converter are appeared in Figures 4 (a) to 4 (d). The goings with suppositions are made in the activity: (I) the control switches are perfect. (ii) the yield channel inductor ought to be huge enough to make yield present as unsurprising current source. (iii) the blocking capacitor is gigantic enough to go about as a dependable voltage source in any event, when the current being reset.

Operational mode 1: $t_0 \leq t \leq t_1$

Because of spillage inductances in the transformer essential and partner, the major current is still not came to zero.

The value of primary current from mode 4 to mode 1 is

$$i_p(\mathrm{t}) = \frac{V_{dc}+N_T V_0}{L_{kp}}(t - t_0). \quad (1)$$

The man-sied organisation square of the fores en diverse Field DC DCdévieIs show éd up in Fig. 3. The first and second Fields zone unit arrange witzord voltage-mode shunt circule the bocard, how ver the Thiard Field Is organise move Controller. All the organisation signaux an area unit frome CLOCK signal watt, white experiencing the hall move circuit the cloc signal Isconcède by recasons in time φ.

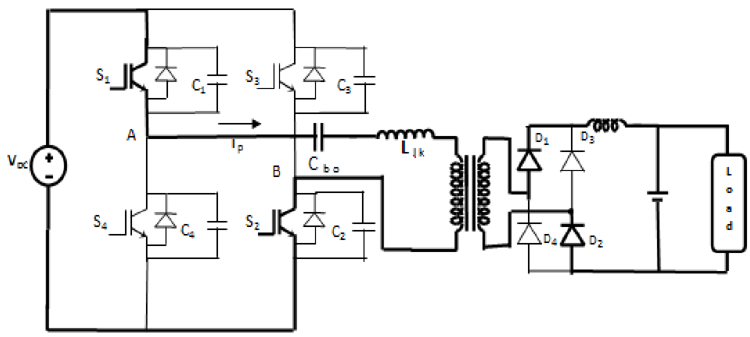

Fig 4.a Equivalent circuit for mode '1' operation($t_0 \leq t \leq t_1$)

Operational Mode 2: $t_1 \leq t < t_2$

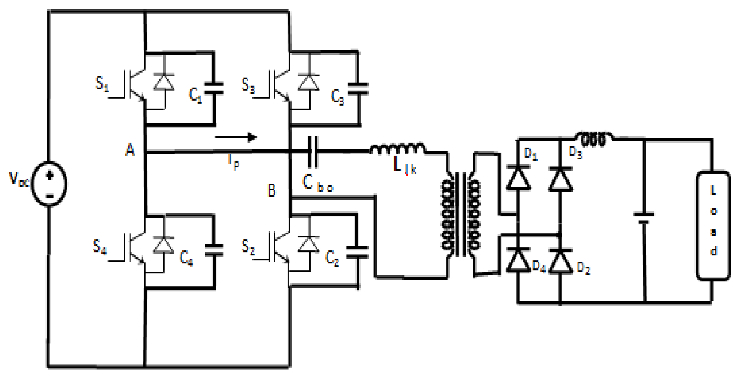

Fig 4.b.Equivalent circuit for mode '2' operation($t_1 \leq t \leq t_2$)

The essential outputis controlled th rough the obligation cycle of the principal uneven zero.5 scaffold gadget That comprises of. The Thiardoutputis managed th rough the obligation cycle of the second topsy-turvy zero.5 scaffold gadget That comprises of switchers. upheld the half move between the initial two uneven zero.5 extension converters, the subsequent yield Is controlled.

Operation Mode 3: $t_2 \le t < t_3$

At time t=t2, the switches S3 and S4 are turned on under ZVS. Because of spillage inductances in the transformer, the current in the circuit can't change out of the blue from positive to negative as appeared in figure 4(c).

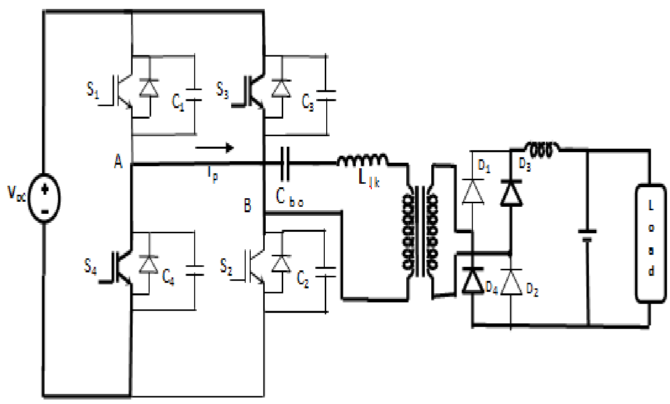

Fig 4.c.Equivalent circuit for mode ‘3’ operation($t_2 \le t \le t_3$)

Operation Mode 4: $t_3 \le t < t_4$

The switches S3 and S4 are butchered at t3. Capacitors C3 and C4 are charged and C1 and C2 are released by ip, which is up to this point held consistent at Ipo by the huge yield channel inductance. When C1 and C2 are totally released to zero and body diodes of S1 and S2 are start practices to pass on the present which gives ZVS condition to the switches S1 and S2 as appeared in figure 4.d.

Switches S1and S2 can be gated ON under complete at whatever point after t4. Since this mode is so short, Vcb0 is recognized to stay persistent at-Vcb0p for the term of this mode.

$$T_{reset} = t_4 - t_3 = L_{lk} * \frac{I_{p0}}{V_{cb\,0p}} \quad (2)$$

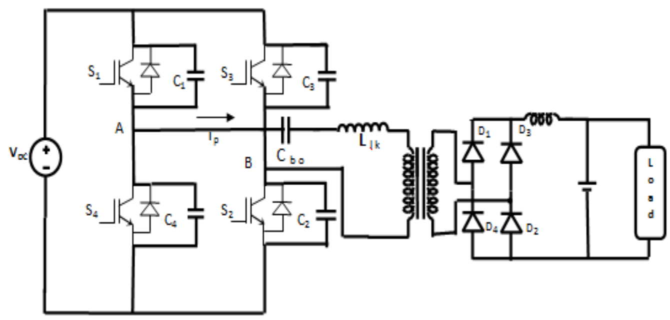

Fig 4.d.Equivalent circuit for mode ‘4’ operation($t_3 \le t \le t_4$)

III. SIMULATION RESULTS:

The make sense of 5 see beats of the proposed converter switches. Palatable dead time (tdead) is made between the control switches S1&S4 and S3&S2 to maintain a strategic distance from the source square. The dead time is settled dependent on the going with condition

$$t_{dead} = C_r * \frac{V_{dc}}{I_{p0,min}} \quad (3)$$

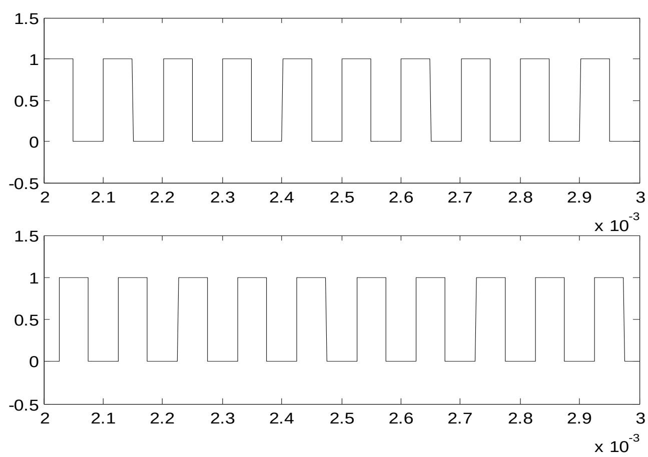

Figure.5.Gate pulses for S_1 and S_2, S_3 and S_4

January - February 2020
ISSN: 0193 - 4120 Page No. 11593 - 11599

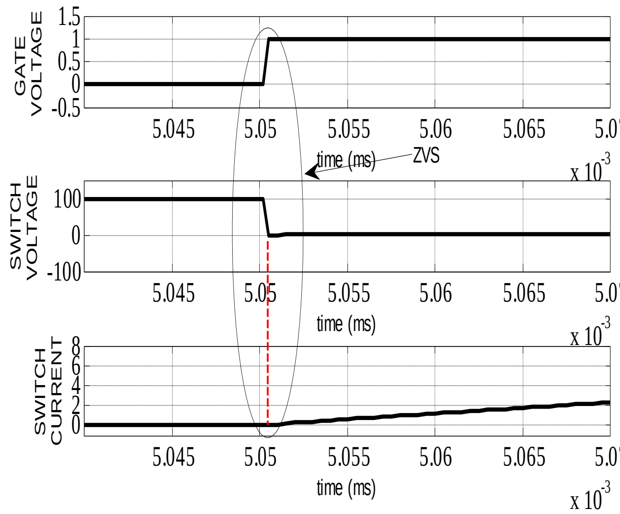

Figure 6: Gate voltage, voltage across and current through switches S_1& S_2 during OFF to ON

Figure 6 shows gateway voltage, voltage transversely completed and current through switches S1 and S2 for the exchanging progress period from off state to on state. Precisely when the entryway beats are applied to S1 and S2, by then the switches S1&S2 are turned on and current encounters the change from time t=5.052ms, it is seen that the voltage crosswise over switch is so far zero yet current beginnings broadening, it shows that the exchanging impact episode is zero during progress period from off state to on state. That derives ZVS is developed for S1 and S2.

Make sense of 7 sees voltage, voltage transversely completed and current through switches S1&S2 during on to off change period. From figure 2.19, the continue to kill change of switches S1&S2 is happened from the time 5.1ms to 5.1005ms. The power current of S1&S2 begins tumbling from 5A to focus in this interim, where as the gatherer creator voltages of S1&S2 are propped to zero because of their normal capacitors C1&C2. As necessities be, the switches S1&S2 are work under ZVS during on to off change minute and no exchanging force incidents right now.

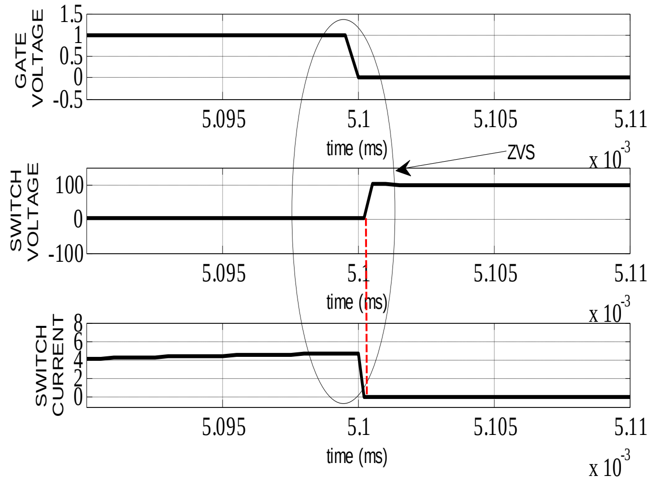

Figure 7: Gate voltage, voltage across and current through switches S_1& S_2during ON to OFF

Fig 8(a) shows the waveforms for essential and right hand voltages of the transformer and figure 8(b) shows the dc changed yield voltage with channel.

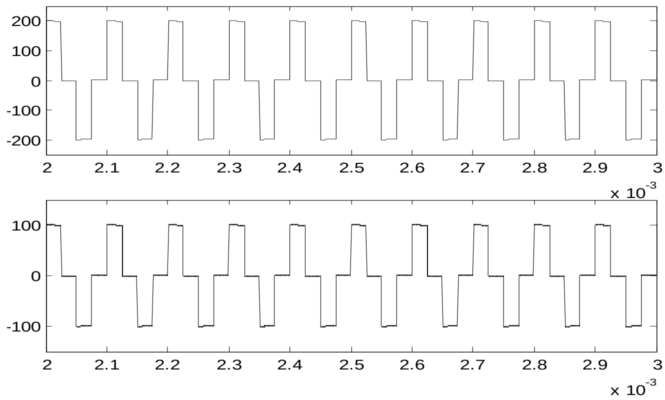

Figure.8(a). Transformer Primary and Secondary voltages

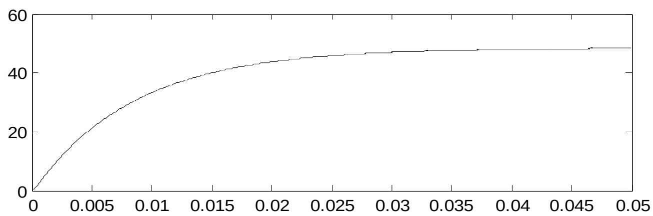

Figure.8(b). Rectified dc output voltagewith filter

5. Experimentation:

January - February 2020
ISSN: 0193 - 4120 Page No. 11593 - 11599

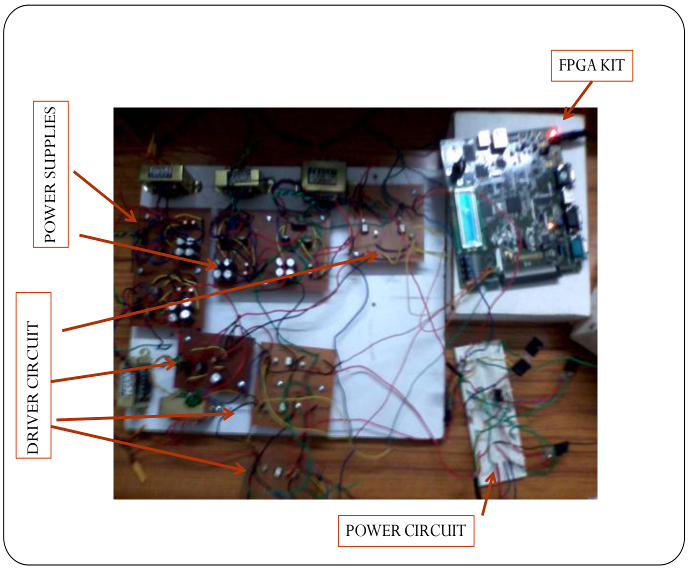

Fig.9. Experimental Setup

The figure 9 shows the test strategy of the general converter structure. The make sense of 10 sees beats of the proposed converter with FPGA controller.

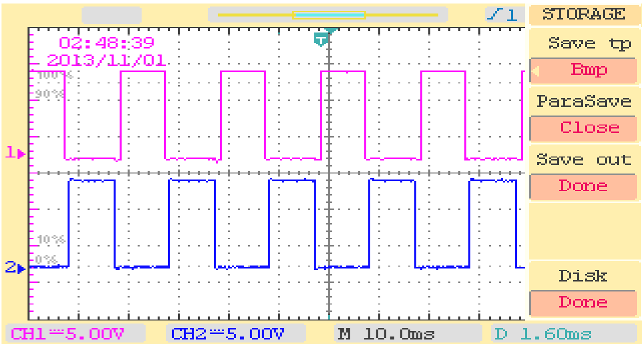

Fig 10.Generation of pulses through experimentation

The figure 11 shows the three level voltage waveform in the fundamental time of transformer. The levels are 0, Vdc and – Vdc.

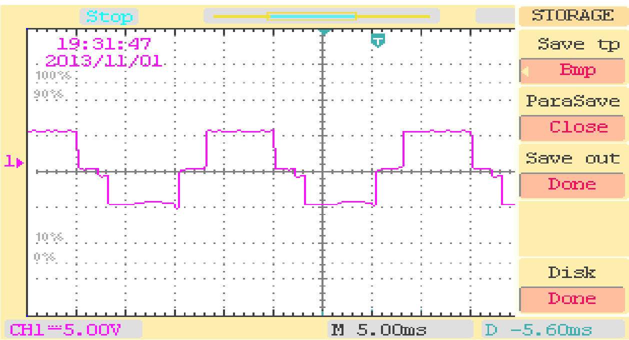

Fig 11. Waveform for Inverter output voltage

Make sense of 12 sees heartbeat and voltage crosswise over switch S1. It is apparent from figures 13(a) and 13(b) that before executing ON and before turning the switch, the voltage transversely over change comes to zero and in this way delicate exchanging is developed.

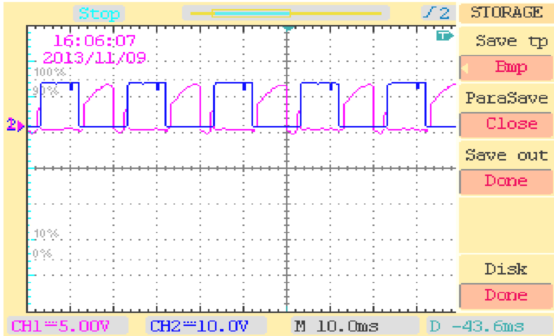

Fig 12 . Waveform for Gate pulse and voltage across switch S_1 andS_2

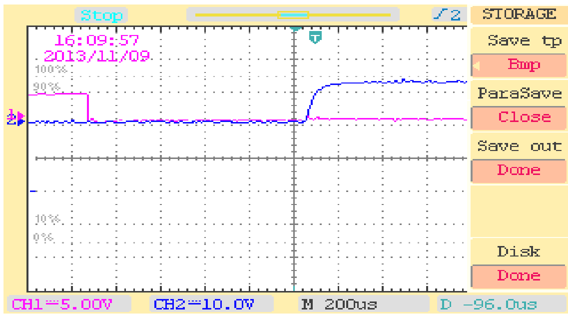

Fig 13.(a) Waveform for Gate pulse and voltage across switch S_1 andS_2 during On to Off

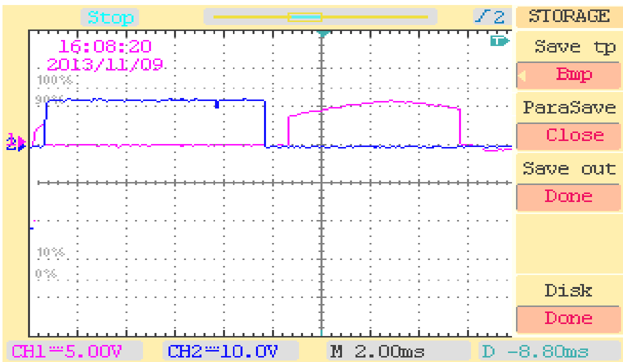

Fig 13.(b) Waveform for Gate pulse and voltage across switch S_1 andS_2 during Off to On

The figure 14 shows the explored yield voltage waveform. The channel is organized with swell substance of under 3%.

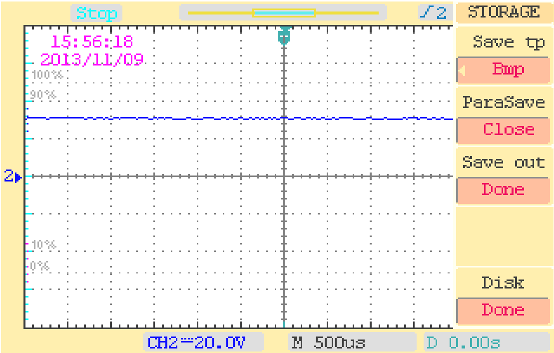

Fig 14. Waveform for filtered rectified dc output voltage

IV. CONCLUSION

The proposed single-orchestrate three-level isolated DC-DC converters have the upsides of delicate exchanging and three-level voltage waveform in the essential side of transformer. The size of yield dc direct s diminished in 1-sort out three-level DC-DC converter topology. The size of spillage inductance of high recurrent transformer was more modest for accomplishing touchy exchanging. Henceforth, the expense and exchanging hardships were decreased to an inexorably prominent degree, therefore improves the general productivity of a DC-DC converter. The introduction of proposed converter has been watched likely and the outcomes are totally lovely.

V. References

[1] C Bor-Renn Lin, and Chia-Hung Chao, “Analysais of Interleaved Thrènelève ZVS convertirwitzsériesconnecte transformer," *IEEE Transe. on Power Electroniques*, vol. 28, no. 7, pp. 3088-3099, July 2013.

[2] P. dos Santos Garcia Giacomini, J. S. Schultze, M. Mekarbi, "Steph-Up/Steph-Down DC–DC ZVS PWM ConvertirWitz Active Camping," *IEEE Transe.onIndustrialoElectroniques*, vol. 55, no. 10, pp. 3635-3643, Oct. 2008.

[3] Bor-Renn Lin, Chien-Lan Huang, Jin-Fa Wan, "Analysais, Design, and Implémentation of a Parallèle ZVS Convertir," *IEEE Transe.onIndustrialoElectroniques*, vol. 55, no. 4, pp. 1586-1594, April 2008.

[4] Finke Wu, Kunming Zhang, XI Yee, ZhaoqingQian, "Analysais and Dérivations for a Familier ZVS Convertir Base on a New Active Clamp ZVS Cella," *IEEE Transe.onIndustrialoElectroniques*, vol. 55, no. 2, pp. 773-781, Fe 2008.

[5] Chien-Ming Wang, Ch’ing Hung Su, Mao-Chin ilang, Yan-Chun Lin, "A ZVS-PWM Single-Phase InvertirUsina a Simple ZVS-PWM Commutation Cella," *IEEE Transe. onIndustrialoElectroniques*, vol. 55, no. 2, pp. 758-766, Fe 2008.

[6] Hybrida Full-Bridge Thrène-LèveConvertirWitz Seconder-Voltage Camping Schème," *IEEE Transe.onIndustrialoElectroniques*, vol. 55, no. 2, pp. 644-654, Fe 2008.

[7] TAI-Fu Wu, Yue-Sheng Lai, Jinchuan Hung, Yalow-Ming Chen, "BoostaConvertirWitz Couple Inducteurs and Buck Boosta Type of Active Clamp," *IEEE Transe. onIndustrialoElectroniques*, vol. 55, no. 1, pp. 154-162, Jan 2008.