TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 11558 - 11562

Implementation of Cascaded Switched Diode Multilevel Inverter for Photovoltaic Integration

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Article Info
Volume 82
Page Number: 11558 - 11562
Publication Issue:
January-February 2020

Article History
Article Received*: 18 May 2019*
Revised*: 14 July 2019*
Accepted*: 22 December 2019*
Publication*: 21 February 2020*

Abstract
In recent times, significant research has been carried out on Multi-Level Inverters (MLI), due to their importance in various applications such as renewable energy system and drives. Generally, multilevel inverters use more number of switches, which require more installation space and cost .The major focus of current research is to obtain a high quality output with less number of switches.Dual stage cascadedswitcheddiodemultilevel inverter methodology ispresented in this paper.A positive staircase output is obtained in the first stage. Full wave output voltages are generated by applying phase opposition disposition technique adding full bridge inverter in the second stage. The proposed method has benefits of minimized number of components and less total harmonic distortion. The proposed methodology is carried out using MATLAB/SIMULINK and its performance is analysed.

Keywords: *Multi level inverter (MLI), Cascaded switched diode (CSD) multi level inverter, Phase opposition and disposition (POD).*

I. **Introduction**

Nowadays, the need for renewable energy is growing due to the increasing demand of electrical energy and depletion of traditional energy sources. Solar PV and wind turbine are widely usedrenewable energy sources. All these renewable sources need power electronic circuitry for interconnecting to grid/ load. The main power electronic component needed is inverter as shown in figure1 (a) and 1(b)

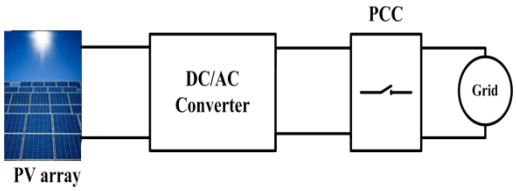

Fig.1(a) PV array connected to grid

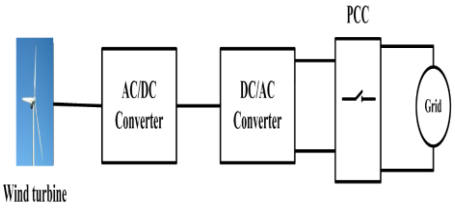

Fig .1.(b). Wind energy source connected to grid

A conventional two level inverter produces a two-level voltage output with reference to the common negative terminal. Whereas three or more than three inverters having an output level are called as MLI [1-3]. MLIs have several applications such as FACTS, renewable energy systems, drives, UPS and aircraft systems, etc.[4], [5]. The output voltage of the MLIs is the stepped waveforms and these inverters made up of symmetrical and asymmetrical voltages with different switches like IGBTs, MOSFETs [6], [7]. In general, based on structure, MLIs are classified as three types and they are (i) Neutral Point Clamped (NPC), (ii) Flying capacitor and (iii) cascaded H-bridge inverter (CHB). The multi-level inverter for CHB is the conventional cascaded method[8],[9]and the major drawback of this method is number of switches required is more and its interrelated circuitry, which lead to a composite system and cost. The diode-clamped or NPC multi-level inverter uses a number of fixing diodes for higher levels and the balancing of capacitors which are joined in series is a big problematic [10]. Another problem of the diode-

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clamped inverter was power flow with capacitor inequality. The flying capacitor MLI needs a large number of capacitors and for the voltage balance of the capacitor control complex algorithms are needed [11].

The symmetric voltage structure of MLI has the benefit of modularity that itis easy to design. Two novelsymmetric MLI structures have been proposed in [12], [13]. The inverter topology reported in [12], is depended on a mixture of cascaded fundamental units and one H-bridge unit and the structure advised in [13], depended on the non-insulated voltage dc sources with compact number of switches. The disadvantage of these topologies isthat they require several numbers of switches and gate drivers. It increases control complication, circuit cost and size.Asymmetric voltage inverters based new structure has been reported in literature, which shrinks the number of switches and voltage sources as compared to CHB and flying capacitor inverters.

For making a huge number of output voltagelevels, the inverter wants several large numbers of IGBTs. To overcome these drawbacks, a novel asymmetrical voltage structure for the MLI may be used, but the disadvantage of this topology is the use of a full-bridge converter, which is restricted for levels which shrinks the number of IGBTs and can produce all levels (odd and even) at the voltage output. This topology has the need for a great number of IGBTs and gate drivers. The regularly used modulation control strategy techniques for different symmetrical or unsymmetrical MLIs are the essential frequency control methods i.e. the carrier-based sinusoidal pulse width modulation, the space vector modulation (SVM) and a few non linear control methods such as hysteresis control and sliding mode control.

Phase opposition and disposition control scheme has been developed for two-stage cascadedmulti-level inverter topologies in this paper. The developed control scheme gives less total harmonics disposition as compared to the conventional inverter. The proposed MLIconstruction extended to number of input conversion stages.

This paper isstructured as follows: Section 2 illustrates the circuit description of the proposed inverter. Section 3 demonstrates the simulation results of the proposed method. Finally, conclusions of this paper are represented in Section 4.

II.CSDtopology

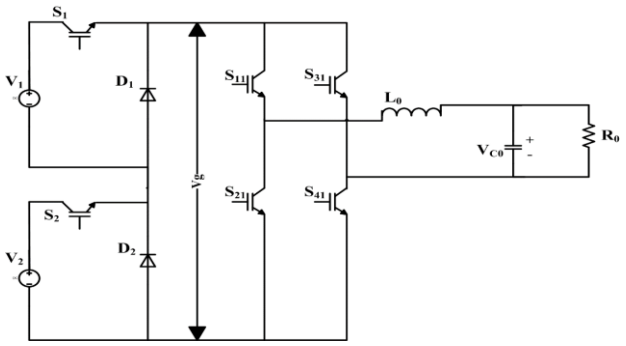

Fig.2: proposed dualstage CSDtopology

Figure2 explains the 2-stage CSD multi level inverter, which consists of a cascaded switched-diode converter and a full-bridge inverter. The proposed configuration has two stages. Stage-1includes a voltage DC source (voltage DC equal to V_1), switch $S_1$with internal inverse diode and diodeD_1.

The first stage is a dc source V1, an S1 switch with an internal inverse diode and a D1 diode. The parallel fitting of the diode D_1 helps to avoid the shoot through of bridge arm. In the fundamental stage, two values can be obtained for V_1: one, 'V_1'when switchS_1conducts and '0'when switch S_1 is turned OFF. When S_1 is on, $S_2$is OFF.., as listed in Table I.

Table1:- First stage output voltage

state	Switch states		Vg
	s_1	s_2	
1	off	off	0
2	on	off	V_1

As listed in Table I, the waveform of positive staircase-like output voltage can be produced by the

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first stage converter. The 2nd stage converter is required to produce maximum voltage output. The transfer state study for both positive and negative reference voltage is given in Table II.It is certain that the (+ ve) and (-ve) halves of the voltage output are obtained with the inclusion of the 2nd-stage.

Table2: Second stage output voltage

state	Switches states				V_0	Conditio n
	s_{11}	s_{21}	s_{31}	s_{41}		
1	on	off	off	on	V_g	$V_{ref} \geq 0$
2	off	on	on	off	$-V_g$	$V_{ref} < 0$

II.I.POD (Phase opposition disposition) Technique:

In POD method for MLI, (m-1) exporter waves are used. In which the exporter wave directly above the '0' reference are out of phase by 180^0 with exporter waves below '0' reference , but the exporter waves below reference are reflect image of exporter waves above reference. This method has superior harmonic performance at lower modulation files. Exporter wave and modulating wave and the gate pulse for upper and lower halves is shown in Figure3. And simulations are executed at unity modulation pointer, frequency 2kHz exporter and frequency 50Hz modulating

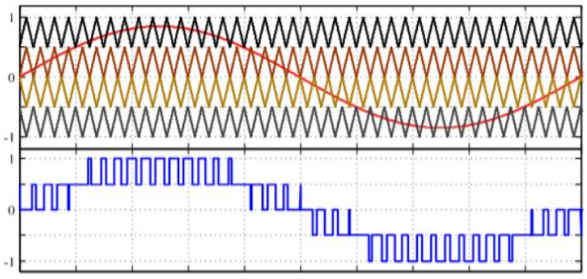


Fig 3: The proposed phase opposition disposition control scheme

Figure 4 represents the proposed block diagram of the phase opposition disposition control scheme for the proposed MLI. As shown in table 2, bycomparing the two OR gate outputs, the positive and negative voltage output of the proposed inverter's second stage isobtained. First stage of the proposed POD technique is only considered for the positive state. In the first stage sine wave is compared with two constants with a relational operator and the signal is given to gate signal switches of S_1 and S_2.

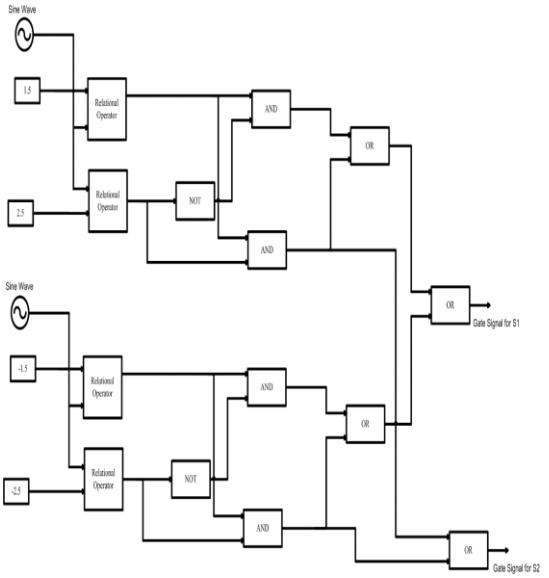
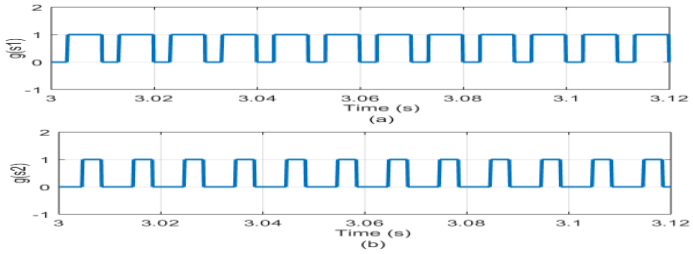


Fig.4. The Block diagram of phase opposition disposition control scheme

III. Simulation result

The proposed 5-level 2-stage CSD multi-level inverter is simulated at modulating frequency of 2500 Hz .The proposed parameter values for simulation are $V_1 = v_2 =$ 80volt , R = 50 ohm, L = $650x10^{-3}$H,C = 550 μF.

Fig5Gate signal for first stageat a)switch S_1



b)switch S_2

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The second stage inverter's gate signals are shownin Figure 6.As shown in Table2, when$v_{ref} \geq 0$.$S_1$and$S_4$are switched on. At this state, the voltage output $V_0 = V_g$ .When V_{ref} <0, S_1 and $S_4$are turned-off and $S_2$and $S_3$are turned on. Now the voltage output $V_0 = -V_g$ for the (-ve) half cycle. Thus binary (+ve) and (-ve) splits ofwaveforms are gained

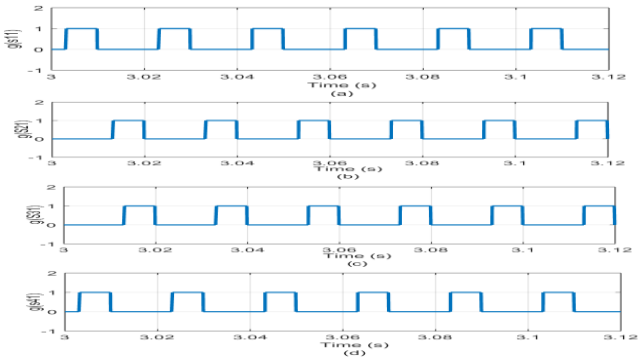
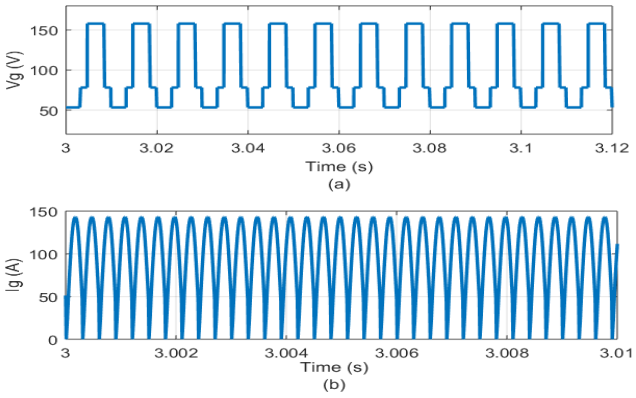


Fig.6. Switching sequence for second stage of multi-level inverter

Stage-1converter voltage output V_g , which is the sum of the cascaded units of all outputs, is shown in Fig. 7(a). And the first stage converter current output i_g has shown in Fig. 7(b).Fig.7. First stage output voltage and output current of Multi-level inverter



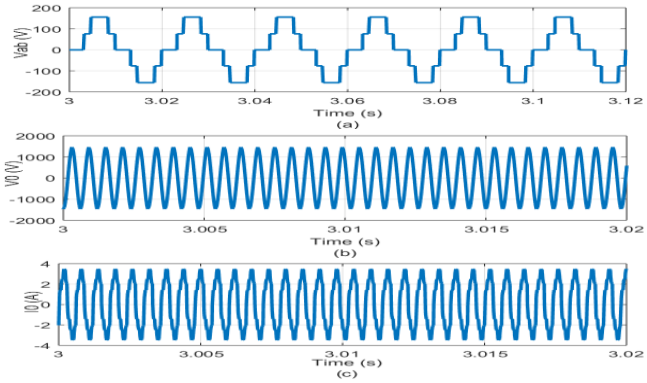


Fig.8.The multi-level inverter's second stage output voltage and current a). Output voltage before the filter is connected b). Output voltage after filter was connected c). Inductor current.

Fig. 8 illustrates stepped voltage output wave-form V_{CD} , the voltage output V and the inductorcurrenti$_L$.As shown in figure, V is a 50 Hz stepped fashion waveform, with no spikes of high voltage. The voltage and current output after LC filter are almost sinusoidal.

The THD of the stepped voltage output wave-form V_{CD} of the 5-level MLI is 16.31%, as shown in Figure. 9

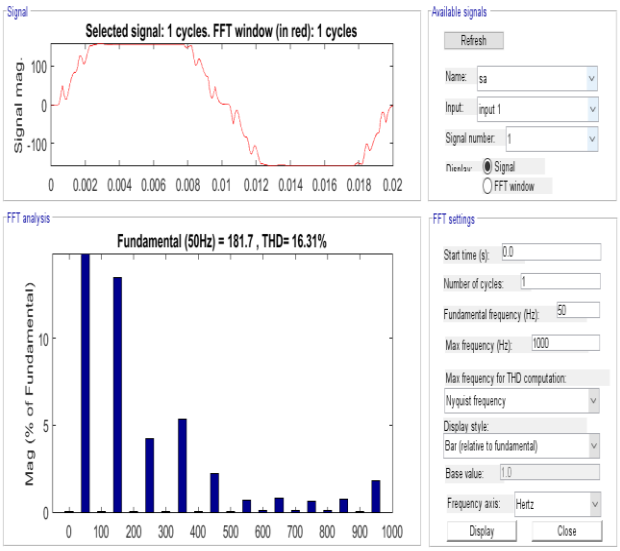


Fig.9.:The FFT analysis of the proposed multi-level inverter

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