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Power Optimization in 8T SRAM Cell using Bit Interleaving Concept

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Abstract:
Nowadays, power dissipation is the foremost concern in SRAM. This paper discusses about lowering power which is the central topic in SRAM design. The modified 8T SRAM cell improves the read steadiness and writes ability. Here, 8T SRAM with effective bit Interleaving is used to attain the soft error tolerance. The modified design will consume minus Power when associated to the 6T SRAM design and one cell is initiated at the time of read or write operation. Simulation results show the power consumption as 5.52 mw which is less when associated to the 6T SRAM. The Simulation is done via Tanner 13.0 tool.

Keywords: SRAM, Power dissipation, Stability, ability bit Interleaving.

1. Introduction

SRAM is an unstable memory which is quicker and consumes low power than Dynamic RAM. It is used in microprocessors, Portable devices, cache memories. Several methods have been engaged to distribute the requirement such as voltage, multi-threshold CMOS process to abate the leakage. By using these techniques large amount of energy will be saved and also the speed performance is improved. SRAM is established on the sensor which deals with the leakage [6]. Here, the optimum voltage of modified SRAM at which the energy consumption per read and write operation has been decreased. Many configurations in SRAM cell focus to improve the read failure by using separate read buffer [3].

The mandate for SRAM has been increased in large scale industries. SRAM occupies significant portion of System on Chip (SOC). SRAM consumes more power but refreshing operation is not required which is necessary for high speed devices. The memory design faces various issues like decreases noise margin [2]. The challenge is to develop a 8TSRAM cell which consume less power than conventional 6TSRAM. Dynamic voltage technique (DVT) is used to expand read steadiness and write ability. The SRAM array consists of sense amplifiers and address decoders [4]. Due to leakage current, the speed of devices and power decreases automatically [5].

This paper is systematized as follows. In Section II, the existing 8T SRAM. Section III, the modified 8T SRAM. Section IV, the Bit Interleaving architectures. Section V, proposed 8T SRAM with Power Reduction Technique. Section VI, results and simulation.

Section VII, Power comparison in SRAM cell. Section VIII, conclusion.

2. Existing 8T SRAM CELL Design

In conventional 6T SRAM, several critical issues were faced by the designer in declaim read and write operations. The newly designed 8T SRAM works promote two transistors to admittance the RBL. The 8T SRAM cell design was developed, where the read bit line, Write bit line and word signal lines are isolated, to detach the data retention and data output element. As a result, the modified 8T SRAM exhibits read-disturb-free function. Write function is done by write access method. Read function is done by the read admittance transistor and by RWL [2]. When the Read Bit Line (RBL) is not accessed, the leakage current causes a voltage drop that leads to power dissipation in the output. The below fig 1 spectacles the existing 8T SRAM.

January-February 2020
ISSN: 0193-4120 Page No. 10944 - 10947

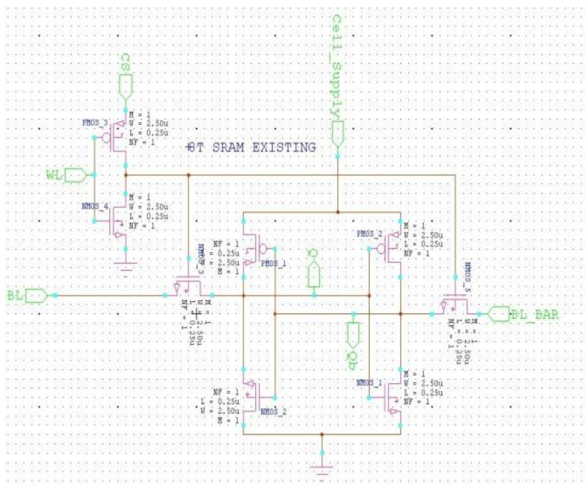

Figure 1: Existing 8T SRAM

3. Modified 8T SRAM CELL

The 8T SRAM CELL helps for read stability. It has one BL and two WL (WWL and RWL) and it's used for read and write operation. An CS supply is used for cutoff the feedback. Separate WL is used to regulate the read/write operation. WWL transfer data from BL to Q and opposite information store in QBAR. In this circuit two cross coupled invertor is used (left has 3T[1PMOS,2NMOS] and right has 2T[1PMOS,1NMOS]). During read operation, BL transfer data from cell as output when RWL is in ON condition. When 0 stored in Q, P3 turns ON and it's detected by sense amplifier. If 1 is stored in Q, P3 turns OFF condition.

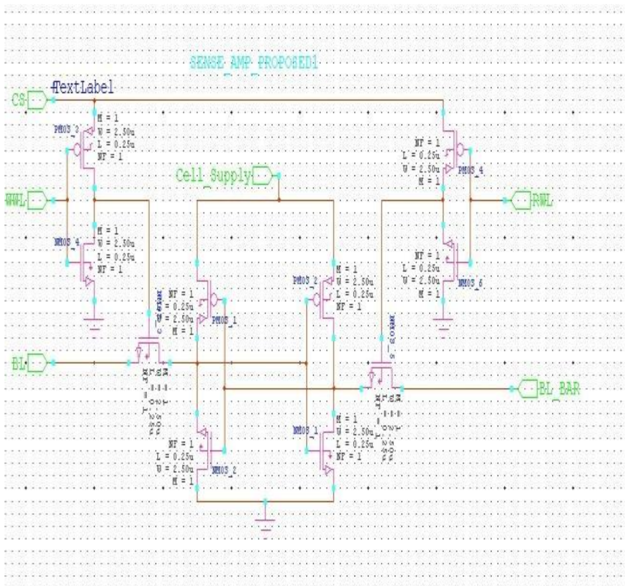

Figure 2: Modified 8T SRAM CELL

Write Operation

When write is in '0' condition, BL=0 and BLBAR =1 are the inputs given to circuit and WL is always in enable condition. The output 0 is kept in node Q and 1 is kept in node QBAR. When write is in '1' condition, BL=1 and BLBAR =0 are the inputs given to circuit. The output 1 is kept in Q and 0 is kept in QBAR.

Read Operation

In read operation, the values are deposited in Q and QBAR(Q=1 and QBAR=0). When QBAR is in '0'condition N5 turns ON and compare themselves shows difference, low voltage, capacitor will discharge and current will flow. So the output of BLBAR is 1 because of voltage decrease and BL=0.

Hold Operation

When WL is in HOLD condition, both WWL and RWL is in OFF condition.

4. Bit-Interleaving Architectures

Bits of same words remain situated next to each other. A NAND gate can be select only one word within N number of words in a row. The below Figure 3 shows the SRAM word organization Structure.

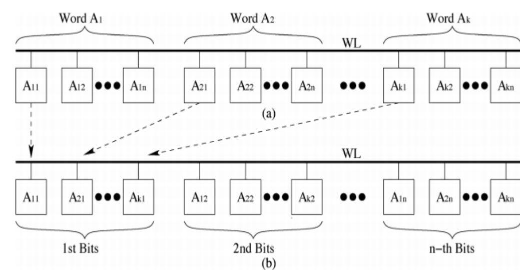

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Figure 3: SRAM word organization.

This architecture is commonly used because of its easiness and firmness. This has a negative result on chip. It has half-access issue during write operation [1]. The cell in the equivalent row will be active only if word line is high. Thus, disorders to the cell are lessened and simulations exposed that the cell is more balanced and less disposed to inaccuracy during operation [1].

5. Modified 8T SRAM With Power Reduction Technique

Write Static Noise Margin indicates the write ability of the cell. When the circuit is in hold mode, sleep transistor act as switch that power supply to the circuit [7]. The read and write operations are divided, to modify the 8T SRAM design, which is high. In adding to this, a ground erection is used during the write operation to decline the comment loop, which promote the write ability. The below Figure 4 shows the Modified 8T SRAM with Power Reduction Technique.

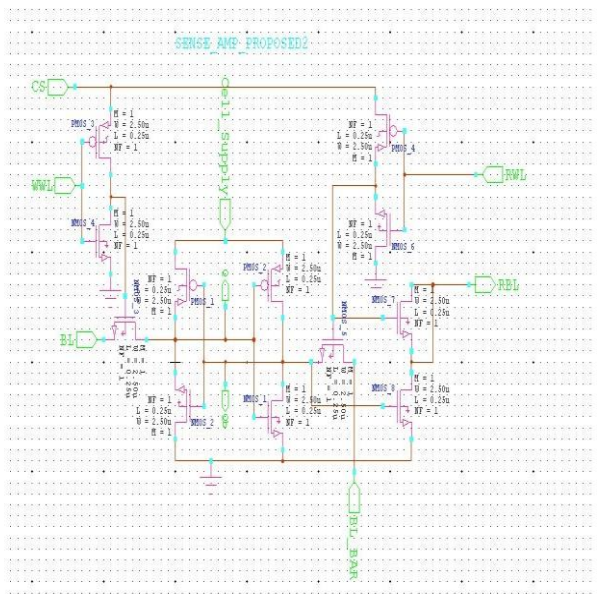

Figure 4: Modified 8T SRAM with Power Reduction Technique

6. Results and Discussions

The design and implementation of 8T SRAM is discussed. It achieves good read stability and write ability compared to the previous existing SRAM. Modified 8T has been compared with the various voltage with respect to power. For the period of read and write operation the power dissipation in SRAM shows functional constraints during active mode. The voltage is decreased in power. The output waveform of Modified 8T SRAM is shown in Fig 5.

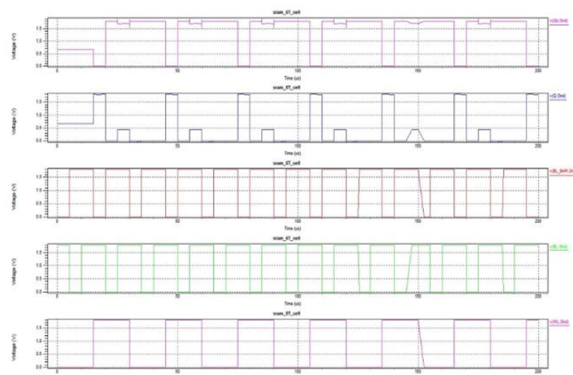

Figure 5: Modified 8T SRAM

The output waveform of Modified 8T SRAM with Power Reduction Technique is shown in Fig 6.

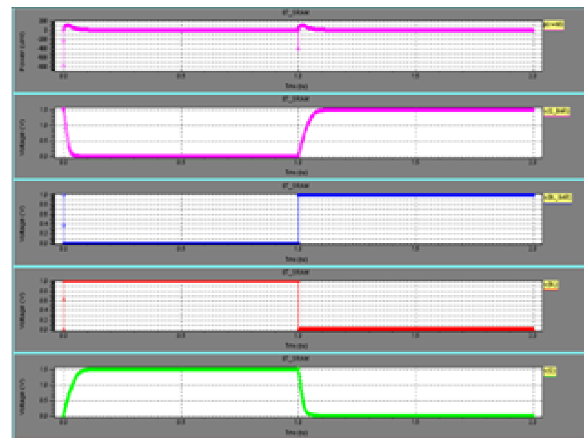

Figure 6: Modified 8T SRAM with Power Reduction Technique

7. Power Comparison in SRAM CELL

Simulated parameters have been shown in

Table 1: Power Comparison table

Different SRAM CELLS	Power Consumption (μW)	Delay
8T SRAM	9.79	5.44 ns
Proposed 8T SRAM	8.13	3.86 ns

Table 2: Comparison on basis of Frequency

Frequency	Power Indulgence in 6T (μW)	Power Indulgence in 8T (μW)
1 GHz	6.75	4.72
2 GHz	9.854	8.782

8. Conclusion

In this paper, power consumption is analyzed and 8T SRAM cell has been modified. In SRAM, the write power is commonly higher than read power. The Modified 8T SRAM cell provides power efficient solution. The simulated output of the modified 8T SRAM cell has high stability, decreased power, write ability and read stability.

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