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Quasi Z-Source Resonant DC-DC Converter with Improved Voltage Gain

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Abstract

A dc- dc resonant quasi z-source converter is proposed. The key features are high step-up / step-down ratio, high efficiency, low system voltage tension, and soft-switching, i.e. turn-on ZVS for all switches, and turn-on and turn-off ZCS for all diodes in both buck / boost operating state. The main switch also operates in the lower resonant while in the upper resonant the active clamp switch operate to maintain the zero voltage switching (ZVS) condition for the main switch and there are small switching losses. The transformer's leakage inductance was used to create the clamp capacitor resonant circuit. Low input current ripple produced by using a boost circuit at the input of the converter ideal for applications in fuel cells. Over a wide load range, the proposed converter accomplishes ZVS for switches and zero current switching (ZCS) for diodes. Device voltage without any snubber circuit is also clamped.

Keywords: Quasi z-source resonant converter, active clamp circuit, voltage doubler circuit

1. Introduction

Many inexhaustible originate, such as photovoltaic (PV) board and fuel cell stacks (FC) have low-voltage and high-current properties and require low-current ripples [7]. The use of these power sources includes a DC-DC converter with voltage isolation, low input current ripple, and high step-up ability that lead to high output. High switching frequency is thus the basis for a high-power density transition. For example, high frequency switching messes up, high loss for power, high voltage or current spikes, and all called electromagnetic interference (EMI). Soft-switching operation is used in DC-DC converters to wipe out these issues. An additional switch is attached to a standard DC-DC converter to provide a soft switching state. To maintain a soft switching state, an auxiliary switch is attached to a standard DC-DC converter. It is possible to classify the converters used for sustainable power assets into two critical classes that are current-fed and voltage-fed converters. Both high-power and low-voltage applications, such as FC's and PV's, these converters are increasingly reasonable. For current-fed converters, the most common topologies are full-bridge, half-bridge and push-pull converters [8].

2. Quasi Z-Source Resonant Converter

The circuit of input boost contains L_B boost inductor [3] and S_1 switch. The beginning side of a transformer's leakage inductance is illustrated as L_K and C_1 and L_K's leakage inductance is provided to the resonant circuit. The Active [10]clamp circuit is a C_2 and S_2 configuration. The diodes D_1 and D_2 make a full wave rectifier on the secondary side of the transformer, which makes the voltage double circuit capacitors C_{o1} and the balance of C_{o2} [12].

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Quick diodes are a little longer in view of the ZCS on the output diodes. In addition, load resistance is shown separately as R_L. N_1 and N_2 are the transformer's primary and secondary proportions. "N" is defined as n= N_2N_1. F_s and F_r are independently alternating frequency and resonant frequency. Figure 1 displays the planned converter circuit

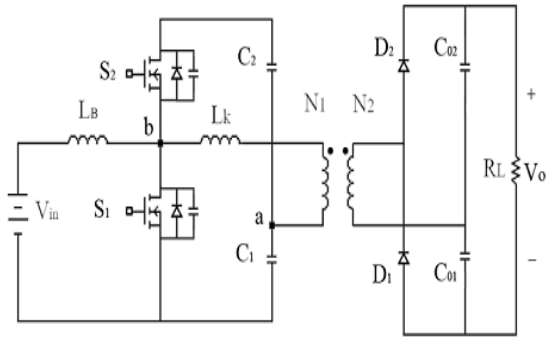

Figure 1: Quasi z-source resonant converter

Resonant converters that are acceptable for high-voltage and high-frequency functions are suggested in LLC. To achieve high voltage, the transformer's magnetizing inductance needs to be low, which increases magnetizing current and higher conductivity and core losses. A quasi z-source resonant (QZSR) current-fed half-bridge [4] is favored in figure 1. A traditional boost converter is replaced with an active clamp circuit [11]. There is soft switching for the converter to accept the active clamp circuit. A high-frequency transformer delivers galvanic isolation and increases the income voltage. In addition, the reverse recovery problem of the output diode was disposed of by a voltage doubler circuit at the yield and twice the voltage gain. In addition, the converter works in a quasi z-source [5] resonant state. In this circumstance, the current stress and loss of switches will be reduced to their base value, while the pulse width modulation (PWM) method can still restrict the converter [1]. As a matter of fact, the proposed converter embraces the resonant converter's soft-switching efficiency, and the conventional PWM converter's effortless control and use. By reducing the exchange loss of the proposed converter, it works at a higher frequency of switching. The quantity of parts is also small. Subsequently, the volume and weight of the present converter will be drop and its power density will be rise. In a wide range of load variety, this converter retains soft switching, but switches suffer the ill effect of high current pressure switches.

3. Circuit Operation

Six interims represent the operation of the proposed converter. Significant currents and voltage bend are concocted and working circuit process is appearing in fig 2. S_2 is switched ON at the time prior to t_0. It is agreed that the input current is worth I in view of the fact that the inductance L_B is high enough to improve the current wave of input. The other statement that C_2 voltage has a constant value of V_{C2}

Interim I [t_0~t_1]

Appearing in t_0, S_2 explode off and compares input and current transformer charges and releases separately parasitic capacitor of S_2 and S_1. The current pass forward by the switch S_1's body diode from that point. For whatever length of time this current runs along body diode, voltage is zero cross-sectional over S_1. In order to accomplish ZVS, gate signal can be applicable at the entrance. This transition will be done when the S_1 extends to zero reverse current.

Interim II [t_1~t_2]

Appearing in t_1, the switch S_1 [13] current changes its path and passes along the switch on the grounds that in the past interim S_1 has been switched ON. I circulated via s1 and source and V_{in} input charges L_B. The voltage V_{o2} has been added to the C_1 and L_k after t_0 by transformer primary winding. I_{Lk} drops to zero and the interval ends. The D_2 performance is performed. So:

$$-i_1 = \frac{-\frac{V_{o2}}{(n-V'_{C1})}}{L_K} d_1 T_s \quad \text{…….…... (1)}$$

$$d_1 T_s = t_2 - t_0 \quad \text{…… (2)}$$

V'_{C1} is voltage of capacitor C_1 at the time t_0

Interim III [t_2~t_3]

Appearing in t_2, changes in the transformer current bearing and voltage of the output capacitor C_{o1} are transmitted to the beginning side of the transformer by means of a transformer, and C_1 and L_k resonance. Once I_{lk} reaches zero, this period will be done. During this interim, the input inductance current over the input inductance L_B is increasing due to V [6]. In view of changing the transformer current in this interim, the secondary current bearing is too modified, so that D_1

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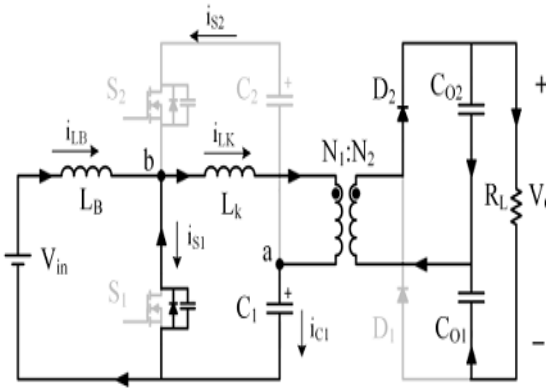
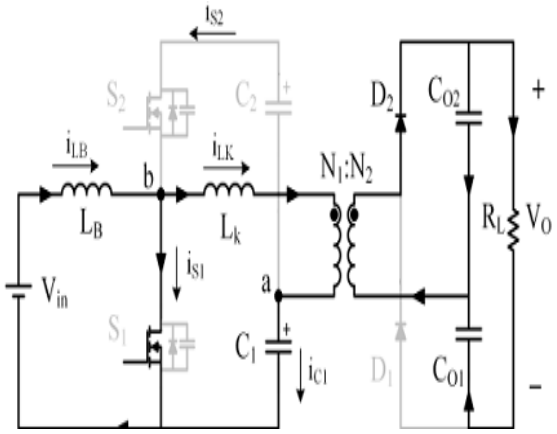
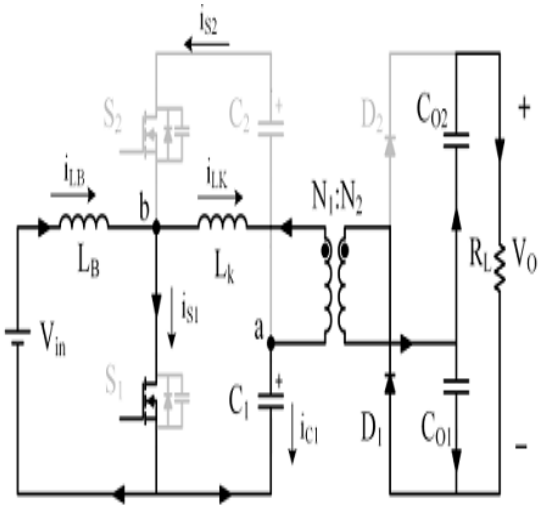
leads to the doubler output circuit and provides the C_{o1} [9] output capacitor.



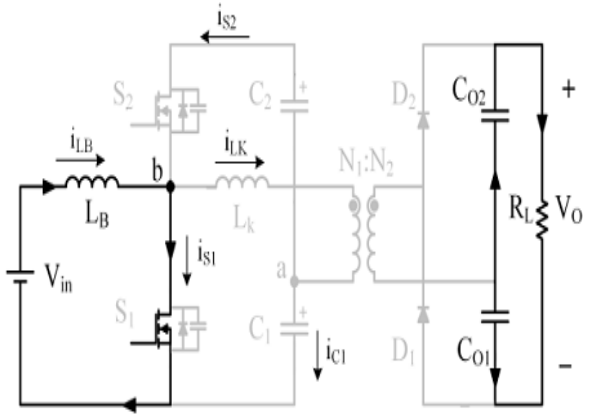
Interim I



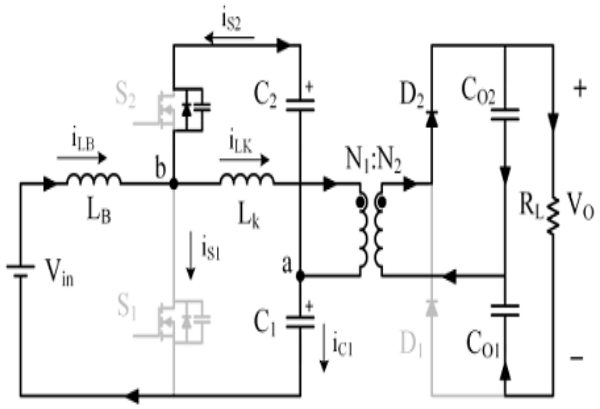
Interim II



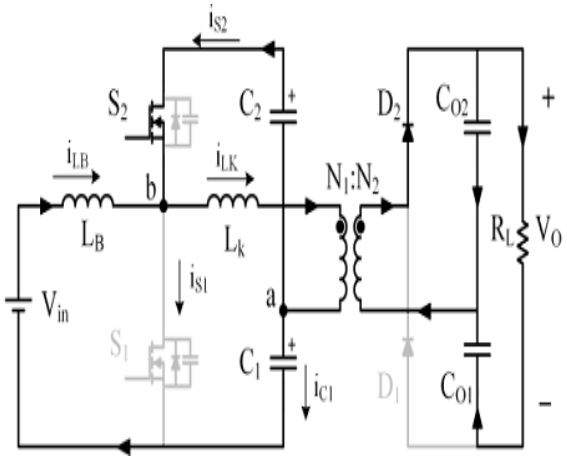
Interim III



Interim IV



Interim V



Interim VI

Figure 2: Working Methods of QZSR dc-dc converter

Interim IV [t3~t4]

The interval begins at the point where the transformer current falls to nil. Capacitor C_1 and inductor L_k converts power to output and converter's activity goes to irregular conduction mode (DCM). Voltage over the transformer and capacitor C_1 reach to V_3 , yet the current of S_1 remainder I_{in} in whole this interim and the power supply charges the inductor L_B . In view of the graph

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appeared in figure 2 by request volt-second equalization to the transformer's primary turn:

$$d_1V_1 + d_3V_3 = d_2V_2 \ldots\ldots\ldots\ldots \quad (3)$$

The diodes are switched OFF at the output as the secondary current is zero. So supply the heap in this interim output capacitor (C_{o1} and C_{o2}).

Interim V [t_4~t_5]

Appearing in t_4, S_1 turns OFF and input contrast and transformer charges current and releases individual S_1 and S_2 parasitic capacitors. The current pass by the switch S_2's body diode and charges C_2. The voltage across s_2 is zero as soon as the body diode is conducted and the pulse of the gate can be put in to accomplish ZVS. For output, D_2 conducts and delivers capacitor output C_{02}. This intermediate will wrap up at the point where S_2 switch current hits zero.

Interim VI [t_5~t_6]

At the point where S_2's body diode current stretches to zero, it's heading changes, and it passes through the S_2 switch that was switched on in the past interim. The transformer current is raising much the same as in the past. After t_4, capacitor C_1 has been charged as input constant current flows through the transformer. This cycle is ended by the exit of the S_2 pulse gate. In the time between t_4 and t_6, the transformer current rises directly from 0 to i_1.

4. Theoretical Analysis

4.1. Comparison of switching depletion in resonance behavior above and below

The switch's turn-off and conductive dissipation can be determined by subsequent relationships

$P(\text{turn-off})=1/2V(\text{turn-off})I(\text{turn-off})(t_r/T_S)$ …… (4)

$P_{conduction} = R_{on}\, I_{rms}\text{^}2$ …… (5)

Where $V_{turn\text{-}off}$ and $i_{turn\text{-}off}$ are the voltage and the switch's current at turn-off minute, separately and t_r and t_s is the switch's up time and switching time. t_r is limited to the switch's features, but $V_{turn\text{-}off}$ and $I_{turn\text{-}off}$ rely on the converter's features. R_{on} is the switch's conductive obstruction. So you can accumulate switching losses coming out of:

$P_{switching}=P_{turn\text{-}off}+P_{conduction}$ …… (6)

4.2. ZVS Condition

$Is_2(t_4)=i_{lk}(t_4)\text{-}i\ in(t_4)=i_1\text{-}Iin=Iin$ …….. (7)

In S_1's body diode current is consistently I_{in}, so this implies ZVS for switch S_2 accomplished for all heap runs ($i_1=2I_{in}$ will be seen in the next area). At t_0 when S_2 turns off, I_{in} and i_{lk} compromises pass through S_1's body diode.

$C_{oss,\ total}=C_{oss,\ S1}+C_{oss,\ S2}$ …….. (8)

Coss is a parasitic switch capacitor along these lines.

4.3. Input current

The switch s1 is turned on by DTs during this period and V_{in} is the voltage crosswise over L_B. The current wave of feedback is as follows:

$$\Delta i_{in} = \frac{V_{in}}{L_B} DT_s \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (9)$$

4.4. Voltage and current stress of semiconductors

As declare earlier, C_1 voltage is consistent between t_3 and t_4. Turn voltage S_1 rises straight to its height, and then turns off, and S_2 turns off. From that point on, the sinusoidal voltage of S_2 decreased to t_3. When switches work in ZVS mode, turn-on losses may be ignored while turn-off losses remain.

5. Simulation

The new structure is used to strengthen the downsides of the current framework and to address them. The programming of PLECS / Simulink was recreated in the new application circuit outline and shown in fig 3.

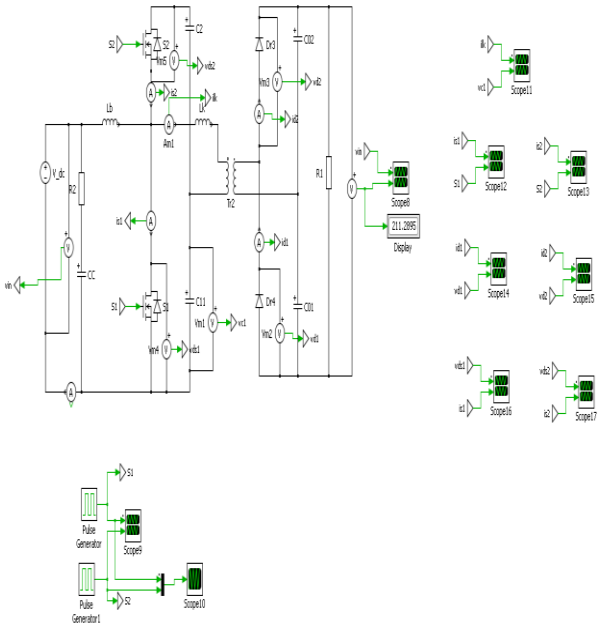

Figure 3: Simulation diagram of quasi Z-source resonant converter

The input voltage is 24V, and by boosting performance, the output voltage is raised to 212V and appears in fig 4.

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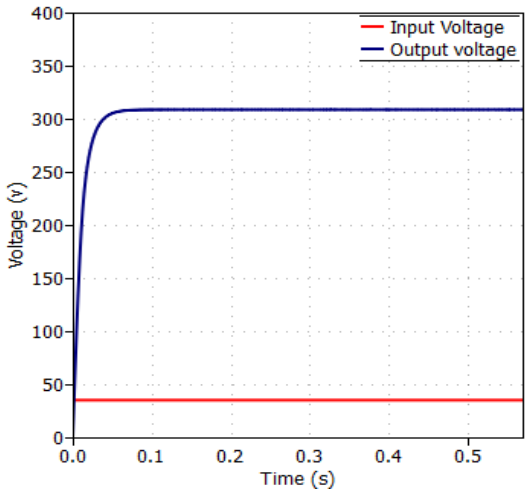

Figure 4: Input and the Output voltage of the boost converter.

The current ranges of the leakage inductor and the voltage levels across the capacitor were shown in fig 5.

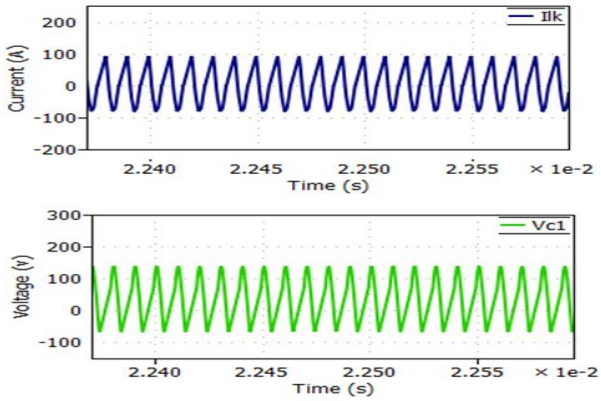

Figure 5: Current and voltage of leakage inductor and capacitor.

I_{lk}'s current is very well seen as zero in some interims, so the converter works in the resonance below as stated earlier. The voltage of the C_1 capacitor is not stable resulting in a slight deviation from the switch voltage. This can be seen in Figure 6.

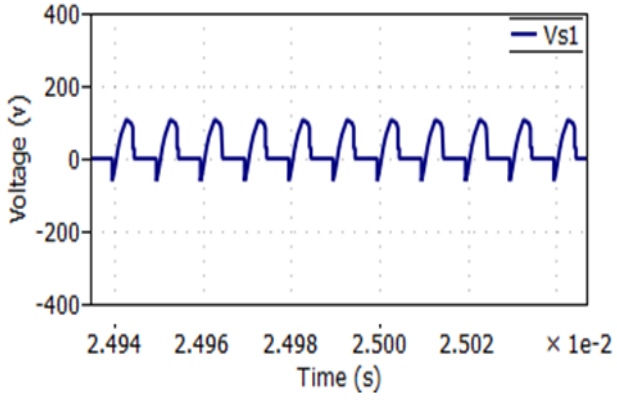

Figure 6: Current and voltage of switches S_1 of QZSR converter

Because of the variety of C_1 voltage, the voltage over the switches does not appear to be consistent. fig. 7 explains the current and voltage level of the D_1 diode [12].

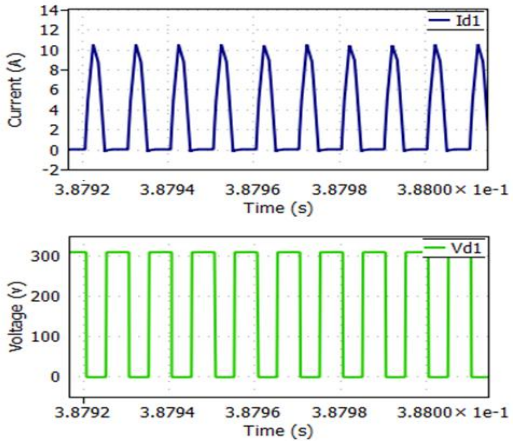

Figure 7: Current and Voltage of output diode D

The voltage gain of the proposed framework is 314V on the duty cycle of 0.45. Thus the diagram of voltage gain is shown below fig 8.

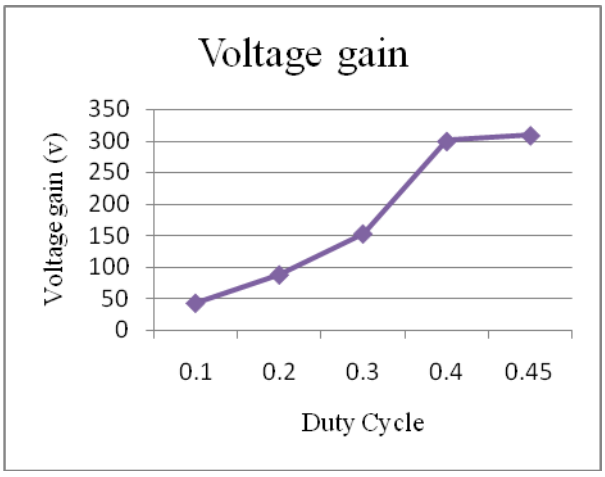

Figure 8: Voltage Gain Vs Duty Cycle.

The Output is enhanced over the current system and power Vs efficiency plots the waveform. The power and efficiency levels are expanded linearly. The waveform is shown in fig 9.

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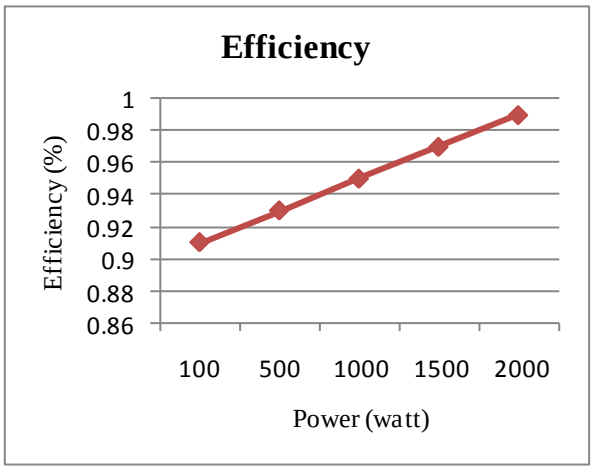

Figure 9: Power Vs Efficiency

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