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Design and Implementation of Reflected Binary Code Carry Select Adder Based Further Desensitized Halfband FIR Filter

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Abstract

In digital signal processing, half band Finite Impulse Response (FIR) filters are widely used in the application of multi-rate systems to strengthen their efficiency. Construction of the filter as a cascade of section causes improved reduction in coefficient sensitivity in digital filter. In existing method, desensitized half band FIR filters are used to enhance the performance of the filter using reduced SQRT CSLA where the filter complexity is reduced by simplifying the adder part in the multiplier but it increases the area and speed. To reduce the area further, the Reflected Binary Code Carry Select Adder (RBC CSLA) in multiplier part is used and to increase the reduction in coefficient sensitivity, further desensitized half band FIR filter structure is presented. The proposed architecture is implemented in Xilinx 12.4 ISE and evaluated using Modelsim 6.3c.The 32-bit RBC CSLA adder offers 28.88% reduction in number of LUTs and 22.22 % reduction in occupied slices than 32-bit SQRT CSLA. The proposed RBC adder based further desensitized FIR filter using modified Booth multiplier with RBCCSLA achieves 9.48% reduction in delay and 3.98% reduction in power consumption. The proposed method offers better performance compare to the existing method in terms of reduced hardware complexity and high speed.

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1. Introduction

Half band FIR filters are commonly used in the application of data converters, communication systems, signal processing, etc. The complexity of digital filter is minimized by constructing as a cascade blocks. The research work mainly aims to achieve reduced co-efficient sensitivity for half-band filters with enhanced performances by reducing the hardware complexity. In the existing method, modified Booth multiplier with SQRT Carry select adder (CSLA) based MAC unit is proposed for the desensitized filter with a reduced coefficient for efficient filter performance. However the previous researches only focus on less co-efficient sensitivity with less hardware complexity which provides good performances but does not satisfy the condition of high speed with parallel processing. The primary objective is to reduce area further with high speed using RBCCSLA based further desensitized half band FIR filter in the Booth multiplier part. Generally the paper is

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organized with the literature study in section 2, existing method in section 3, proposed method in section 4, results and discussions in section 5 and conclusion in section 6.

2. Literature Survey

Li, Y., et al [1] presented a sixteen-order high-speed FIR filter with four methods such as Full custom Distributed Arithmetic (DA) scheme, Conventional multiplications and additions, Add-and-Shift method with advanced computation schedule. The add-and-shift method examines up to 80% decrease in total occupied slices and 63.3 % versus the largest conventional parallel multiplication implementation.

Willson, A.N [2] presented the design and realization of the low pass FIR filter in which the filter's frequency response can be provided with a significant insensitivity to the filter's tap-coefficient values which offers high speeds, less power consumption and smaller IC area.

Bhatnagar, S [3] proposed the modified carry select adder architecture with less area and power. By replacing the binary to excess-1 converter (BEC-1) with D-latch the high speed CSA is achieved. Over BEC SQRT CSA, the BEC-1 D-latch offers good performance in terms of area, delay and power. This method needs only 86% of gates and 77% of delay than of the original CSA designs required.

Fred Harris et al [4] designed the cascaded form of half-band filter for software defined radio transmitter. The cascaded filter consists of many stages for processing the input signal. With respect to the output sampling frequency, the number of cascaded stages is getting optimized. An initial offset frequency is applied to the input samples for frequency shifting process by the cascaded half band up sampling operations.

Sahoo, S.K. et al [5] proposed a new structure for a high-speed Finite Impulse Response (FIR) Filter. CSHM transfers the process of multiplication into a series of shift and add operations. CSHM gives a significantly enhanced performance over the implementation of Carry Save Array Multiplier (CSAM). The Dual Channel Adder and Compressor are used at each and every middle stage to shrink computational delays, propagating sum and carry discretely to the end and then using a very high speed adder like a Carry-Look-Ahead Adder.

Ravish Aradhya H. V et al [6] proposed the Hybrid Carry Look-ahead Adder (HRCLA) which has been designed by rippling the last carry bit of a 4-bit CLA. A four bit HRCLA has been implemented by using Cadence using 45nm technology. The implementation results show that the 12.2% of Area, 4.6% of power improvement and 14.01% of critical path delay overhead over CLA. This high level of performance is achieved by minimum delay full adder. This work would be useful for MAC design of FIR filter, FFT and other digital signal processing applications.

Ramesh Babu M et al [7] proposed an efficient low power ripple carry adder (RCA) for ultra low power applications. The main objective of this work is to reduce power dissipation by eliminating PMOS tree and also by retrieving the energy stored at the output by reversing the current source direction discharging process instead of dissipation in NMOS network with domino logic, pass transistor logic. Further a comparison of the performances of dual rail domino logic and CPL adder circuits with traditional adder circuits has been presented.

Shiann-Rong Kuang [8] proposed the power-efficient configurable booth multiplier (CBM). It supports single 16-bit, 8-bit and twin 8-bit parallel multiplication operations. To reduce the power consumption efficiently, a novel dynamic range detector is developed in this work to detect the effective dynamic ranges of two input operands. Results show that the developed multiplier has more complex than non-CBMs, but significant power and energy savings can be achieved.

3. Existing Method

Desensitized half band filter architecture with modified booth multiplier using SQRT CSLA adder increases the overall system performance. An half band FIR filter whose transfer function using real value is expressed in the equation (1)

$$Y(z) = Z^{-M}(c_0 + \sum_{v=1,2,3,4..}^{M} c_k (z^v + z^{-v}) \qquad (1)$$

Let us consider the proposed half band FIR filter transfer function factor is $(1+Z^{-1})$ and the transfer function is H(z) for the degree 15(16-tap) transfer function for odd number co-efficients, i.e for instance [9], [10]

$$Y(z)=(1+z^{-1})[c_7+(-c_7)z^{-1}+c_7+c_5)z^{-2}+(-c_7-c_5)z^{-3}+(c_7+c_5+c_3)z^{-4}+(-c_7-c_5-c_3)z^{-5}+(c_7+c_5+c_3+c_1)z^{-6}+(c_7+c_5+c_3+c_1)z^{-7}+(-c_7-c_5-c_3)z^{-8}+(c_7+c_5+c_3)z^{-9}+(-c_7-c_5)z^{-10}+(c_7+c_5)z^{-11}+(-c_7)-z^{-12}+c_7z^{-13}] \qquad (2)$$

The above equation can be rewritten as

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$$Y(z)=(1+\ z^{-1})\{[a_0z^{-14}+a_1(z^{-6}-z^{-8})+a_2(z^{-4}-z^{-10})+a_3(z^{-2}-z^{-12})+a_4(1-z^{-14})]+z^{-1}[a_0z^{-14}-a_1(z^{-6}-z^{-8})-a_2(z^{4}-z^{-10})-(a_3(z^{-2}-z^{-12})-a_4(1-z^{-14})]\} \quad (3)$$

Here a0=c_1+c_3+c_5+c_7, a1=c_3+c_5+c_7, a2=c_5+c_7, a3=c_7. Where c_0, $c_1 \ldots c_k$ are the filter co-efficients. Figure 1 shows the direct form structure of existing desensitized half band FIR filter using SQRT CSLA.

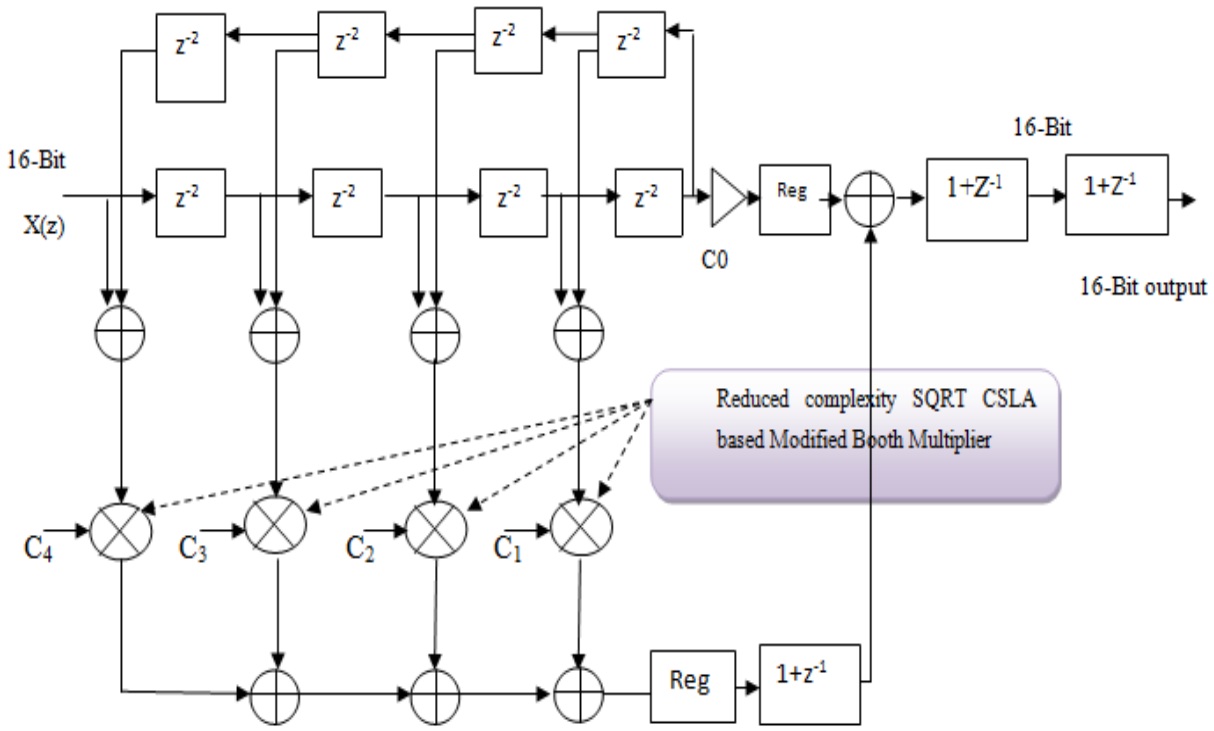

Figure 1: Existing 16-tap desensitized half band FIR filter using SQRT CSLA

4. Proposed Method

To design the RBCCSLA based further desensitized halfband filter, the discernment attained from the desensitized FIR filter can be utilized. The RBCCSLA based desensitized half band FIR filter is formed by doubling the $(1+Z^{-1})$ block and by removing one Z^{-2}delay in desensitized cascaded FIR filter and using of RBC adder in the Booth multiplier. These are the two main factors in the proposed method. Such method has N/2 +1 number of structural adders with $((N+2)/4)+1$ number of coefficients. From this design, the coefficients quantization and adder complexity will be minimized further when compare to the existing method. From the existing desensitized filter, the RBCCSLA based further desensitized halfband FIR transfer function can be expressed as

$$Y(z)=(1+z^{-1})(1+z^{-1})[c_4+(-c_4)z^{-2}+(c_4+c_3)z^{-4}+(-c_2-c_1)z^{-6}+(c_4+c_3+c_2)z^{-4}+(-c_4-c_3-c_2)z^{-10}+(c_4+c_3+c_2+c_1)z^{-12}+(c_4+c_3+c_2+c_1)z^{-14}] \quad (4)$$

This can be written as

$$Y(z)=(1+z^{-1})(1+z^{-1})\{[a_0z^{-14}+a_1(z^{-6}-z^{-8})+a_2(z^{-4}-z^{-10})+a_3(z^{-2}-z^{-12})+a_4(1-z^{-14})]+z^{-1}[a_0z^{-14}-a_1(z^{-6}-z^{-8})-a_2(z^{4}-z^{-10})-(a_3(z^{-2}-z^{-12})-a_4(1-z^{-14})]\} \quad (5)$$

Using this factorization equation (5) the further desensitized half band FIR filter has been designed

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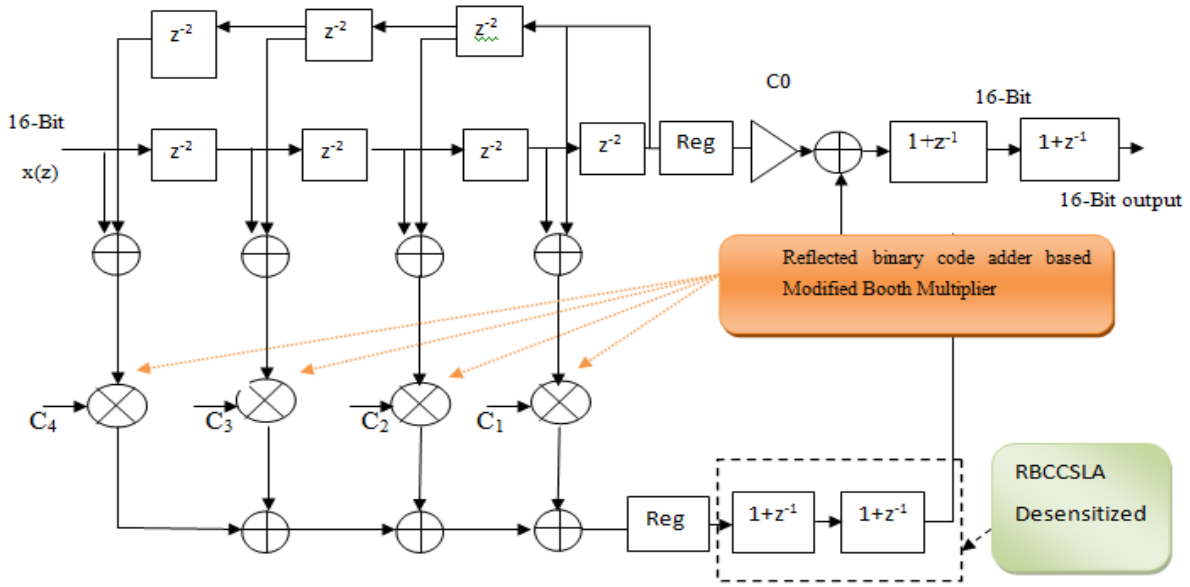

Figure 2: Proposed 16-tap further desensitized halfband FIR filter using RBC CSLA

Booth multiplier is one of the efficient designs for signed bit multiplication [1]. The performance of multiplier depends on the type of adder used for multiplication. So to enhance the performance of Booth multiplier in this work, a reflected binary code adder is used to further reduce area and delay and to increase the speed. When SQRT CSLA in existing multiplier is replaced with the RBCCSLA, it offers reduction of area and delay.

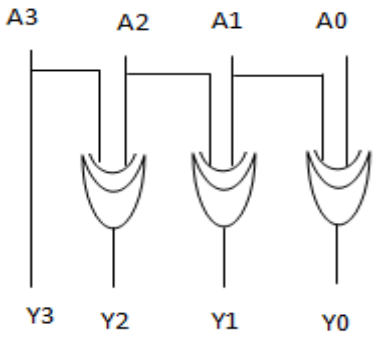

Figure 3: 4-bit Reflected Binary Code

The 4 bit reflected binary code is shown in the figure 3. Here A3,A2,A1,A0 are the binary inputs and Y3,Y2,Y1,Y0 are the binary outputs. The Boolean expression and truth table representation of the 4-bit RBC is expressed as:

Yo=A0 XOR A1

Y1=A1 XOR A2

Y2=A2 XOR A3

Y3=A3

Table 1: Truth Table of RBC

A[3:0]	Y[3:0]
0000	0000
0001	0001
0010	0011
0011	0010
0100	0110
.	.
.	.
1111	1000

The proposed structure of 32 bit RBC CSLA is shown in the figure 4. The structure consists of eight groups or modules of ripple carry adders (RCA). Each group consists of one module of 4-bit RCA and RCA output is given to 4-bit RBC and the outputs are taken through multiplexer.

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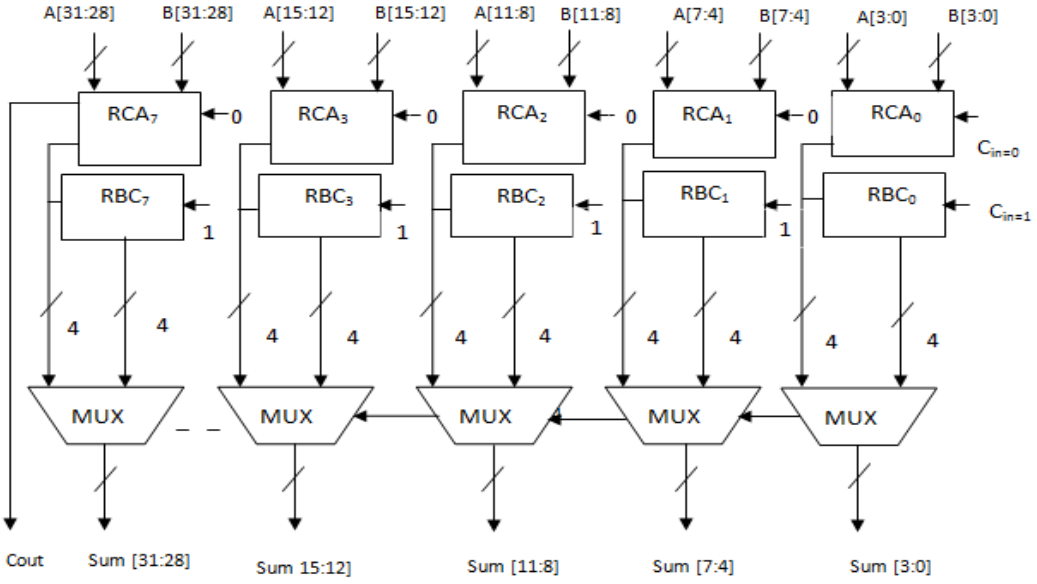

Figure 4: 32-bit structure of RBC CSLA

5. Implementation Results

The proposed design has been developed using Verilog-HDL and synthesized in Xilinx ISE family Spartan3 device XC3S400 package PQ208 and speed -5. In the application of DSP, the reduction of coefficient sensitivity is the main concern for using RBCCSLA based further desensitized halfband FIR filter. The performance analysis of RBCCSLA based further desensitized FIR filter is enhanced further with the help of high performances of RBC MAC unit structure which reduces the area and delay of the system compared to existing adders. Figure 5 shows the simulation result for the proposed RBCCSLA based further desensitized FIR filter.

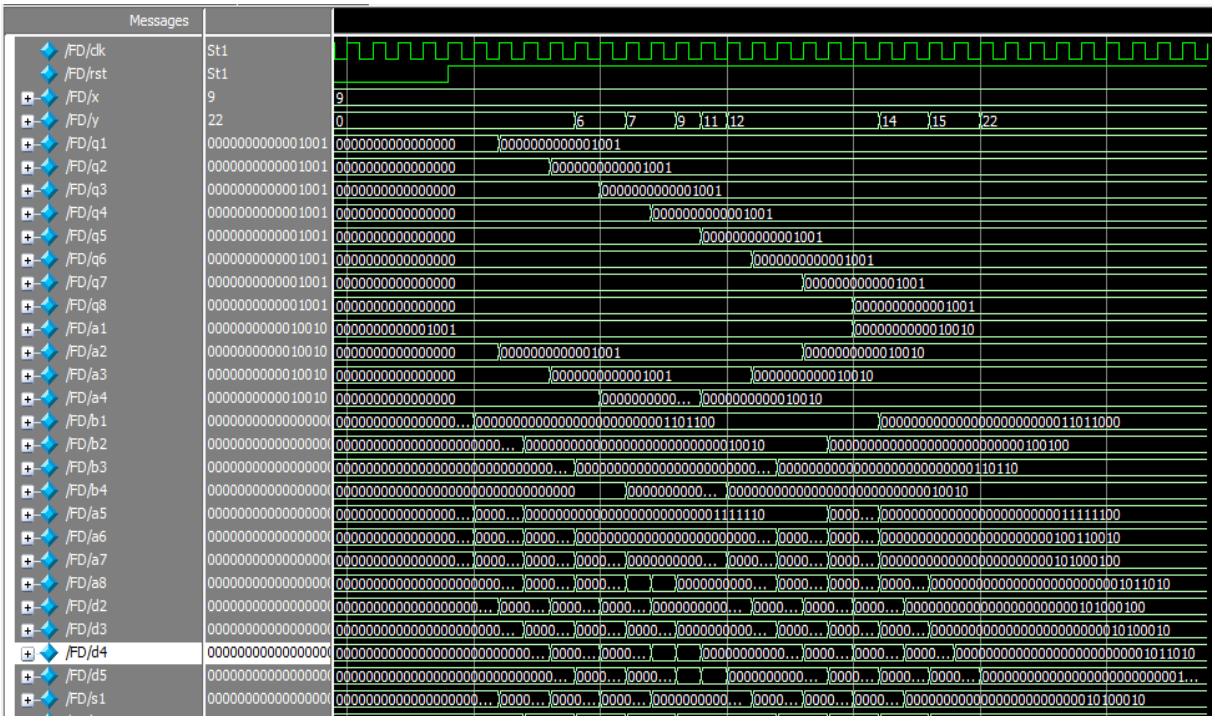

Figure 5: Simulation results for the proposed method using RBC

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Table 2 shows the comparison analysis of the proposed and existing CSLA adder. It confirms that the proposed RBC uses less LUT and slices than the SQRT adder.

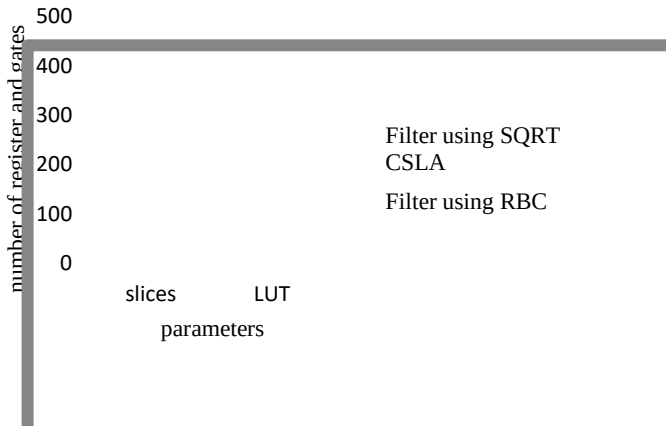
Table 2: Comparison of Existing and Proposed adder

Parameters	**SQRT CSLA adder (16-bit)**	**RBC CSLA adder (16-bit)**
Number of LUTs	45	32
Number of occupied slices	27	21

Table 3 illustrates the comparison of the existing and proposed RBC CSLA based further desensitized half band FIR filter.

Table 3: Comparison of Existing and Proposed RBCCSLA based further desensitized half band FIR filter

Parameters	**16-bit- desensitized FIR filter using SQRT CSLA**	**16 bit- Further Desensitized using SQRT CSLA**	**16bit-Proposed Further Desensitized using RBC CSLA**
Number of slice Flip-flop	352	413	408
Number of LUTs	2787	346	334
Number of occupied slices	1866	346	337
Delay(ns)	90.134	14.640ns	13.252ns
Power (W)	0.966w	0.630w	0.605w



a)

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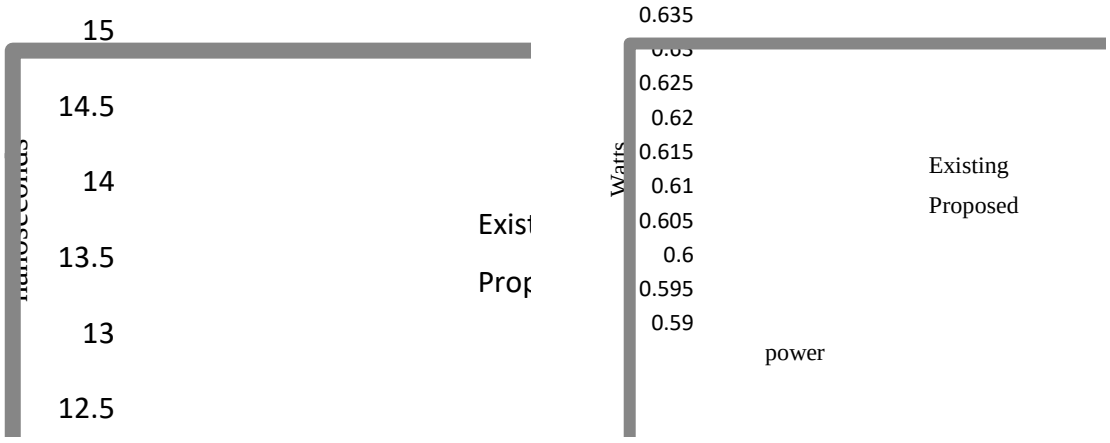

b) c)

Figure 6: Performance analysis of the existing and proposed method

Figure 6 (a, b & c) shows the area, delay and power of the existing 32-bit desensitized halfband FIR filter SQRT CSLA adder and the proposed filter using RBCCSLA adder respectively. From the figure it is obtained that the proposed method is found to be efficient in terms of Area, Delay and Power compared to the existing method.

6. Conclusion

In this paper, the design of further desensitized FIR filter is experimented by using Verilog HDL in the application of multirate digital signal processing. The $(1+z^{-1})$ block is added for reducing the sensitivity of the halfband FIR filters. In this Direct form FIR filter, the modified booth Multiplier is introduced to enhance the performance of MAC unit of further desensitized FIR filter. Also a new adder part is developed in the multiplier to increase the performance. The 32-bit RBC CSLA adder offers 28.88% reduction in number of LUTs and 22.22% reduction in occupied slices than 32-bit SQRT CSLA. The proposed further Desensitized FIR filter using modified booth Multiplier with RBC CSLA offers 9.48% reduction in delay and 3.98% reduction in power consumption than existing RCA based digital FIR filter.

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