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Power Optimized BCD adder Using Low Power Techniques

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Abstract:
Today growing market demands the Microelectronic Circuits with less power consumption because of mobile and portable electronic systems are working with the Batteries. In this scenario, density of the chip increases with the increase of transistors on the chip. Increase of density causes difficult of reducing the power dissipation and hence limit the functioning of the system. In this work proposed BCD adder circuit by Gating-Vdd technique to reduce the power consumption and analyze the proposed adder circuit with Sleep Transistor and Conventional techniques. Today most of the VLSI systems are having CMOS devices, that's the reason concentrated on the development of BCD adder using CMOS devices.

Keywords: *BCD adder, sleep transistor, gated-V_{dd} transistor.*

I. INTRODUCTION

Power, Speed and Area are the Major design constraints of any VLSI system design [1]. Battery life is sole important for portable devices, as it emphasizes the significance of power. According to the customer demand, speed and smaller devices (lesser area) are also equally important. Faster the operations, power consumption will be more. Similarly, sizing down leads to denser device of transistors in the devices and increases the power consumption. The limitations to achieve optimal design need the further Technology Innovation [2]. In every Processor, particularly in ALU , there is a need of Adder Circuits. To perform the BCD addition, demand of BCD adder circuits.

Essentially an advancing technology is required to fulfill the desired requirements in Applications like gaming, video processing etc.

To meet the calculation and diversion requests, the semiconductor IC's preparing modules and graphical handling units.

Our cell phone not to be consumed that much of power during computations. The gadget applications like tablet PCs power scattering is more essential. For this purpose VLSI designers must meet the computational requirements. So decreasing the power utilization is an important parameter and everyone to think or plan the devices in that direction.

II. METHODOLOGY

Power gating is a procedure utilized in incorporated circuit configuration to lessen control utilization, by closing off the current to squares of the circuit that are not being used. The power gating can be actualized from various perspectives. This work mainly deals with the sleep transistors and the Gated-V_{DD} transistors.

PMOS or NMOS act as sleep transistor with high V_T and is used to control the power supply, not to allow the supply to unused components in a structure. The PMOS sleep transistor called header switch to switch V_{DD} supply. The NMOS sleep transistor called as footer switch controls V_{SS} supply. In structures, either a header or footer switch is utilized because of

January-February 2020
ISSN: 0193-4120 Page No. 8789 - 8795

tight voltage edge and too vast region occupancy when both header and footer switches are executed. In spite of the fact that the idea of the sleep transistor is straight forward, ideal sleep transistor plan and usage is a test because of different impacts, presented by the sleep transistor and its executions, on structure execution, territory. Ideal sleep transistor configuration additionally relies upon plan explicit objectives and picked CMOS innovation and procedure.

In sleep mode, low leakage PMOS transistors uses as header to stop control supplies to parts of a structure. Whereas NMOS footer switches can be used as sleep transistors. The sleep transistors embedding into the chip's, the ability to adopt a leakage power related with the power supply. The actual power called virtual power which t drives the cells and can be invalidated.

Normally, in a power gating technique, high-V_T sleep transistors are used in this technique, generally called multi threshold CMOS (MTCMOS).

Power gating execution has additional examinations for timing end use. The going with parameters ought to be considered and their characteristics intentionally picked for a productive execution of this methodology or permanent power connection. Block diagram of Power gating circuit shown in Fig.1

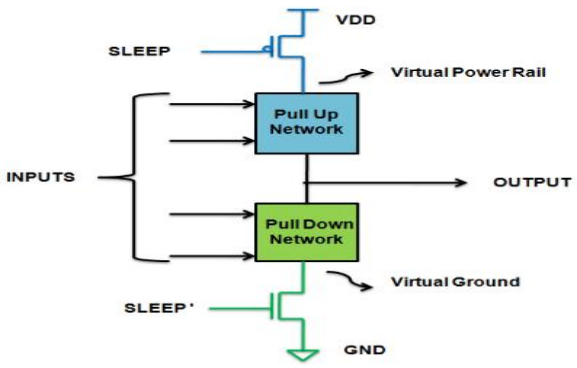

Figure 1: Block Diagram of Power Gating

III. BCD ADDER

Conventional BCD Adder: Conventional BCD adder shown in Fig 2.

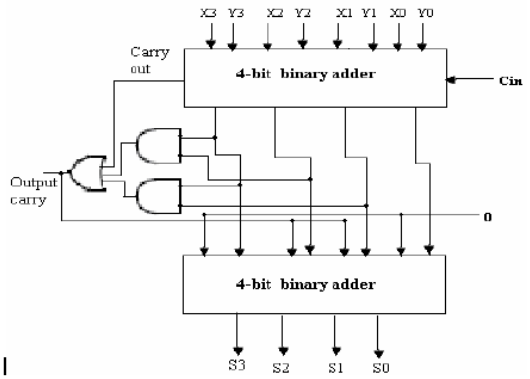

Fig 2:Block Diagram of BCD Adder

In BCD, only 0000-1001 (0 to 9 decimal numbers) binary numbers used. Any BCD two digit number consists of Four binary bits for the first decimal digit and next four binary bits for the second decimal digit.

BCD adder using sleep transistor:PMOS or NMOS with high threshold voltage used as sleep transistorand can be utilized as a switch. To switch the V_{dd} supply, PMOS sleep transistor is used. Logic circuit using sleep transistors shown in Fig 3.

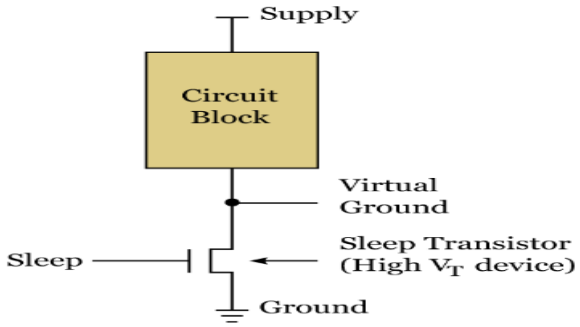

Figure:3 Design of the logic circuits by using sleep transistor

The most outstanding structure is the distributed sleep transistor network (DSTN).In a DSTN, the sleep transistor associated with family of gates by virtual-ground wires. The tapping point is occurred, where sleep transistor is associated with the design of logic gates. By adding more wires to shape a work containing all virtual-ground wires, get the

January-February 2020
ISSN: 0193-4120 Page No. 8789 - 8795

distributed sleep transistor network structure among the leakage decrease systems; the power gating procedure has turned out to be a standout amongst the best strategies. At nano scale, the circuit thickness being expanded then the sleep transistors usage is an essential job in decreasing the leakage intensity of the circuit. BCD adder using sleep Transistor shown in Fig 4.

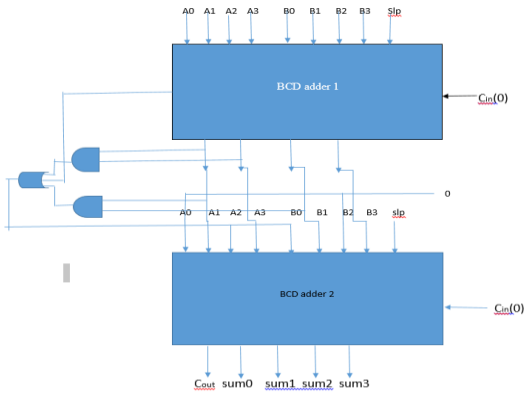

Fig 4: BCD adder using sleep transistor.

The V_{ss}supply is controlled by the NMOS sleep transistor, footer switch. In designs, both header and footer switches are implemented.

IV. Literature Survey

1. C. Chrisjin Gnana Suji etc. all discussed Performance analysis of power gating design in low power VLSI design. Power dissipation, time delay parameters are considered, sleep transistors, BCD adders, DSTN, clock gated power rating, sleep transistor scheduling are mentioned, Merits are Decrease in power dissipation, Demerits are Ground Leakage

2. Changolong Leitte discussed Distributed sleep transistor network for power reduction, cluster based design is used. Area, performance, power, supply voltage, leakage currents parameters are considered. sleep transistors, clustering algorithm, switching circuits are mentioned, merits are area decreases, performance increases, transistor size decreases, compatible with timing driven placement, demerits are large interconnection resistances.

V. Design of Gated –V_{DD} Circuit

In order to overcome the drawback of conventional BCD adder, a novel circuit called BCD adder using gated-V_{DD} transistor is used. Gated-V_{DD} enables an IC to eliminate virtually all the leakage energy dissipation in the chip's of unused sections by "turn off" the supply voltage. The extra transistor is introduced in the supply voltage or the ground path of an IC to turn ON the used sections and turned OFF the unused section. The gated – Vdd circuit shown in Fig 5.

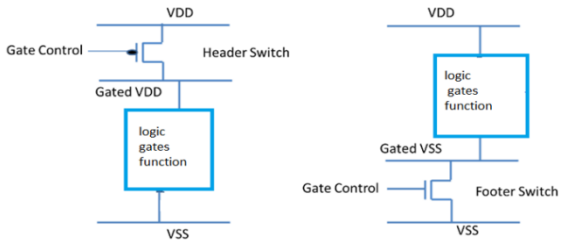

Fig 5: Gated-V_{dd}circuit.

Thus, gated the chip's supply voltage. Gated-V_{dd} technique reduce leakage and leakage energy dissipation and gives the best performance advantages of lower supply and threshold voltages.

VI. Implementation

BCD adder using Gated-V_{DD} transistor: A BCD adder using gated-V_{dd}transistor shown in Fig 6.

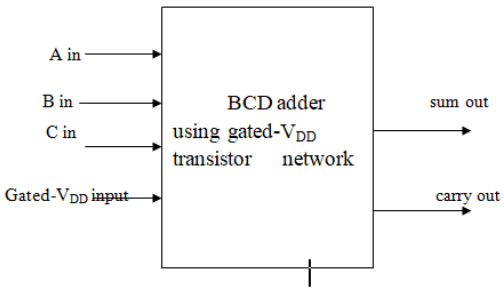

Fig 6: BCD adder using gated-V_{dd} transistor.

In ideal mode , the gated-V_{dd} transistor turn off the circuit. This implies cutting off the power rails, this can reduce leakage power effectively. The leakage

January-February 2020
ISSN: 0193-4120 Page No. 8789 - 8795

components, both sub threshold and gate leakage has become more and more, when the transistor geometry gets smaller,. The leakage power occupies significant portion of overall circuit power. The best technique Gated-V_{DD} transistor adopted between the conventional BCD adder block and the power supply rails either or both V_{DD} and V_{SS} may leads to reduce the transistor leakage.

The flow chart for the design of the BCD adder circuit by using the gated-V_{DD} transistor technique can be implemented by using the flow chart shown below in figure.

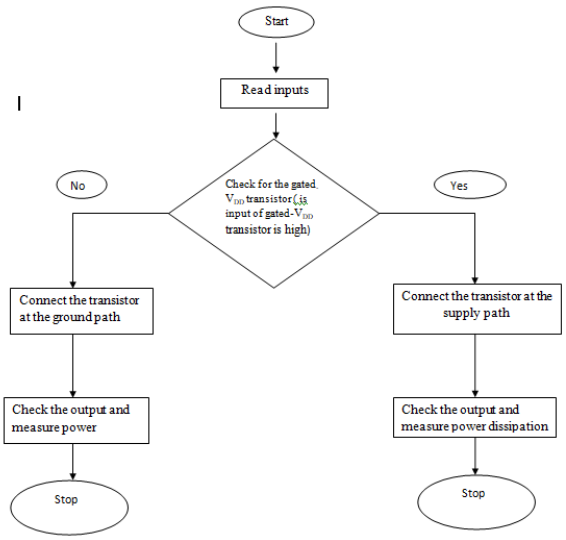

Fig 7: Flow Chart For Implementation of BCD Adder Using gated-V_{dd}.

The flow chart shown in fig 7indicates the function of the gated-V_{DD} transistor (new transistor). First the state of the transistor input must be checked before connecting the gated-V_{DD} transistor to the circuit. If the input is high then the NMOS transistor is used as new transistor and is connected at the ground path. If the input of the transistor is low then the PMOS transistor is used as the gated-V_{DD} transistor and is connected at the power supply path. The output at the supply path transistor produces its output waveforms by without causing any distortion in the wave forms. The power dissipation will also reduce. The transistor connected at ground path produces the output waveforms by causing some amount of the distortion in the waveforms. The leakage power reduction of the transistor connected at the ground is more than that of the transistor connected to the supply path. Hence NMOS transistor is most widely preferred in the design

VII. Results

Simulation results:

Conventional BCD adder: A BCD adder is one type of the adder used in the digital logic. It's addition is different from normal full adder. The logical diagram of the BCD adder is shown in figure 7.3.

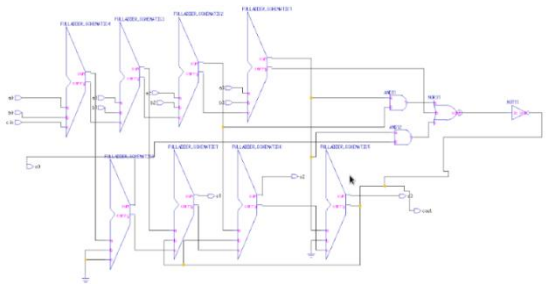

Figure 8: Logic Diagram of Conventional BCD adder

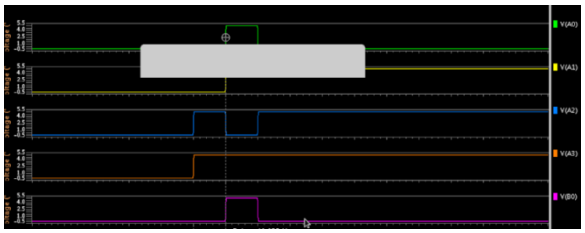

Figure 9(a): Conventional BCD Adder Waveforms.

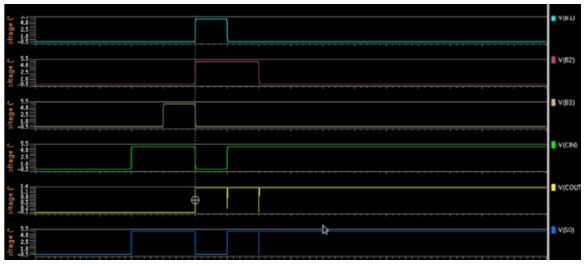

Figure9(b): Conventional BCD Adder Waveforms.

The digital systems uses two sets of four different inputs having same number of bits. One of the four inputs of the BCD adder is called as the addend and the other is called as the augends.

January-February 2020
ISSN: 0193-4120 Page No. 8789 - 8795

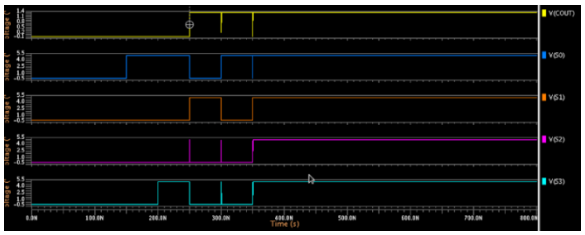

Figure9(c): Conventional BCD Adder Waveforms.

2. BCD Adder using Sleep transistor:

A BCD adder is one type of the adder used in the digital logic. It's addition is different from normal full adder. The logical diagram of the BCD adder using sleep transistor is shown in figure. 10.

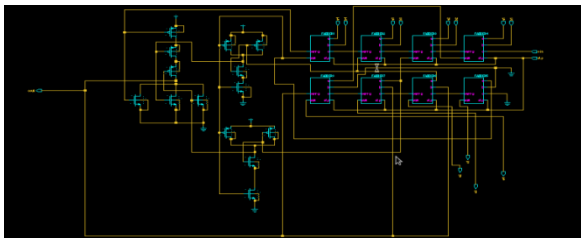

Figure 10: Logical Diagram of BCD Adder using Sleep Transistor.

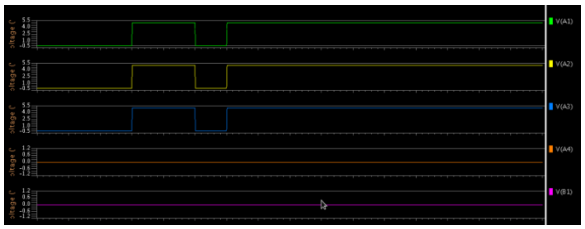

Figure11(a): Waveforms of BCD adder Using Sleep Transistor.

The above inputs are called as the addend of the BCD adder by using sleep transistor. The waveforms of the BCD adder using sleep transistor produces less delay when compared to that of the conventional BCD adder.

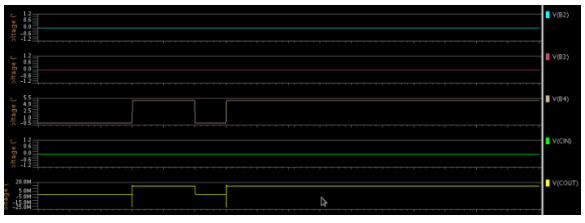

Figure11(b): Waveforms of BCD adder Using Sleep Transistor.

In this section we have describes the simulation results. First, take the output for the schematic design. Using the net list, convert the schematic into layout and make the layout design.

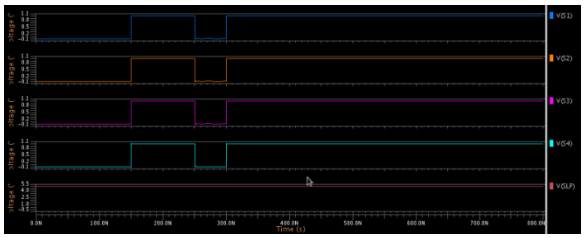

Figure11(c): Waveforms of BCD adder Using Sleep Transistor

In this section we have describes the simulation results. First, we take the output for the schematic design. By running the layout, obtain characteristics of the circuit and the V-I characteristics also.

BCD Adder Using Gated-v_{dd} transistor:

A BCD adder is one type of the adder used in the digital logic. It's addition is different from normal full adder. It can also be implemented by using Gated-V_{DD} transistor. The logical diagram of the BCD adder using Gated-V_{DD} is shown in figure. 12.

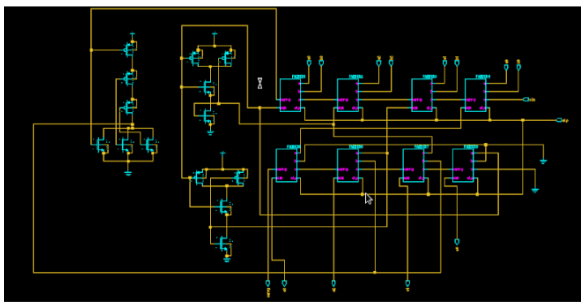

Figure 12: Logical Diagram of BCD Adder Using Gated-V_{DD} transistor

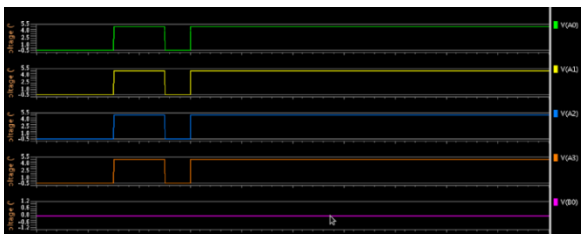

Figure13(a): Waveforms of BCD adder Using Gated-V_{DD} Transistor

January-February 2020
ISSN: 0193-4120 Page No. 8789 - 8795

The above inputs are called as the addend of the BCD adder by using gated-V_{DD} transistor. The addend part of the BCD adder consists of four input lines with multiple numbers of bits. The waveforms of the BCD adder by using gated-V_{DD} transistor have less delay when compared to that of the conventional BCD adder.

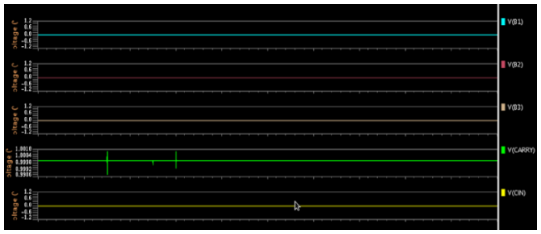

Figure13(b): Waveforms of BCD adder Using Gated-V_{DD} Transistor.

In this section, the simulation results are described. The inputs are called as the addend of the BCD adder by using gated-V_{DD} transistor. The addend part of the BCD adder consists of four different inputs with same number of bits.

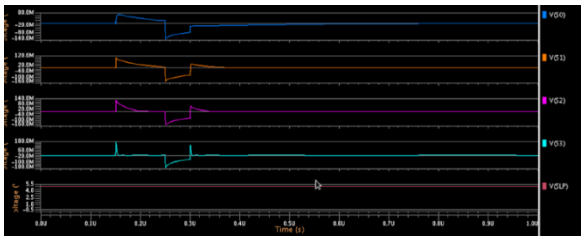

Figure13(c): Waveforms of BCD Using Gated-V_{DD} Transistor

Table 1: Power Comparison of BCD adder (Conventional) , BCD adder using Sleep Transistor, Gated-Vdd

Techniques used:	BCD adder by using Gated - V_{DD} transistor	BCD adder by using Sleep transistor	Conventional BCD adder
Voltage(v)	Power delivered(nW)		
1	6.965	28.791	58.8992
1.1	8.187	33.591	69.2985
1.2	9.5402	38.848	80.815
1.3	11.036	44.60	93.558
1.4	12.689	50.894	107.647
1.5	14.517	57.779	123.220
1.6	16.538	65.312	140.427
1.7	18.772	73.555	159.435
1.8	21.243	82.578	180.433
1.9	23.977	92.459	203.627
2.0	27.001	103.28	229.248
2.1	30.348	115.14	257.550
2.2	34.054	128.15	288.814
2.3	38.156	142.42	323.350
2.4	42.699	158.08	361.501
2.5	47.730	172.28	403.646
2.6	53.301	194.16	450.201
2.7	59.470	214.96	501.623
2.8	66.300	237.69	558.419
2.9	73.862	262.75	621.143
3.0	82.233	290.29	690.406
3.1	91.496	320.56	766.879
3.2	6.965	353.86	851.299
3.3	113.07	390.46	944.471
3.4	125.61	430.72	1047.3
3.5	139.46	474.98	1160.7
3.6	154.76	523.64	1285.8
3.7	171.66	577.14	1423.8
3.8	190.32	635.95	1575.9
3.9	210.99	700.56	1743.6
4.0	233.61	771.61	1928.3
4.1	258.64	849.63	2131.7
4.2	286.23	935.34	2355.8
4.3	316.61	1029.5	2602.4
4.4	350.06	1132.0	2873.8
4.5	386.87	1246.2	3172.4
4.6	427.35	1370.6	3500.8
4.7	471.87	1507.1	3861.8
4.8	521.04	1656.8	4258.5
4.9	581.43	1820.8	4694.3
5.0	683.83	2000.6	5173.0

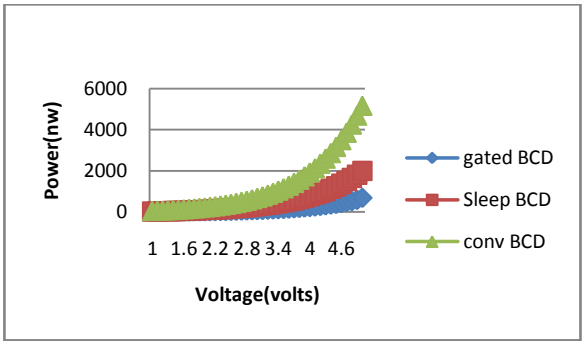

Fig 9: comparison plot of conventional BCD adder, sleep BCD adder and Gated-v_{dd} BCD adder.

The total power dissipation of the circuit conventional BCD adder, BCD adder using Sleep transistor and BCD adder by using gated-V_{DD}

January-February 2020
ISSN: 0193-4120 Page No. 8789 - 8795

transistor is tabulate in the table. 7.1. From the table it is proved that the value of the power consumption increases with increase in the voltage. The power dissipated by the BCD adder using sleep transistor is less when compared to that of the conventional BCD adder. The power dissipated by the BCD adder by using gated-V_{DD} transistor is less when compared to that of the both the techniques i.e., conventional BCD adder and the BCD adder using sleep transistor.

VIII. Conclusion

Thus the proposed work demonstrates the advantages of gated-V_{DD} transistor over sleep transistor in terms of average power consumption. The gated-V_{DD} transistor undergoes less power dissipation when compared to that of the sleep transistor.

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