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Design and Analysis of BIST Approach for 3D-Mesh Nocs Router Testing

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Abstract:
A new built-in self-test architecture for complex and heterogeneous systems on a chip is presented with flexible, hierarchical, and distributed power-restrained, embedded memory. The proposed structure consists of a BIST architecture in a 3-D NOC, low area, low power memory BIST control system, and a serial interconnection to them for low routing overheads. The architecture is technology-independent due to its simplicity; the proposed approach offers heterogeneous memories as well as the error spotting to minimize time complexity and achieve high test competitiveness in power and time constraints.

Keywords: *BIST architecture, 3-D NOC, power, and time constraints.*

I. INTRODUCTION:

There has been a significant improvement in application capacities of unrestricted consumer requirements for innovations, and Gates continues to decline. Several cores can, therefore, be combined in a single die and allow the SOC(system-on-chip) to enhance performance. The researchers and designers are increasingly investigating noc as a high-performance and scalable communication system to address interconnection complexity issues in multiprocessor systems on chips.A chip network includes routers, connections, NIs, and cores that can be configured to standardized routers or point to point channels interlinking IP cores. The system can then connected to a chip network. Any of these elements may be faulty. NoC frames are comparatively less controllable or detectable as they can be somewhat interconnected and scatter through the chip. Concerning this issue, Built-in Self-Test (called BIST) was developed to overcome it. BIST-based approaches have elevated chip overhead, which results in degradation of performance and increased diffusion of power. Several other works have been proposed regarding the NoC Test Architecture to collaborate with the architecture of communication and reduce overhead. The Test Access Switch (TAS) is used to relate one switch, and TAS broadcasts all the test sets. Two TASs were used where one is on the lower right of the system, and the other on the upper right of the system.The benefit was shown in testing time, but there is no need to adjust the position of TASs, and a different routing algorithm is expected. Here in this paper, we propose an alternative NoC software research design approach. We use NoC processors to manage the entire research procedure for this system design

The BIST architecture was used for the embedded systems with a single processor until multipurpose technology was developed to handle the whole testing activity. For this process, the central processing unit was used. Through

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designing complicated embedded systems of several processors, some research has tried to minimize each processor's test time utilizing various core parallel strategies using the same BIST. In order to conduct an effective routers study, our advanced BIST system design can have desirable characteristics when compared to the other existing BIST systems. The idea behind our strategy was that the core serves as a message generation center in an NoC to produce the test packets used for router testing.

The paper can be structured in the form of The existing BIST technologies as depicted in section 2; The suggested technique was explored in Section 3, Then research results were recorded in Section 4. Finally, our work is summarized in the section 5.

II. LITERATURE SURVEY:

Kumar [1] proposed an arbitrary layout, implemented on a BIST Field Programmable Gate Array would develop a new methodology for fault detection position and diagnosis on the interconnecting and logical frame. This strategy will define any single bridge, accessible or bonded fault in the cross-connection, and every operational fault, which contributes to a shift in the truth table of a component in the logical frames. Existing CLBs in FPGA configure the test pattern generator and output answer analyzer, so no other region overhead is required for the BIST design recommended.Bhaskar et al.[2] Propose the EBISR scheme hardware design. To test computer overhead (HO), repair speed, durability, and quality penalty, a simulator is introduced. Zhang et al. [3] On the basis of their previous work, the BMSIC-TPG is focused on several single-input (MSIC)-TPG modifications. The transmitted circuit expends MSIC vectors, thereby increasing the overhead equipment of the check circuit generation. Pandir [4] in which the Faults dictionary could be updated or corrected at a time according to the MBIST needs and the control signal provided in the redundancy analysis (RA) algorithm. The pivots of the row and column and the application for maintenance are further inspected by a previous list provided through comparable acts. Cai et al. [5] A novel self-test built-in algorithm (BIST), used for testing low-voltage SRAM, is suggested in this paper. Martinez et al. [6] Present an LFSR study using a known PG (ATPG) test set. Through their respective trade-off analysis, two methods are used to classify flaws that are difficult to detect. The Berlekamp-Massey (BM) algorithm is used to optimize the overhead field reduction. Gorman et al. [7] proposed the BIST methodologies. Kumar et al. [8] propose a new test technique to reduce energy consumption in the test mode by reducing the switching operation on built-in auto-test circuits. Patnaik et al. [9] discuss the BISR (CBISR) configurable strategy for the remedying of variable size and reliability control memories.Silveira et al. [10] Present an efficient, self-test built-in memory (MBIST), which can easily be adapted to specific user requirements and memory configurations. His RTL code is created using software scripts that allow easy reading without using the compiler instructions. The simple Architecture can be modified for multiple test methods, such as concurrent checking all data or serial testing of information at the same time. Sun et al.[11] proposed BIST implementation. Martirosyan et al. proposed the Efficient Memory and non-volatile Fault Detection & Diagnostics Methodology. Martirosyan, S., & Harutyunyan, G.[12] (2019, September). An Efficient Fault Detection and Diagnosis Methodology for Volatile and Non-Volatile Memories. Ince et al. [13] Proposed about the Digital Built-in Self-Test for Phased Locked Loops to Enable Fault Detection. Bernardi et al. [14] proposed a Facilitating fault-simulation comprehension through a fault-lists analysis tool. Seung-Ho et al. [15] Proposed about the fault detection mechanisms in BIST.

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III. PROBLEM STATEMENT:

The 3D routing technology suffered a lot due tofault routing and memory issues. There are several other existing technologies that are there, but they are all not useful. Hence there is a need for an effective method to overcome the issues in the 3D routing technology. We would propose a new topology and 3-D network-in-chip BIST topology that will reduce expenses, time, power, and memory complexity.

IV. PROPOSED METHODOLOGY:

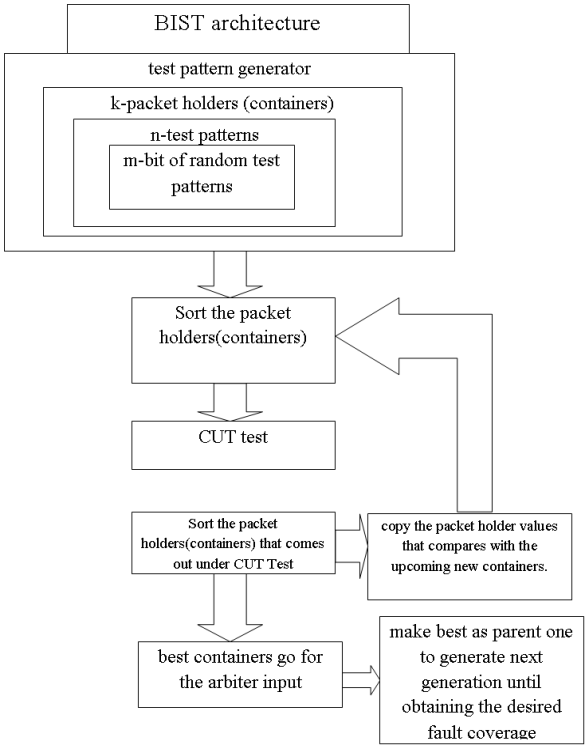

Figure 1 Schematic representation of the proposedarchitecture

Analysis of NoC routers is the primary goal of the proposed control of the architectural design. The test software is responsible for maintaining the test system during analysisas depicted in Figure 1.Here We concentrate on 3D NoC topology in the proposed method. Because of its regularity, it's straightforwardness to use, and having several source-destination routes, 3-D mesh topology is one of the most feasible and commonly used network topologies**.** In order to convert the condition of NoC to test mode and also to control the overall research process, test software uses additional custom test instructions**.**Mainly two steps were followed for converting the condition of the NOC.

1.packet sending and

2. Test collection

While in the first step, in addition to a specific customized test command will switch the NoC state directly towards test mode and render the test packets. Then in the second step, it is necessary to return the test answers for fault analysis after sending all test packets. Therefore, other customized test instructions have also been taken into account for this task. In order to make it more testable, The BISTis created in the NoC architecture. The Hardware mainly consisting of:

•Research packet generator

• signature generator

• sample response loader

• MUXs

Here in which the packets generator generates the router's test pattern controlled by new additional custom test instruction, the signature generator is responsible for compacting and generating registry chain data signatures, "MUX" is used to change the circuit from average to test mode. Test packets were generated depends on the internal router structure. In the suggested test pattern development methodology the optimized test patterns are first created for the arbiter and then mapped to test packets for the entire router circuit instead of produced test patterns for whole router circuit resulting in inadequate fault coverage or generated test patterns for different individual components contributing to a massive hardware overhead. The router testing process can be undergone by using the following steps,

1. Generation of the test patterns

For generating the test patterns, the number of containers can be sorted out after that it can get copied after that new containers can be produced. Repeat the following steps. Repeat the

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steps before the variance of fault coverage is below the limit value. The arbiter will have some constraints over its feedback based on just the NoC design and its routing-algorithm. It should be noted.Thereby after the generation of test patterns, it must be considered.

2. Packet generation:

In the previous parts, the test patterns produced should be transmitted to both the wireless router input ports. Some of the test packets that contain test data are presented for this purpose.The related router components were therefore checked via the message transfer process of these packets.After generating the packet, it should be implemented on the proposed architecture to prove the effectiveness of the method.

3-D NOCBIST architecture:

3D NoC is a simple topology of 2x2x4 mesh, which includes x-addr, y-addr, and z-addr. Thanks to its many properties, including regularity, simultaneous data transmission, and regulated electrical parameters, the mesh topology is chosen for our project. A maximum of seven input ports may be used for every switch, in which the five input ports (local, north, south, east, and west) and the other two ports (up and down) are committed to the interaction between the two layers. The number of ports depends on the switch position in the design since unused links with other switches are eliminated to reduce energy consumption.

Routing:

3d NoC routing is dependent on the fixed X - Y-Z routing algorithm that fulfills the X, Y, and Z coordinates. X - Y-Z routing is addressed as the vertically structured routing algorithm which has the highest performance because it is simple to implement, is free of blockage and life lock. As regards the above constraint, the total wide range of possible inputs from the arbitrators in the 3Dmesh topology could be 1350, and the other entries could be invalid in a normal NoC function mode and never occur in a normal NoC function. The fault with the remaining input variety can, therefore, be eliminated from the fault list. Instead, we add that container to the test patterns and choose the best container to develop the next batch. We follow these instructions until the required fault coverage is reached. Then after that, the test pattern could be generated. We also incorporated two custom recommendations. One is used to apply test packages and the other two to collect test answers. These newly designed guidelines were in three formats (R-type, N-type, and P-type) are available. The first 6-bit will be used as an opcode. Then the first 6-bit custom instructions are also considered to be opcodes and the remaining bits as follows. Ultimately, five input messages enter router inputs simultaneously. Therefore, by a single test instruction, we will deliver these five signals. As a result, test application instruction should be able to decide:

(a) Which port to save the logical virtual channels?

(b) Which digital network for the processing of the message is used?

(c) The message demanded what output port?

In view of these issues, our test package generation requirements require only 28 bits and are not subject to NoC size. After applying the instructions, the fault can be determined.Depends upon the response obtained, the signature was generated. Then the signature can be gone back to the signature generated a file and find out whether the size should be greater or not. If it is greater, it should be eliminated and start the recovery process. This overall fault detection process was done by the BIST architecture.

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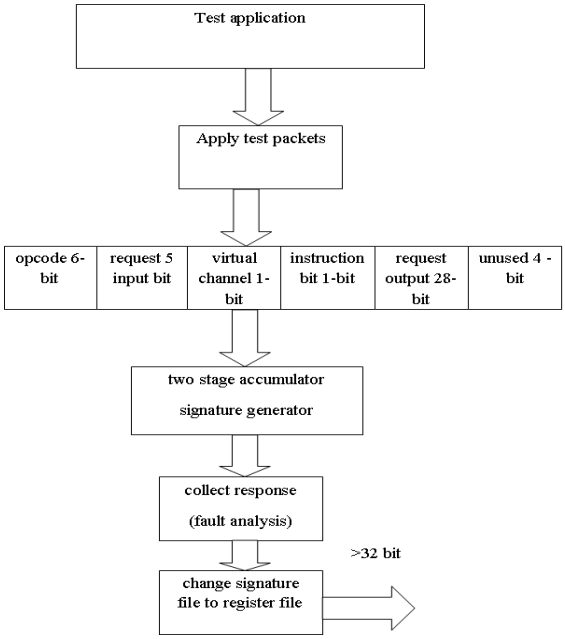

Figure 2 Application layer

V. RESULTS AND DISCUSSION:

The proposed methodlength of the test time and fault performance was analyzed. We used a simple serial fault simulation process for the evaluation of the proposed test architecture within a single SA fault coverage, which first injects one single SA fault into one of the sub-components, then runs the entire testing program to determine whether or not the error injected can be detected through the trial program. This procedure is carried out for all defects in order for each router component to be covered by fault.

Logic	**MUX**	**Signature generator**	**Packet generator**	**Response loader**	**Total**
AND	10	252	55	52	369
NAND	0	0	0	0	0
OR	5	195	28	0	228
NOR	0	0	2	0	2
XOR	0	215	5	0	220
XNOR	0	0	0	0	0
NOT	5	42	55	0	102
BUF	20	154	103	105	382
DFF	0	42	0	0	42
SUM	40	900	248	157	1345

Table:1 Gate count of the Hardware and the router circuit.

Table 1 represents the gate count of the testing hardware and the router circuit. The architectural test style implemented, which is, however, quite independent of NoC size. Our studies are, however, conducted in 2*2*4 3D mesh topologies, and the overall proposed work performance values are shown in Table 2.

LUT	14
FF pairs	04
Delay	156.01ns
Power	0.0851mw
Frequency	756.861 MH^2

Table:2 overall performance of the proposed methodology.

In order to prove the exceed performance of the proposed method, the result can be compared with the other existing mechanisms.

Methods	**Coverage of the faults**	**Clock cycle**	**Test size**	**Test pattern**
3-D NOC with BIST architecture	94.43	300	333	200
ATPG [16]	80.14	3452	-	2518

Table:3 performance comparison

Table 3 represents the comparison of the proposed method with the existing technology. This will reveal that the proposed method performance was highly efficient in fault detection over communication.

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VI. CONCLUSION:

In NoC architecture, we proposed a test methodology for router testing. The advantages of the BIST methodologies are used in our integrated research model in which personalized study guidelines are provided for experiment models and test answers. Our experiments take place on a real NoC hardware area.Findings demonstrate that somehow, the implemented router testing BIST architecture with overhead Hardware performs well when compared to the existing ATPG method.

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