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Closed Loop Design based Resonant Continuous input Current with ZVS Dc-Dc Boost Converter

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Abstract:
The idea was to integrate a resonant tanks into converters to create oscillatory (usually sinusoidal) voltage, current waveforms so that the requirements of ZCS (zero current switching) or ZVS (zero voltage switching) for power control switches could be achieved.The resonance state is commonly used by the soft-switched power converters. Resonance condition usually occurs only during turn-off &on phases, so that ZCS and ZVS can be generated across each switch. Under ZVS scenario, the controlled three and five multiple-output dc-dc converter is proposed. In CCM(continuous conduction mode), the resonant inductor mounted in the converter front side can work and smooth the input current of the converter. Often clarified are the different stages of operation, soft switching state and control schemes.

Keywords: *DC-DC converter; ZVS, ZCS, Losses of Switching, PI Controller*

1. INTRODUCTION

A DC to DC converter is an electronic circuit that converts DC source from voltage level to voltage level. The DC-DC converters are commonly used in various electronic devices such as mobile phones, MP3 players and laptops for battery power supply.There is flexibility for developing DC-DC converters from a single dc power supply to produce multiple dc output voltage. Such multiple output voltages are supplied to the various dc load applications. This scheme will reduce the overall system area by producing several DC voltage levels from single supply source. There are more ripples in the The dc voltage given by the rectifier or the battery is not a constant value and is not appropriate for many electronic devices. The dc-dc voltage regulators are used to regulate the ripples even when the input voltage or the load current changes. The dc-dc converter switching power supply mode is widely used as it uses a transistor type switch and less failure components such as transformers, inductors and capacitors to control the output voltage. There are two different parts in the switched mode power supply: the control component and the power part. The majority of the work is performed by the control part to enhance the quality of output voltage. In Switched mode power supply, the MOSFET is typically used as a control switch to regulate the appropriate output voltage. The MOSFET switches are not to be done constantly and they only operate at fixed frequency intervals, which is why These switches are useful for a long time to come and also provide less power loss to the converter circuit. The fundamental structure of the supply of powershif ted mode is used to increase or decrease DC voltage input. Essentially, the SMPS circuit consists of an output-side filter to eliminate the ripples due to switching[1]. The project's main objective is to control three different output voltages with zero-voltage switching(ZVS) dc-dc converter. The converter consists of three voltages with different outputs. The first and second outputs are operated with the aid of two asymmetric half-bridge converters. The third output is regulated on the basis of the phase shift between two asymmetric half-bridge converters. For all the key switches, ZVS is

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realized. Such multiple output dc-dc converters can provide higher efficiency at high switching speed. Also proposed are the different stages of operation, soft switching condition and control schemes.

The three multiple output converter's closed loop and open loop control strategies were explained. Closed-loop transfer feature of the device. Any electrical or electronic control system's transfer function is the mathematical relationship between system input and output, and thus defines the system's behavior.

To meet The dramatic increase in electronic products in high-power applications for lower power losses like telecommunications, power supply switched mode, etc. The converter is now designed for maximum frequency service, but there is an Expanded switches loss[2]. The soft switching mode eliminates the issue of switching resonant converter failure. There are many styles and techniques suggested for transforming topologies. Similar to PWM converters, the resonant converter (RC) is used in high power applications. Resonant converters usually have one downside, i.e. their non-linear nature, resulting in dynamic response to variable load conditions and operating frequencies.The most suitable topology for this work is the Resonant Converter type LLC. This topology brings to various industrial applications ofall series and parallel Resonant Converter advantages[1]. This series and parallel resonant converter has one major disadvantage, i.e. the absence of SRC load control and the flow of PRC load independent current.. The LLC resonant converter switching input and output side is based respectively on ZVS and ZCS switching[3]. Resonant convertes are able to operate under high frequency spectrum and produce better performance [4, 5] with high power density with low switching loss compared to PWM or hard switching converters.

2. ZVS BOOST CONVERTER

In this, presents a new Zero Voltage Switching boost converter shown in Fig. 1. There are two switches in use, and both are grounded. Consequently, the gating issues are sufficiently avoided. ZVS switch turn-on is achieved which effectively reduces the loss of switching and the generation of EMI. It is possible to use the classic frequency-controlled approach to control the output voltage. ZCS turn-off is given for the diode, which significantly reduces losses in reverse recovery and voltage ringing. As a result, the diode's voltage stresses are well reduced, effectively helping to choose a diode with lower voltage rating and better performanceThis boost converter operates on the basi s of the DC DC boost converter concept under the Z VS condition of the MOSFET power semiconductor s witch [14, 15]. The ZVS technique is better than the ZCS technique. Since capacitive turn–zero voltage switching (ZVS) technique is removed on failure. Using this CN network, a Highly efficient topology for DC-DC converters overcomes obstacles such as asymmetric switch current levels, hurts performance and reduces power. At the transformer's opposite hand, the unregulated diode rectifier is used to minimize switching losses and increase device efficiency[19]. Through preserving the optimal output current[20], the total harmonic distortion (THD) is also reduced. The traditional DC-DC converter structure is shown in Fig. 1

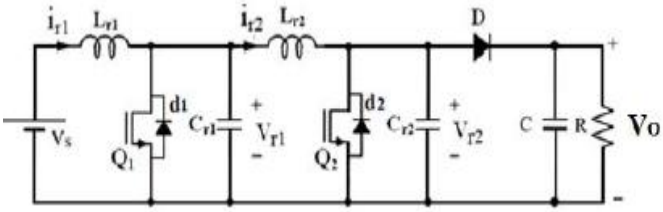

Fig 1 ZVS Boost Converter

For simplify the analysis, it is assumed that all the circuit elements are suitable and that the output capacitor C is high enough so that the output voltage is constant over one switching cycle. The converter is believed to be in steady state. Initial conditions: The process of switching starts at t0. Q1 is believed to be OFF at this moment, while d2, Q2's antiparallel diode, is ON. The initial conditions are ir1(t0)=I1,0, ir2(t0)=I2,0, and vr1(t0)=vr2(t0)=0, respectively. These values are again obtained at the end of the last operating mode. The subscription 1,0 in I1,0 indicates the corresponding value at t0 for ir1. Similar method of denoting certain variables is used. Depending on the output power, I11 can be positive or negative.

3. PROPOSED CONVERTER OPERATION

Closed loop control of the ZVS boost converter We also take 400V as an input voltage in this closed loop mode. The block diagram of ZVS DC-DC converter's proposed closed loop control is shown in Figure 21. As shown in Figure 4, the closed loop Simulink design proposed three output voltage converters. The closed loop's comprehensive control block indicated three output converters as shown in Figure 4. Three outputs are taken as a feedback control in this model. Use the error amplifier to

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equate the reference voltage and the feedback voltage.

The error signal is supplied to the PWM compara tor to compare the ramp signal with frequency and err or signals of 1000 Hz and to give the S4 shift momen tum..

Mode I (t0 – t1): In this point, D2 is performing. Instead, in parallel with Lr2, Cr1 and Lr1 form a resonant network. The magnetic energy stored in Lr1 starts to move to Cr1 and Lr2 in the previous process. Consequently, Vr1 and ir2 are growing. At any point in this interval, the Q2 gate signal should be set high to switch Q2 on at ZVS. This mode continues until the ir2 resonant current crosses at t1 at zero.

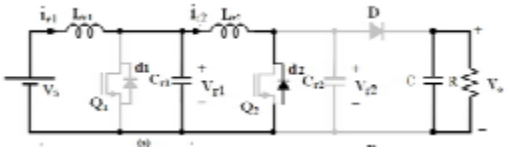

Fig 2(a) mode 1

Mode II (t1 – t2): The current ir2 is slightly optimistic after t1, resulting in the start of output of d2 being turned off at ZCS and Q2. The previous equations in the mode are still valid for this time. At t2, the resonant voltage vr1 has reached zero after an alternative resulting in d1 being biased forward at ZVS. Duration from t0 to t2, where the loads and discharges of Cr1 are parameterized by π1 as shown.

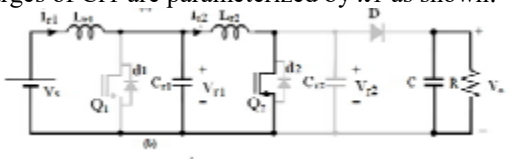

Fig 2(b) mode 2

Mode III (t2 – t3): During this cycle, the input voltage source VS charges Lr1 linearly. The current of Lr2 in the d1-Lr2-Q2 loop is constant and freewheels until the Q2 switch is turned off at t3. The Q2 turn-off is performed under ZVS conditions due to the externally parallel capacitor C2 (and the internal output capacitance of the switch Coss). [10]-[17].

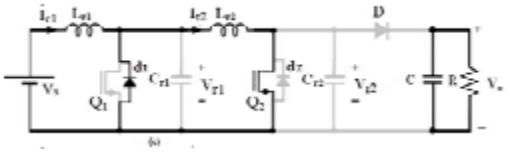

Fig 2(c) mode 3

Mode IV (t3 – t4): The diode d1 is still in development and Lr1's cur rent rises linearly. Lr2 and Cr2 are forming a resonan t network. The voltage vr2 increases sinusoidally unti l it hits VO at t4 and thus the rectifying diode D at Z VS is biased forward.

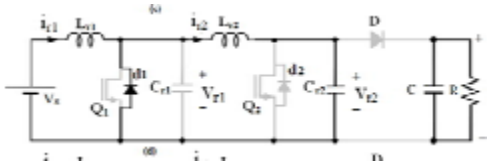

Fig 2(d) mode 4

Mode V (t4 – t5): The diode D is being performed and the output is being supplied with fuel. Ir2's magnitude is declining, while ir1's is rising. The ir1 and ir2 currents are identical at t5 and thus the d1 current is zero. Then at ZCS d1 is turned off. The Q1 gate should be set high at any time in this mode to turn the MOSFET on at ZVS.

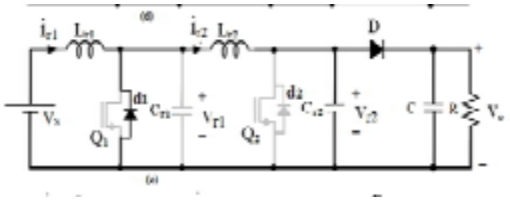

Fig 2(e) mode 5

Mode VI (t5 – t6): The output diode D is still working and the magnetic energy stored in Lr2 feeds the output. The Q1 switch now performs and holds ir1 and ir2 activities the same as before. Still true are those formulas. This mode goes on until ir2 reaches zero at t6 and D is turned off at ZCS

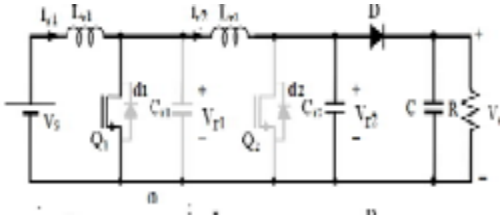

Fig 2(f) mode 6

Mode VII (t6 – t7): The Q1 turn stays ON while D is OFF. Lr2 and C r2 create a resonant circuit and therefore Cr2is discha rges into Lr2. Thus the voltage vr2 sinusoidally decre ases until it reaches zero at t7. The new ir1 continues to grow linearly.

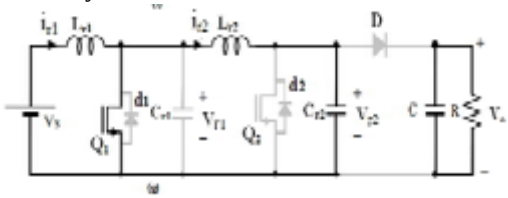

Fig 2(g) mode 7

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Mode VIII (t7 – t8): The antiparallel diode d2 is biased forward at ZVS by hitting vr2 to zero at t7 and provides a freewheeling direction for ir2. Lr1 is still magnetizing and there is a linear increase in its current. The Q2 gate signal should be set high during this phase to turn it on at ZVS. The Q1 toggle is turned off at t8. Under the ZVS conditions, Q1 turn-off is performed due to Cr1

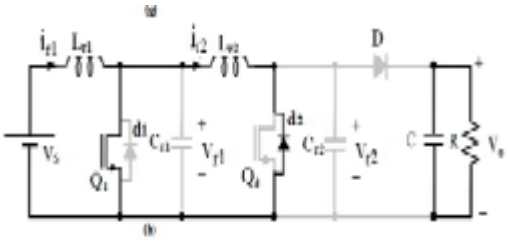

Fig 2(h) mode 8

4. SIMULATION RESULTS

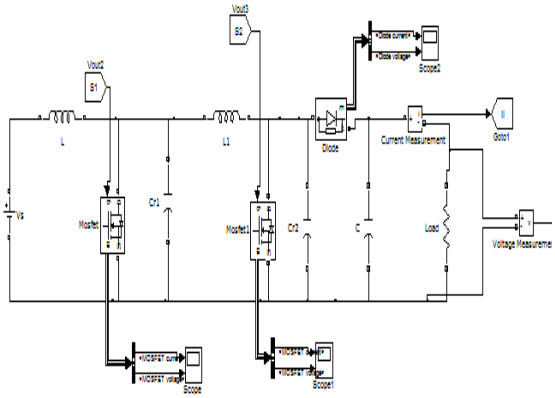

Fig.3 Simulink Model Of Closed Loop Resonant Zvs Boost Converter

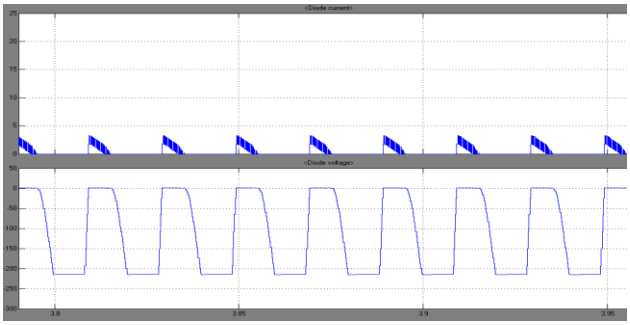

Fig.4 D1 voltage&current under open loop Configuration

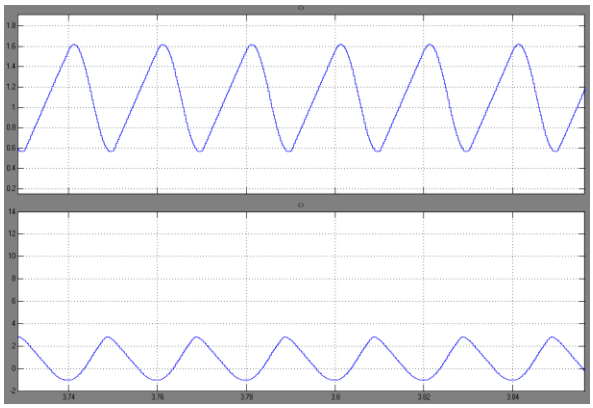

Fig.5Lr1&lr2 under open loop Configuration

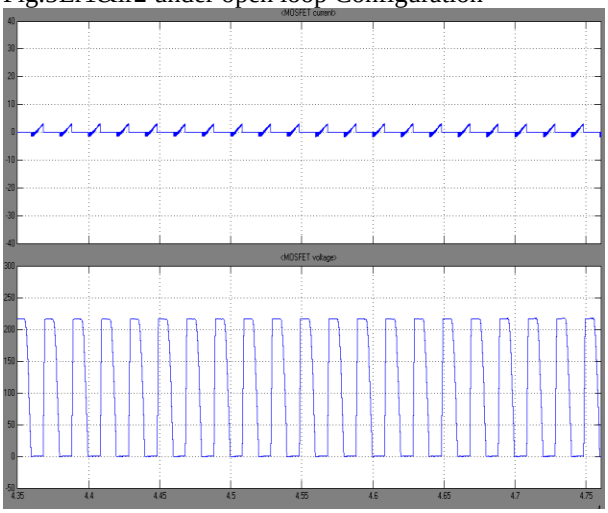

Fig.6 Q2 voltage & current under open loop

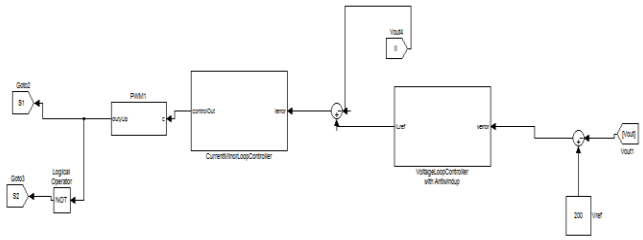

Fig.7 control diagram

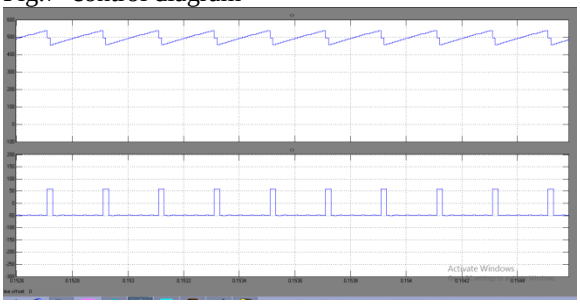

Fig 9 inductor currents under closed loop

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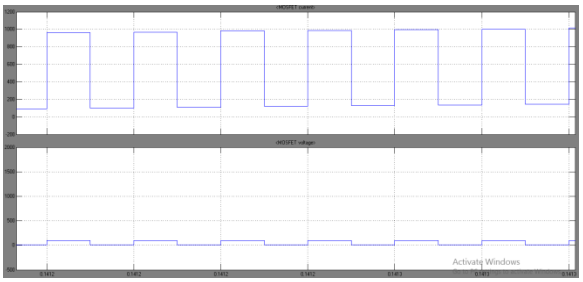
Fig 10 Q1 voltage current under closed loop

CONCLUSION

Including two LC resonant high frequency tanks and two grounded switches, a new entirely ZVS boost converter is proposed. Switch activity in transient and steady states reduces voltage stress. ZVS operation is possible, which reduces switching losses and significantly regulates EMI outputs through Primary side switches when the ZVS dc-dc multi-output converter using proportional sharing. All major switches can realize ZVS, so the converter can operate with higher frequency of switching and higher efficiency. The operating phases, ZVS state and control information are also evaluated in the loop model.

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