TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 4344 - 4351

Design and Performance Evaluation of Gate-All-Around Nanowire FET at Sub-7nm Technology Node

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Article Info
Volume 82
Page Number: 4344 - 4351
Publication Issue:
January-February 2020

Abstract

In the Electronics world, there is a need of more and more scaling of semiconductor devices to march at the tempo of Moore's law so that we face less and less problems in making devices with shrunken dimensions at Nano scale. It has been found in the published literature that the GAA Nanowire FET shows favorable results as compared to the FinFET structure at the technology node beyond 10 nm. In today's time FinFET is assumed to be the Industry Standard Semiconductor technology for making an Electronics Product. Therefore, in this work, a TCAD study of the device GAA Nanowire FET at sub-7 nm technology node is carried out. The design and investigation of the influences of varying channel length in ultra –short nanometer regime on drain current is studied. And then we further investigate and analyze the variability in the performance trends of the device GAA NWFET at ultra-low power Drain voltage (Vds=0.05 V) by keeping the channel length, channel height and channel width constant at 5 nm scale and by varying the Channel doping concentrations, Gate Oxide thickness, Gate Oxide material and use of high–k dielectric materials in Spacer region. Further investigation of the influence of ultra-nanowire channel radius less than or equal to 3nm on device conductivity.

Article History
Article Received: *18 May 2019*
Revised: *14 July 2019*
Accepted: *22 December 2019*
Publication: *21 January 2020*

Keywords: *GAANWFET, Silicon Nanowires, Channel length, Oxide thickness, Spacer material*

I. INTRODUCTION

Nowadays, Silicon Nanowires attracting attention of researchers of various fields and they are finding applications of silicon nanowires as biological [1] and chemical [2] sensors, and as thermoelectric [3,4], photovoltaic [5], and Nano electronic devices [6,7]. In all of the above fields of study silicon Nanowire performs well due to their improved nanowire electronic properties. Electronic properties of the nanowires and performance of thermoelectric conversion [4] and bio-molecular sensing devices can be improved by reducing the nanowire diameter. Since the Silicon Nanowires have distinctive geometry which allows the more elementary process of fabricating of Multi-gate FETs. As the scaling of CMOS technology below 22 nm node, it is faced with the unavoidable short channel effects [8]. To overcome the SCEs, new device structures have developed gradually from classical planar transistors to multi-gate non-planar transistors like double gate, triple gate and to the latest FinFET and to endmost Gate-All-Around (GAA) technologies. Present day technological inventions are completely governed by

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scaling, low power consumption, lower SCEs and in this scenario FinFET as well as GAA technologies both are proving out to be the remedy for the production of sub-7nm chips.

Fin field effect transistors (FinFETs) are the most favorable device structure for large fabrication of devices beyond planar metal oxide semiconductors (MOSFETs) [9]. But further scaling down of the transistor dimensions is an incommodious job requiring novel architectures. As the width of fin in a FinFET transistor proceed towards 5nm, then slightly changes in channel width could result in unacceptable and mobility losses. Additionally, the propensity of radial and axial crystalline Hetro-structures of Nanowire with smooth surface, can repress the charge scattering [10]. Corner effects also has negligible influence on this device structure as the geometrical shape of the channel is replaced fromrectangular one to other polygon shapes like cylindrical shape channel, circular shape, etc.[11-13].Hence, deep study specially in terms of the ultra-short channel length of the latest GAA technology is very much important for future scaling and low power solutions.

II. DEVICE STRUCTURE AND PARAMETERS

Complete 3D device structure of GAA NWFET is shown in Fig.1 which shows the Source/ Drain electrode attached with source/ drain Epitaxy. Channel is fully wrapped up by the Gate electrode which in turn connected to the source/ drainEpitaxy through source/ drain extension. In Fig.2 the 3D structure of GAA NWFET channel along with its source

/drain extension only is shown as a Nanowire. The direction of channel is assumed to be along the z-axis of the structure. Channel region is lightly doped (NA=1012 cm-3). Metal Gate Work function φm = 4.6eV and the working Temperature is T=300k. The MOSFET is n- type and the device parameters are summarized in table1. Table 1 Shows the Value of Parameters Used in Simulation.

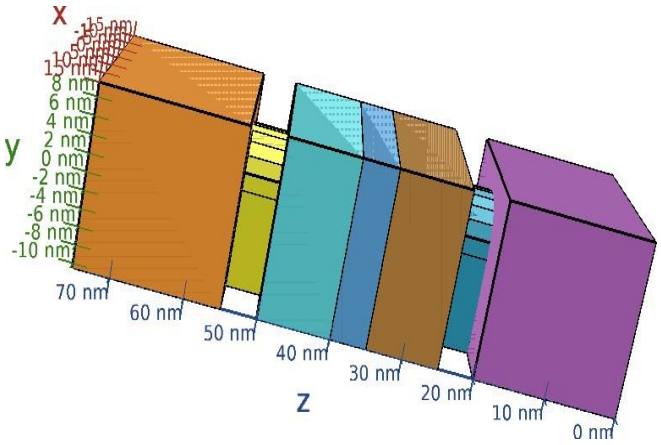

Figure 1 Complete 3D Structure of GAANWFET

Table 1: Parameters Used in Simulation

PARAMETERS	VALUES
Radius	2.00 nm
O xide thickness	0.920 nm
Contact Width	30 nm
Contact Length	20 nm
Epi Length	5 nm
Spacer Length	10 nm
Channel Length	5 nm
Channel Width	5nm
Channel Height	5nm
Source & Drain Doping	1e20 cm^{-3}
Channel Doping	1e12 cm^{-3}
Material	Silicon

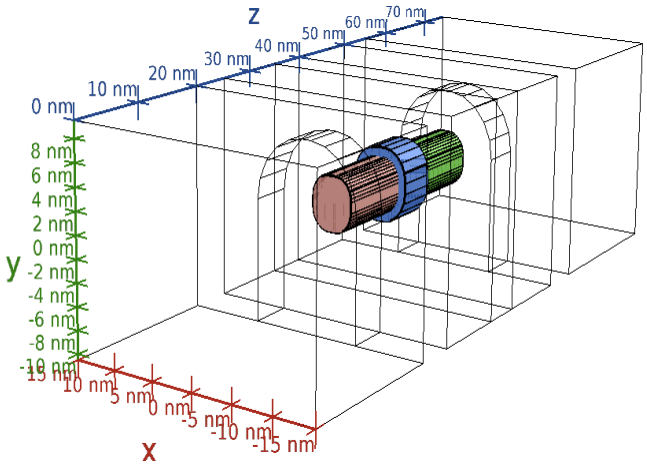

Figure 2 Nanowire Channel 3D Structure

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III. RESULTS AND DISCUSSIONS

Design and TCAD study of GAA NWFET is done based on the structure data. For the simulation purpose we have used Global TCAD Solutions tool [14] which is a Nano-device simulator. In this work, we have used Drift Diffusion model for NMOS specifically with Electron Quasi Fermi level (QFL) that is, DD_NMOS_QFL scheme. The drift-diffusion model numerically predicts device physics in equilibrium and calculates an exponential increase of the carrier concentration towards Si/SiO2 interface. The DD Model is preferred for the simulation of the device characteristics due to its fast speed and ability to efficiently use the time.

A. Influence of Channel Length Variations

Fig.3 shows the plot at constant Vds=0.05V transfer Characteristics at different channel lengths on log scale. Fig.4 gives the plot of Drain current for different channel lengths at linear scale. On reducing the channel lengths the drain current are increasing .This is because on reduction in channel length the threshold voltage also reduces which gives considerable rise to OFF Current and ON Current due to short channel effects like DIBL etc.

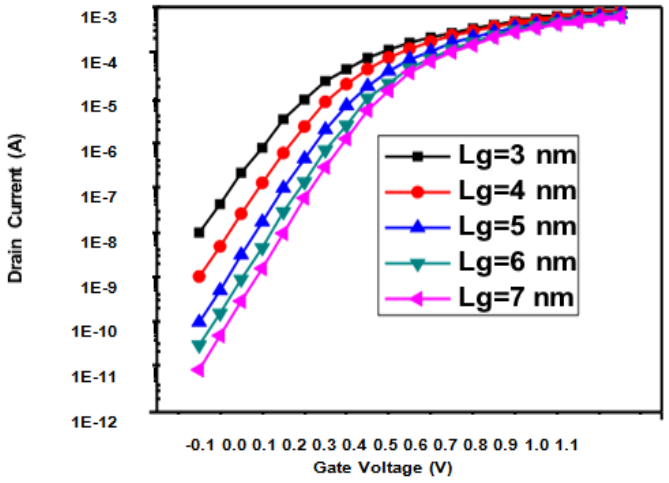

Figure 3 Id vs Vg Curve at Different Channel Length on Log Scale.

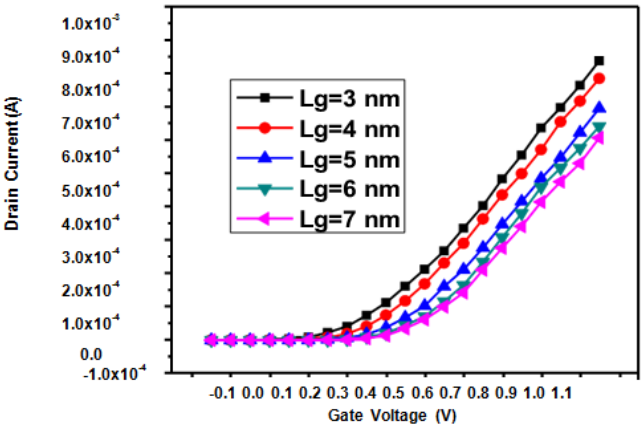

Figure 4 Id vs Vg Curve at Different Channel Length on Linear Scale.

B. Influence Of Channel Radius Variations

In this part, we studied the variation of the channel radius by keeping channel length, channel width and channel height constant at 5 nm scale in linear region at Vds=0.05V. Fig.5 and Fig.6 illustrates the effect of varying channel radius on drain current on linear and log scale respectively. From the graphs it is concluded that on reducing channel radius more no. of electrons available in the channel hence there is considerable increase in drain current. This is because lower the radius or diameter of the device higher is the gate controllability. Here radius r=1 has best gate controllability among the three.

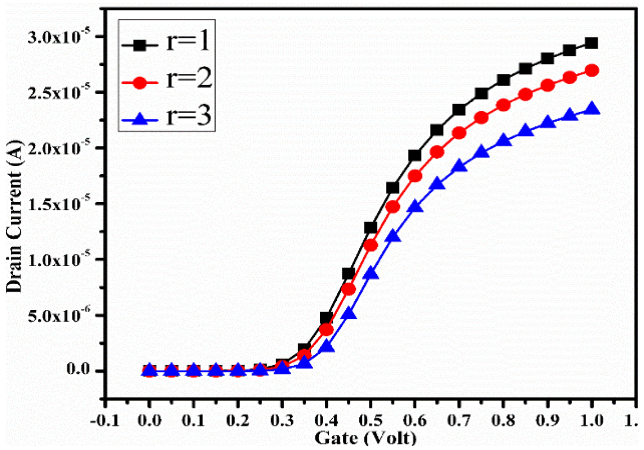

Figure 5 Influence of channel radius on Drain current at linear scale.

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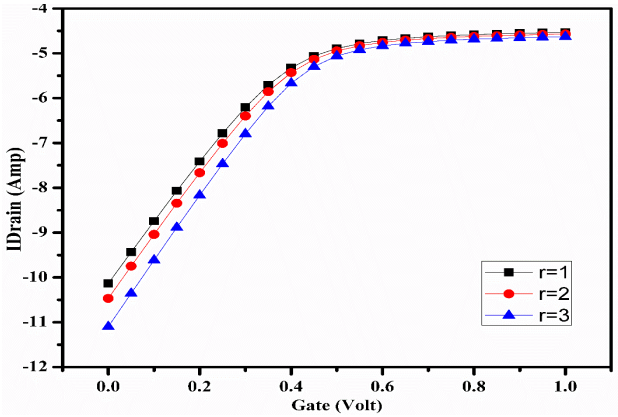

Figure 6 Influence of channel radius on Drain current at log scale.

C.Influence of Spacer Materials on Drain Current

Material of Drain /Source Spacer region also greatly affects the performance of the device mainly OFF current (IOFF) and have smaller effect on ON Current (ION). Fig. 7 shows the device structure indicating Drain/Source Spacer region and channel only while Fig.8 shows the effect of different spacer high-k materials on drain current. From the graph, we can see the trend that spacer materials having higher relative Dielectric Constant reflects lower OFF Current and small increase in ON Current. This is because higher the relative Dielectric Constant, more is the depletions in the channel which leads to increase in the effective channel length and hence OFF Current decreases making the device less leaky. From the graph we can conclude TiO2 is the best spacer material to be used among the materials we have taken but it is costly.

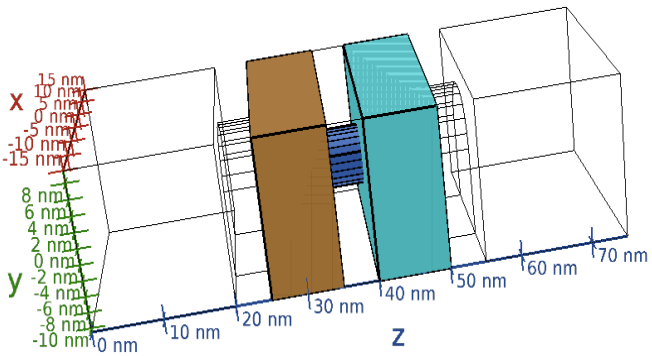

Figure 7 Device showing Drain/Source Spacer region

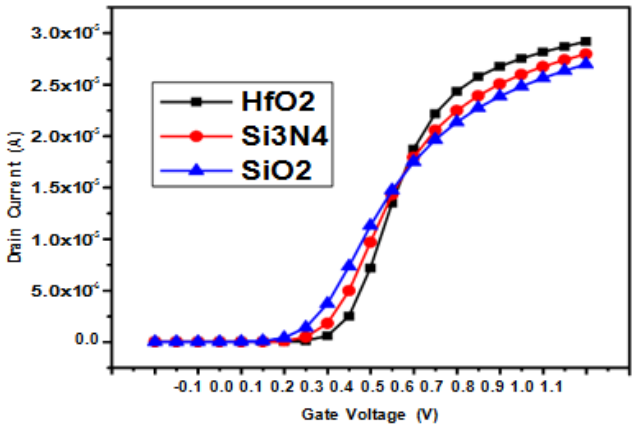

Figure 8 Effects of different Spacer material on Drain current

D. Influence of Gate Oxide thickness on Drain Current

Fig.9 & 10 illustrates the effect of variation of Gate Oxide thickness at linear and log scale respectively. From the graph it is concluded that on decreasing oxide thickness there is considerable decrease in OFF Current and increase in ON Current .Hence, it shows the improvement in ION/ IOFF and/or switching speed.

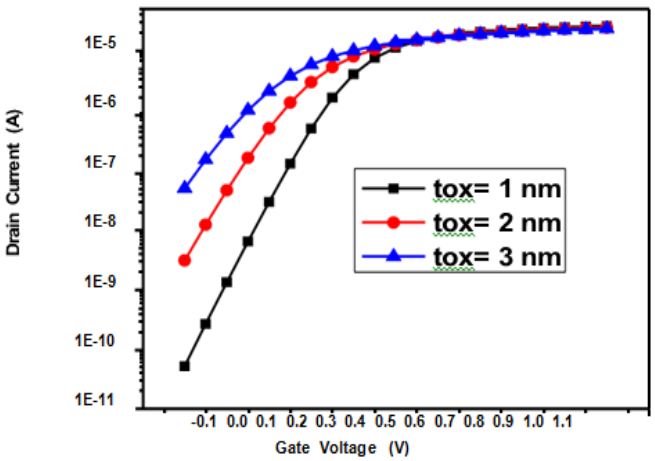

Figure 9 Effect of Gate Oxide thickness variation at linear Scale

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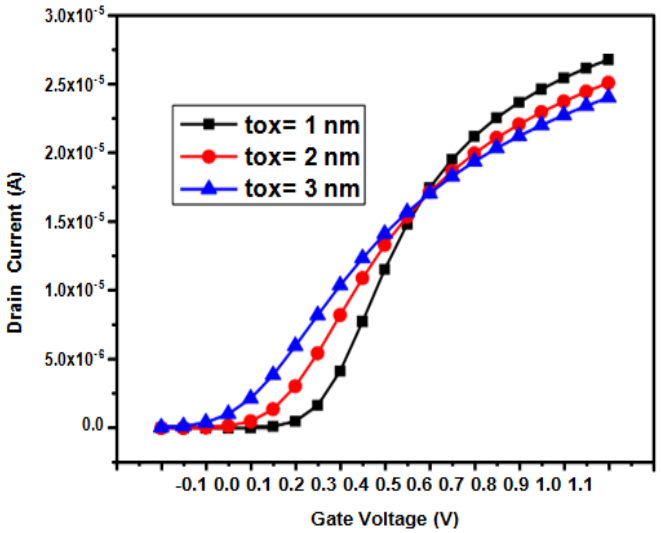

Figure 10 Effect of Gate Oxide thickness variation at log Scale.

E. Influence of Gate Oxide Materials on Drain Current

In Gate Oxide we vary three materials (HfO2, Si3N4 and SiO2) whose effects are shown in fig.11 &12 at linear and log scales respectively. HfO2 shows the best transfer characteristics among the three. This is because of its higher dielectric constant than Si3N4 and SiO2.

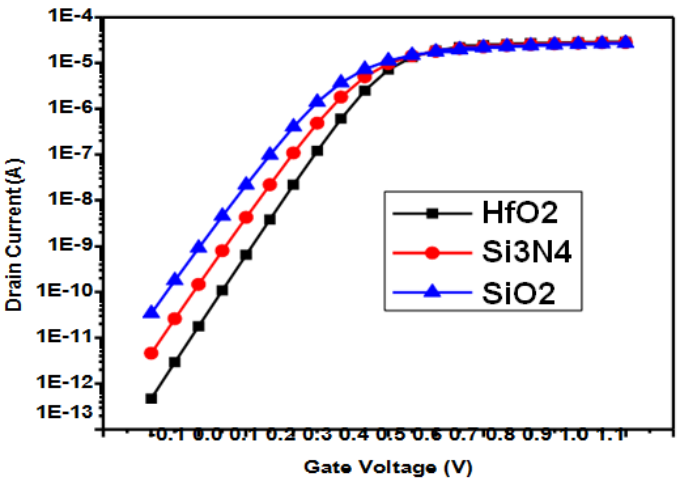

Figure 11 Effect of Gate Oxide material variation at log Scale

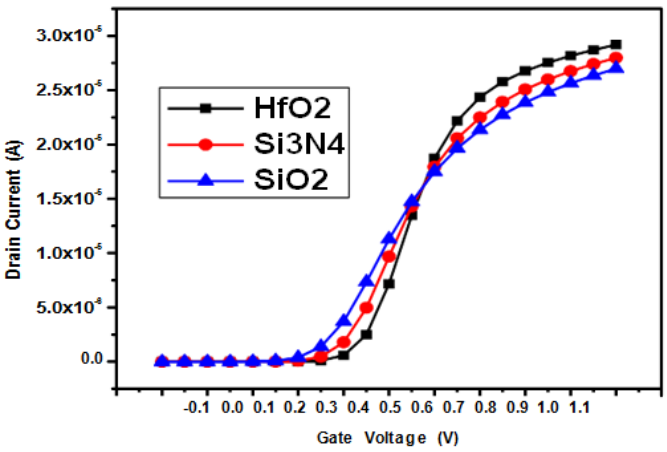

Figure 12 Effect of Gate Oxide material variation at linear Scale.

F. Influence of Channel Doping Concentration Variations

Fig. 13&14 represents the Electron and Hole concentration in the channel. Higher the amount of carrier concentration in the channel, higher will be the drive current of the device as shown in Fig.13. Fig.15&16 illustrates the effect of varying doping concentration in the channel on drain current in linear scale and log scale respectively. Lower is the value of doping concentration in the channel, lesser is the threshold voltage of the device, and hence higher the value of drain current. Vice- versa higher the value of doping in the channel, higher is the threshold voltage of the device, and hence lesser is the current value. However from figures we see that doping variation is not affecting much more the drain current.

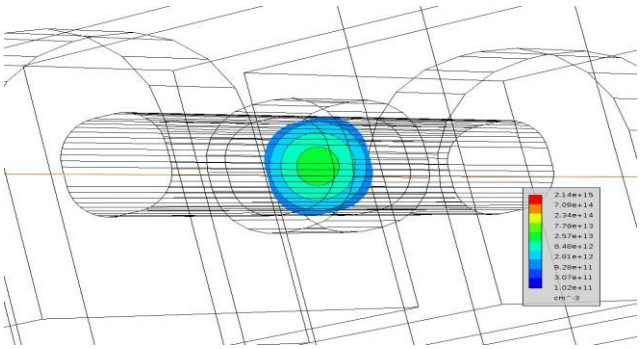

Figure 13 Channel Electron Concentration 2D cutline profile

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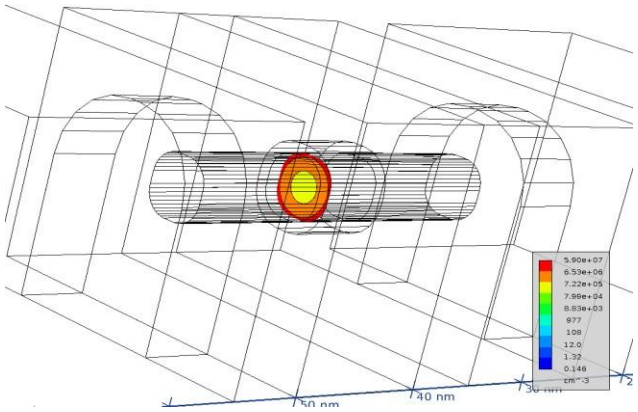

Figure 14 Channel Hole concentration 2D cutline profile

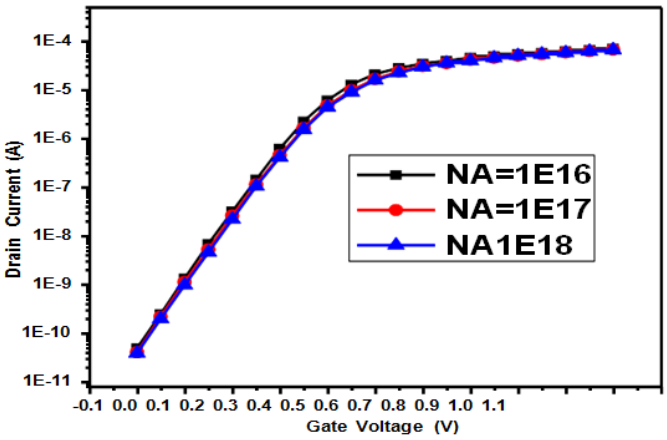

Figure 15 Id-Vgs curve of Different Channel Doping Concentrations in log scale

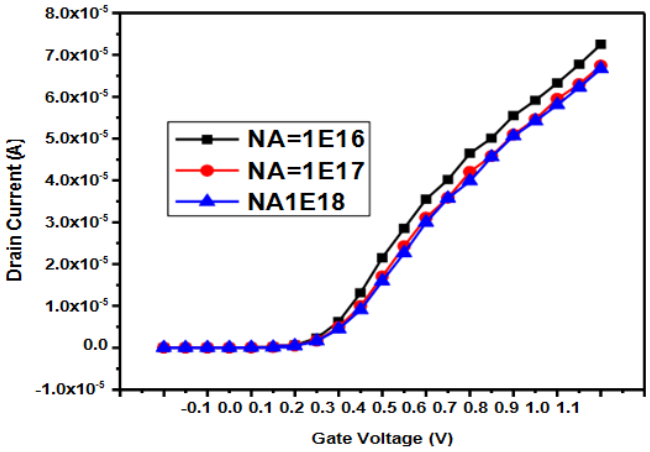

Figure 16 Id-Vgs curve for different channel doping concentrations in linear scale

G. Influence of Channel Material on Drain Current

Here Fig. 17 & 18 are plotted at Vds=0.05V which illustrates the effect of using different materials in the channel by keeping channel length constant at 5nmand channel radius at 2 nm in linear and log scale respectively. From the graphs we found that Si has lowest drain current while SiGe has higher and Ge has highest value of Drain current. This is because of energy band gap (EBG) value and also mobility value. Si has highest bandgap energy (1.12 eV) among the three while Germanium has lowest (0.66 eV). SiGe has the EBG value in between 0.66 eV to 1.12 eV. Lower the energy band gap (EBG) value higher the chances of excitation of electrons from Valence Band to Conduction Band hence higher conductivity of the device. Higher is the mobility, higher is the current value, this is so Ge has the highest value of drain current in OFF-state and ON-state. Si channel device have better performance in terms of SCEs than SiGe and Ge.

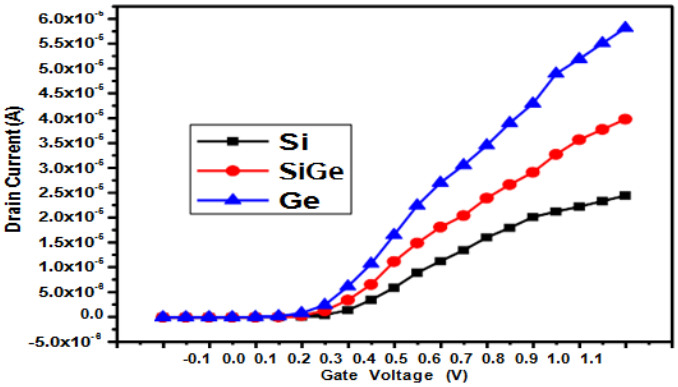

Figure 17 Influence of different channel materials on Drain current at linear scale

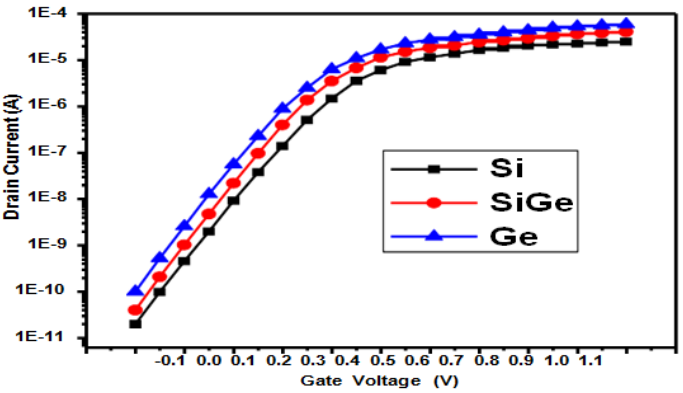

Figure 18 Influence of different channel materials on Drain current at log scale

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IV. CONCLUSION

The performance of NMOS GAA NWFET have been evaluated in this paper, by means of simulation studies using Global TCAD Solutions. The significance of this work is to explore better performance of Si GAA NWFET in terms of higher conductivity, higher ON-current to OFF-current ratio, higher switching speed, suitability to ultra-low power device. Spacer region materials with divergent high-k materials (SiO2, Al2O3, Si3N4, HfO2 and TiO2) is analyzed at 5nm technology node. Channel length for ultra-short range like (3nm, 4nm, 5nm) at constant channel height, channel width and channel radius is analyzed. Channel radius for ultra- nanowire ranges like (1nm, 2nm, 3nm), Gate Oxide thickness and Gate Oxide Material at constant channel length 5nm is analyzed. Also, the effects of varying the amount of doping concentration in the channel on Drain current is studied.

Future Scope:

The presently used Drift –Diffusion Model in simulations presumes a ballistic transport mechanism that means transportation of carriers neglecting scattering effects in the channel. Hence more advanced suitable quantum confinement Models like Density Gradient and VSP QFL should be used for accurate results and to account the surface scattering effects, dominating at very ultra-short nanometer regime. Further investigation could be done with new materials like GaAs, InP, AlAs, etc. nanowire channel and by employing high-k spacer with low-k dielectrics. Different orientation variation in the channel and stress applications can also be investigated for the higher conductivity.

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