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Performance Evaluation of Low Power Adiabatic Techniques

Shipra Upadhyay[1], Amit Kumar Pandey[2] and Shailendra Kumar[3]
[1]Department of ECE, RajarajeshwariCollege of Engineering, Bangalore, India[2]
Department of Applied Science and Humanities, Rajkiya Engineering College, Ambedkar Nagar, India
[3]Indian Space Research Organization (ISRO-HQ), Department of Space, Bangalore, India.

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Abstract:
Due to the fast growth in the semiconductor technology and miniaturization of integrated circuit, low power is one of the interest areas of concern in all digital applications. Reduction of transistor size increases the numbers of transistors on a single chip. Consequently, due to these technological upgradations, the challenges faced by circuit designers such as leakage currents are also enhanced. For low power computations, current in a circuit can be scaled down from nano-amperes to pico amperes with the use of energy recovery techniques based on adiabatic logic circuits. In this paper, some energy recovery techniques have been reviewed and their performances have been compared based on the various parameters such as power consumption, operating frequency and the area occupied by them.

Keywords: Power, leakage current, adiabatic logic.

1 Introduction

The size optimization and increasing integration of electronic circuits has opened an interesting area for researchers that include low power circuit designing. In modern electronic circuits the basic component is the CMOS circuit. The way technology is growing accordingly size of these CMOS circuits are also reducing and thus some new factors play important roles in power calculation. Leakage current is one of the important parameter in nanometer and below technology.

Adiabatic charging and charge recovery techniques are efficient methods for low power designing. The concept of adiabatic logic is taken from the thermodynamic system. In such processes, heat exchanged with the environment is almost zero and therefore heat loss is negligible. Similarly, adiabatic logic technique minimizes energy dissipation by keeping the potential drop across the end terminals small at all times. In CMOS technology, during the switching operation switching power consumption occurs at the load capacitance. Adiabatic technique minimizes the losses in discharging phase because here charge does not get discarded from the load capacitance to the ground, it flows back to the power supply and can be reused. This technique is known as charge recovery or energy recovery method. Further, in order to minimize the losses, number of design methodologies is proposed.

In literature, to implement adiabatic logic circuits various time varying power supplies which are also known as power clocks are used. The frequency of power clock is always much higher than the technological limits. There are two kind of energy losses namely adiabatic losses and non-adiabatic losses in adiabatic circuits. The adiabatic losses occur when the current flows through a

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non-ideal switch proportional to speed of the work. The non-adiabatic loss is due to drop in voltage between a switch's two terminals when it is closed, this loss is not related to the working frequency but to the drop in voltage and capacitance of the node. An instance of a non-adiabatic loss is the dissipation of energy at the diode terminals.

2 Power consumptions in CMOS

In CMOS circuit, power drawn from the V_{DD} pin can be calculated in different ways: instantaneous power, average power, peak power, RMS power, energy etc. Among them average power calculation is most important because it reflects battery life. The three major sources of average power consumption in CMOS circuits are switching power consumption, short circuit power consumption and leakage power consumption.

Although in deep sub-microns and below technology, leakage current plays a big role but still the 75% of total power consumption is due to the switching power consumption. Consequently, number of methods has been investigated to reduce switching power consumption and most interesting method is adiabatic technique.

3 Power Reduction by using Adiabatic Technique

Adiabatic logic circuit attempts to lower the energy consumption without sacrificing the driving capability and other performance merits like high voltage operating capability etc. In adiabatic circuits energy dissipation during charging is less and most of the energy is returned to supply during discharging. Here, a time dependent power supply is used whose rise and fall times are longer than RC time constant of the node (R denotes the resistance of transistors and wiring resistance etc.). It charges the output node to the same voltage as CMOS, but over a longer time. In this way there will be a very small potential drop across the switching transistor. Also these types of circuits have peak currents many times smaller than the CMOS circuit. Since we know that the power dissipation is I^2 R so as I reduce, power and energy dissipation also reduces.

We may categorize adiabatic circuits in three types: (a) On the basis of their energy reduction performance. (b) On the basis of their energy recovery performance. (c) On the basis of their working structure. In the first one, we have fully adiabatic circuits, partially adiabatic circuits and non-adiabatic circuits. In fully adiabatic circuits, operation is performed very slowly, and at such a low frequency there will be very little energy dissipation (almost negligible) [1-5]. In partially adiabatic circuits, due to the some irreversible circuit operations some energy is wasted and some is regained [3-6]. In non-adiabatic circuits there is no provision for charge transfer at reduced potential drop and recovery to the power supply. The second categorization is reversible and irreversible adiabatic circuits.

In adiabatic circuits the word reversibility refers to thermodynamic reversibility not logical reversibility. Thermodynamic reversibility means, there will be a very small energy dissipation (almost zero) when circuit is operated very slowly (adiabatically). In logically reversible circuits from the output, we can predict the input. Logical reversibility does not assure thermodynamic reversibility. Inverter is an example of logically reversible circuits whereas adder is an example of logically irreversible circuit. Reversible adiabatic circuits are complex and difficult to implement as compared to irreversible adiabatic circuits. Third classification on the basis of circuit design

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and operation is static and dynamic adiabatic circuits[9].

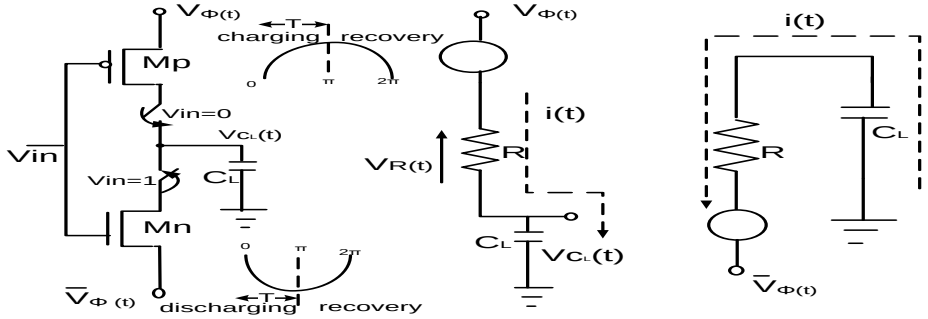

Fig 1.Adiabatic charging and discharging.

4 Literature Survey of several Adiabatic Techniques

In past years, multiple numbers of adiabatic circuits have been proposed and due to their limitations and shortcomings still researchers are focusing to improve the performance by proposing new topology. In this paper authors have reviewed some of the effective adiabatic circuits and furthermore compare their performance in a tabular form.

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4.1 Positive Feedback Adiabatic Logic (PFAL) Circuits

PFAL circuit uses four phase clock and it does not have any DC power source. The phases used in PFAL are ideal, evaluate, hold, and recycling stage. During evaluation phase the logic is evaluated according to the given inputs, the output of evaluation phase is retained in the next phase which is hold phase. The charges stored in load capacitor is recycled and recovered back in recycling stage. The problem with PFAL circuit is that, it does not provide full recovery of energy and hence it is also known as semi adiabatic circuit.

4.2 Efficient Charge Recovery Logic (ECRL) Circuits

This is also a partially adiabatic logic circuit as PFAL circuit. In this logic there are two phases namely pre-charge and evaluation. The logic function is evaluated by pull down network of NMOS transistors and also through PMOS transistors. It has a problem of logic level degradation for pipelined stages.

4.3 2n-2n2p Logic Circuits

This logic is quasi adiabatic irreversible logic. It has pair of cross coupled PMOS transistors and NMOS transistors. Unlike the previous circuits, it uses PMOS devices to recycle the energy.

4.4 Complementary Energy Path Adiabatic Logic (CEPAL) Circuits

CEPAL circuit consists of two charging MOS diodes (M1 and M6), a pull-up (M2) transistor, two discharging MOS diodes (M4 and M5) and a pull down (M3) transistor. Two sinusoidal supply voltages clocks in complementary phases are used. For low input logic, M2 transistor turns ON and M3 transistor turns OFF. Output node follows power clock or complementary clock and swings HIGH. When the energy clock swings down, it forces the output node to float, but this issue is removed immediately because the energy clock followed swings up at the same moment. Thus small voltage at output node is eliminated. CEPAL does not have any hold phase compared to other adiabatic logic circuits. By removing the hold stage, CEPAL circuit tries to enhance and remove the disadvantage of previous circuits. The CEPAL circuit has excellent driving ability and immunity, and its throughput does not depend on frequency ratio (i.e. supply frequency ratio to frequency of input transition).

4.5 Quasi-Static Energy Recovery Logic (QSERL) Circuits

This circuit resemblance to the static CMOS logic circuit. It has two additional MOS diodes and two feedback transistors compared to conventional CMOS circuits. It is consisting of a PMOS transistor, a MOS diode and a feedback transistor in charging path, an NMOS transistor, another MOS diode a feedback transistor in recovery path and two complementary sinusoidal supply clocks. The charging path diode controls the charging while other diode controls the discharging. Feedback transistors are used to lower charging and discharging path resistance. Supply clock signal consists of two phases namely evaluation and hold. During evaluation phase, power clock swings up while complementary clock swings down and both the diodes become forward biased. When the PMOS pull-up transistor turns ON, output node follows power clock. When the pull down transistor turns ON then output node follows complementary clock. During hold phase, power clock swings down while complementary clock goes high, the circuit node remain unchanged due to the diodes. The QSERL circuit has hold phase. Hence dynamic switching is less and energy

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dissipation reduces. Output node is floating which is not desirable.A feedback keeper is required to remove the floating output (i.e. susceptibility to noise) of hold phase. This causes larger area and power overheads problems. QSERL circuits are comparatively more power efficient than CEPAL circuits. The large delay resulting from QSERL combinational logic is very important to discuss and remedy.

4.6 Glitch Free Cascadable Adiabatic Logic (GFCAL) Circuits

The GFCAL circuit operates with single slowly varying triangular power source, and does not need multiphase clocks. Circuit is composed of one PMOS and a diode in parallel with one NMOS and a diode, and a load capacitance (C) is connected in series with them. When input is logic '0', T1 is ON and T2 is OFF and capacitor(C) is charged through the path T1, D1. When supply voltage is decreasing from peak value and less than the output voltage,D1 becomes reverse biased and discharge into the supply through D1 is restricted. Similarly, for input logic '1', T2 and D2 path allows discharging. The GFCAL circuit has approximately the same input and output logic levels.

The GFCAL circuit is based on a triangular power clock with the lowest power dissipation among all, at same time it has main drawback is very large delay and therefore very slow speed of operation.

4.7 Two Phase Clocked Adiabatic Static CMOS Logic (2PASCL) Circuits

In this design, the charging path diodes are removed, therefore current only flows through the transistor during charging, reduces the diode-based circuit disadvantages. In this circuit, split level sinusoidal power clocks are used, which have some benefits such as decreased delay and dissipation of energy, high output swing, and so forth. The 2PASCL has reduced switching activity and there is a tiny ripple of amplitude at high and low logic levels induced by switching transistor ON / OFF resistances and load capacitance. Thus the output is degraded.

4.8 Diode Free Adiabatic Logic (DFAL) Circuits

It has less number of transistors and hence occupies less area as well as lesser power dissipation. Delay is the parameter which has to be minimized to improve the circuit performance.

4.9 *Improved Quasi-static Adiabatic Logic (IQSERL) Circuits*

Table 1. Comparison of various adiabatic techniques

Adiabatic technique	Output	No of devices used	No. of power clock	Clock Style	Power Diss.	Merits	Demerits
PFAL	degraded	6	1	trapazoidal	High	Power diss. Less than CMOS	Partial recovery
ECRL	degraded	4	1	trapazoidal	High	Power diss. Less than CMOS	Partial recovery
2N2N2P	degraded	6	1	trapazoidal	High	Power diss. Less than CMOS	Partial recovery
CEPAL	correct	4	2	sinusoidal	mediu	Correct	Large area

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					m	output	
QSERL	degraded	2	2	sinusoidal	low	Less power dissipation	Floating output
GFCAL	degraded	4	2	triangular	low	cascadeable	Output degradation
2PASCL	correct	4	2	Split level sinusoidal	low	Delay is less	Non adiabatic losses
DFAL	correct	3	2	Split level sinusoidal	lowest	Lowest	non adiabatic losses

5. Conclusion

In this paper, detailed study and comparison of various reported adiabatic logic circuits have been provided.It is observed that adiabatic logic circuits can be a very efficient logic to implement digital circuits in which power is the main concern and delay is not that important. We have observed that there is a scope of further improvement in these circuits. Adiabatic power supply generation and uses is a complex method, these circuits can be improved by proposing a more simple power supply similar to conventional power supply. All the discussed adiabatic logic circuits have some merits and demerits like QERL circuit suffers from floating output. In CEPAL circuit there is a problem of large area. In the 2PASCL circuit power dissipation is mainly due to non-adiabatic losses which cannot be avoided. Further, it is observed that GFCAL circuits have very lesser power dissipation, larger delay and degraded amplitude in comparison to the QSERL, CEPAL and 2PASCL circuits.

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