

Design and Research on Low Power SRAM using Adiabatic Technique with 180nm and 90nm Technology

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Abstract

The low power IC's are essential in all electronic portable equipment's. The performance of the circuit is reduced due to speed of the operations (write and read). The adiabatic technique is used in SRAM and also sense amplifier flip flop and pre-charge circuit. Employing of Adiabatic technique in bit line Static Random Access memory, the power consumption is decreased. The project aims to demonstrate successful read/write operations of adiabatic SRAM and compare its power dissipation with conventional SRAM in 180nm and 90nm technology.

Keywords: SRAM, adiabatic technology, BL, WL.

I. INTRODUCTION

With the rapid growth of modern communications and signal processing systems, handheld wireless computers and consumer electronics are becoming increasingly popular. The SRAM is major component only occupy larger area of the chip die and for SOC designs, the technology selection and system design choices are mainly driven by digital circuit requirements.

The importance for static random-access memory is increasing with enormous use in mobile products, System On-Chip (SoC) and high-performance VLSI circuits. SRAM is significant component used for the cache memory which is intermediate memory in the memory hierarchy, placed between the main memory (usually DRAM – Dynamic Random Access Memory) and the processor. They are designed to work in the same or very close processor frequency. Also finds its application in the main frame computers, engineering workstations and memory in hand-held devices due to high speed and low power consumption. SRAMs need to be not only fast but also reliably, i.e., it must be stable and robust to the system work properly.

Low power SRAM implementation is used to demonstrate the feasibility of low power memory

design. SRAM is constructed using the basic six transistors SRAM cell. They propose the design for low power SRAM memory using Schematic Editor Virtuoso. Peripheral circuits like, Write driver circuit, bit cell Sense Amplifier and Pre-charge Circuit are to be designed and implemented. The paper aims to implement memory cell and demonstrate successful write and read operations.

In their work adiabatic technique were used for reduction of average power dissipation. Simulation of 6T SRAM cell has been done for 180nm CMOS technology. It showed that average power dissipation was reduced up to 75% using adiabatic technique. An SRAM is considering in the most development stage today, with its different variations as well as to support low power application. Stability factor and Leakage power is becoming the most important factor on SRAM (Static Random Access Memory) cells. In the current VLSI digital circuits, power consumption is one of the main design concerns. Power consumption has become a critical concern in both high performance and portable applications. In their work low power technique is discussed, that is adiabatic technique. The performance of conventional 6T SRAM circuit is compared with adiabatic 6T SRAM circuit.

Using. The major reason for the power leakage in SRAM could be a bitline.

II. IMPLEMENTATION

The adiabatic SRAM design is to diminish leakage current and static power of the adiabatic static random access cells and also retains the data stored during the idle mode. The basic conception of the adiabatic SRAM is the applying of two pass transistors that provide various ground supply voltages to the adiabatic SRAM cell for normal and idle mode. One pass transistor applied positive voltage when the adiabatic SRAM cell is in idle mode and another pass transistor endow a virtual ground when the cell is in active mode. If the operation of conventional SRAM is changed to quasi-adiabatic mode, the input waveforms use the trapezoidal pulse.

Upon activation of wordline cell will be activated so that we can push the data by write driver on to the bitline, thus data is stored in q. The latch circuitry can store previous data until next data is pushed. In read operation the data which is available in bit line can be perceived by sense amplifier. The input supply is given with the trapezoidal pulse.

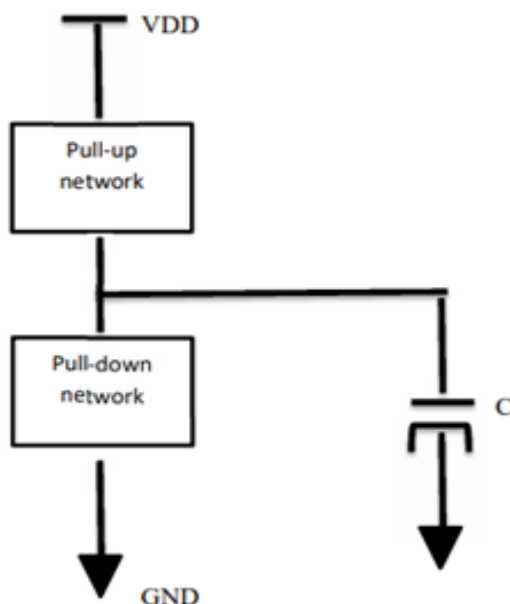


Figure 2.1: Adiabatic charging method

CMOS Static Random Access Memory Cell

By utilizing cross-coupled CMOS inverters a low power SRAM cell designed. Because of this circuit

topology the static power dissipation is very compact; essentially, it is restricted by small leakage current.

The privilege of this design is high noise immunity due to greater noise margins, and the ability to operate at lower power supply voltage. The major disadvantage of this topology is larger cell size.

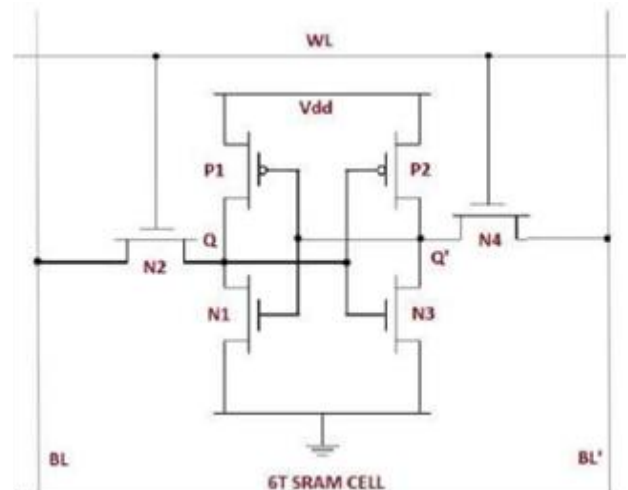


Figure 2.2: CMOS SRAM Cell

PRE_CHARGE CIRCUIT

The pre charge circuit is the main circuit that is constantly utilized within SRAM cell. The job of the pre charge is to charge the bit and bitline bar to $V_{dd}=1v$. The precharge circuit empowers the bit lines to be charged high at all times aside from throughout read and write operation. The following Circuit diagram shows the pre charger where „pre“ is the control enable for pre charging. As Sense Amplifiers (Used to sense data) are very frailty to differential noise on the bit lines because they detect small voltage differences. If bitlines are not precharged long enough, residual voltages on the lines from the previous read may cause pattern dependent failure. An equalizer transistor can be added to the bit line conditioning circuits to reduce the required pre-charge time by ensuring that bit and bit_b are at nearly equal voltage levels even if they have not pre-charged quite all the way to VDD.

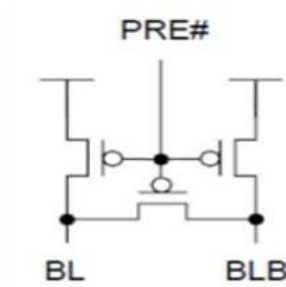


Figure 2.3: Pre-charge Circuit Diagram

SENSE AMPLIFIER

The low power signals are sensed by sense amplifier, the read bit will read data from the memory cell and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

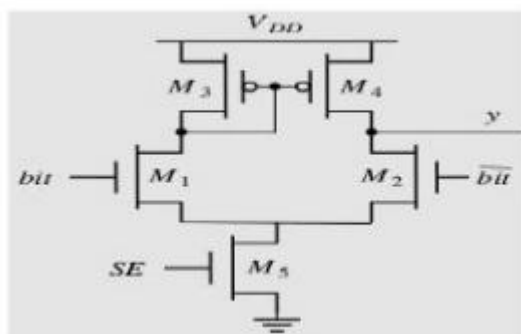


Figure 2.4: Sense Amplifier

III. SIMULATION RESULTS

Conventional SRAM

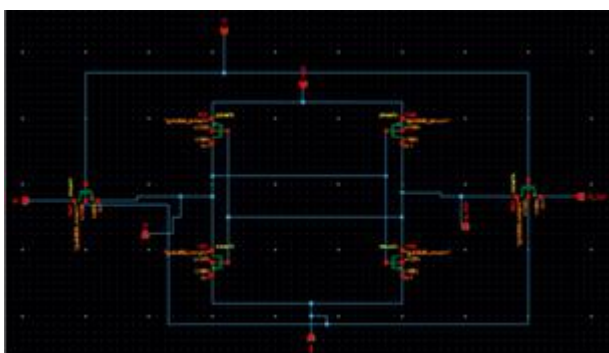


Figure 4.1: schematic of SRAM cell

The 3.1: Figure depicts the schematic of SRAM cell which is used for storing 1 bit of data. Upon activation of wordline cell will be activated so that we can push the data by write driver on to the

bitlines, thus data is stored in q, qbar . The latch circuitry can store previous data until next data is pushed. In read operation the data which is available in bit lines can be sensed by sense amplifier.

Here inputs (V_{dc} and V_{pulse}) are given and simulated.

TEST SCHEMATIC

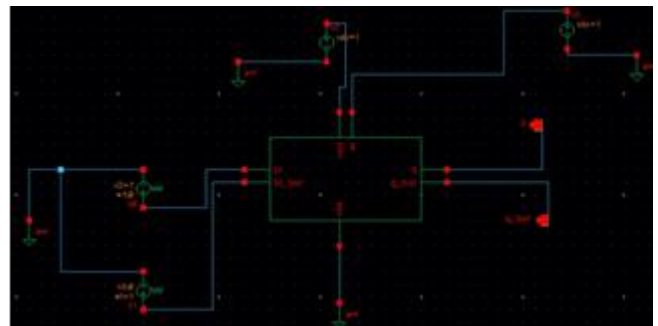


Figure 3.2 Test schematic of SRAM cell

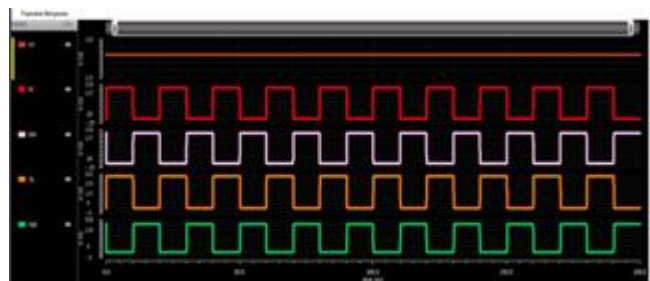


Figure 3.3 Waveform of SRAM cell

Here bl, bl_bar will act as inputs to the SRAM. The outputs q, q_bar are replica of those bitlines.

PRE CHARGE

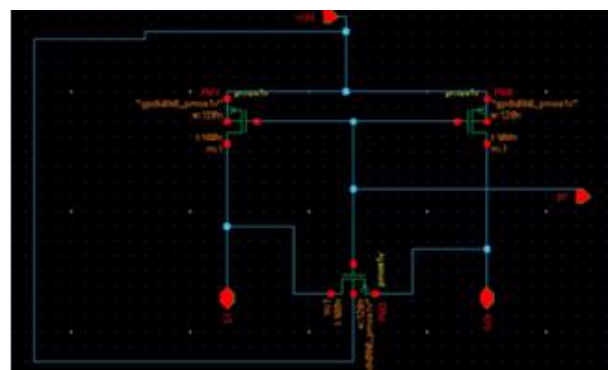


Figure 3.4 Schematic of PRE CHARGE

Pre_charge circuit is used to charge the bitlines when both write and read operations are not in process. When "Pre" is logic "0" then both bit-lines bl_bar and bl charged to high through "Vdd".

SIMULATION WAVEFORM

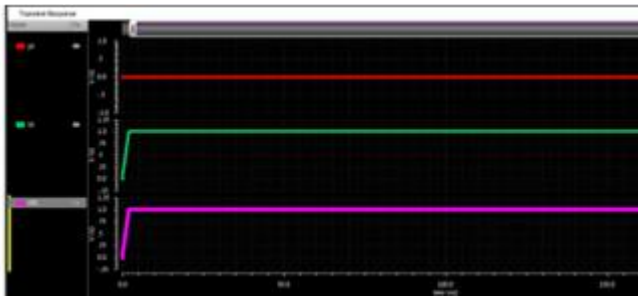


Figure 3.5 Waveform of PRECHARGE

Here, Pre controls the charging of bit lines.

Write driver circuit

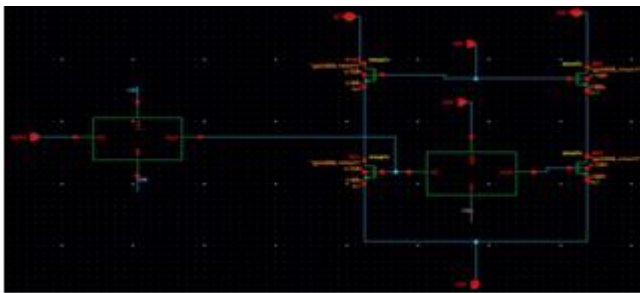


Figure 3.6 Schematic of WRITE DRIVER

By adding a low voltage and a high voltage at two points of the cross coupled inverters. Upon activation of it, the data is pushed on to the bit-lines bl, bl_bar which is then moves to SRAM cell and stored in q and q_bar

SIMULATION WAVEFORM

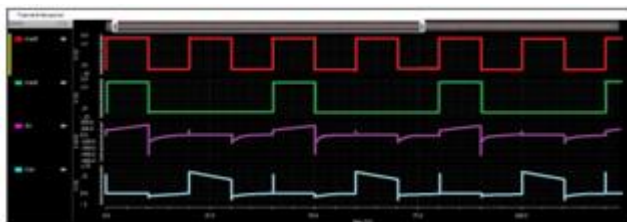


Figure 3.7 Waveform of write driver

The above figure shows that when write enable is high, data in that particular duration is pushed to bl, bl_bar.

SENSE AMPLIFIER

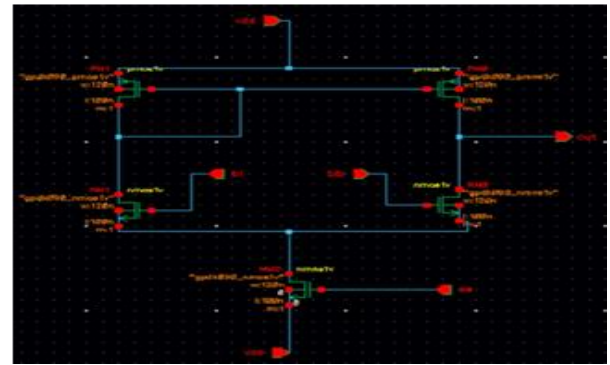


Figure 3.8 Schematic of SENSE AMPLIFIER

By the enabling of sensenable the data which is stored on the bitlines is sensed and shown as "OUT" signal. i.e, For reading "1" NM0 is ON, NM1 is OFF then output is high.

SIMULATION WAVEFORM

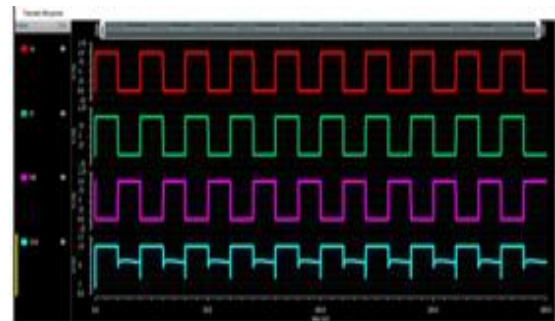


Figure 3.9 Waveform of SENSE AMPLIFIER

From figure it is shown that when SE is high in that particular duration whatever the data present in bitline is stored in out.

SINGLE BIT ADIABATIC SRAM



Figure 3.10 Schematic of 1Bit Adiabatic SRAM Cell

SIMULATION WAVEFORM

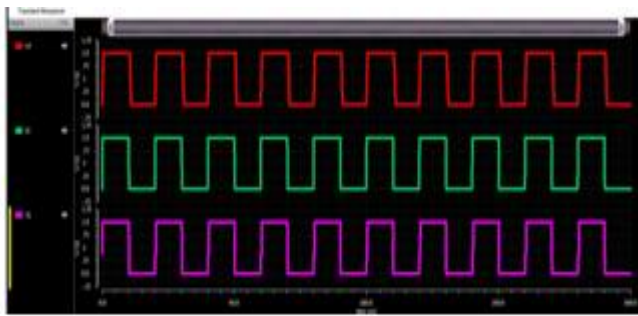


Figure 3.11 Waveform of 1 Bit Adiabatic SRAM Cell

When w_l is high in that particular duration whatever the data is present in b_l is stored as q .

INTERCONNECTION OF ADIABATIC SRAM

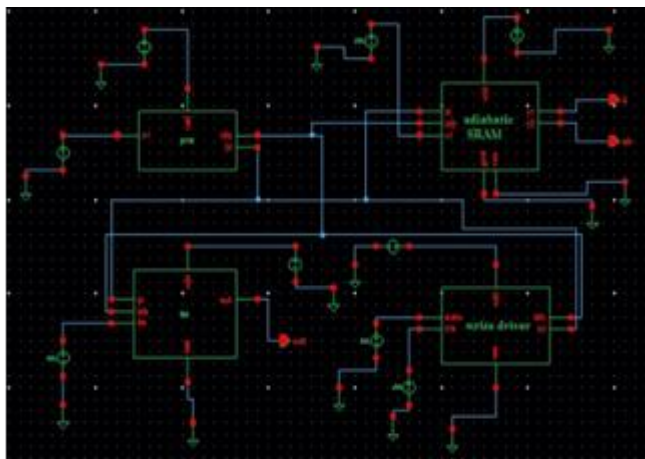


Figure 3.12 Schematic of Interconnection of Adiabatic SRAM 180nm Technology

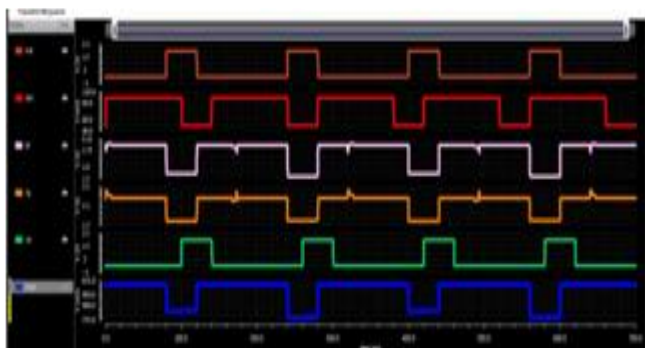


Figure 3.13 Waveforms of Interconnection of Adiabatic SRAM in 180nm 90nm Technology

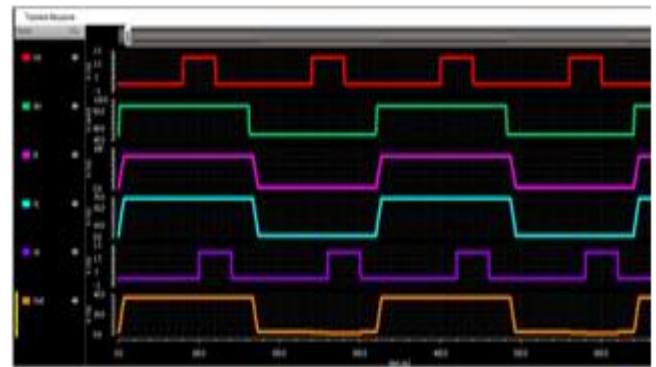


Figure 3.14 Waveforms of Interconnection of Adiabatic SRAM in 90nm

IV. CONCLUSION

The designed SRAM is 16x16 Memory array(256 bits). The peripherals are designed are pre-charge circuit, memory bit cell, write driver circuit, and Sense amplifier. Performance parameters of the design in both 90nm and 45nm technologies is performed. The suggested work is operated with analog i/p voltage of 0 to 1v, supply voltage 1v, and 7.8mW for 90nm and 685μW for 45nm power are consumed with reasonable delays.

REFERENCES

- [1] M. Durgadevi, R.Lavanya "Design of Low Power SRAM using Adiabatic Change of Word-line Voltage", International Journal of Computer applications(0975-8887), 2015.
- [2] Mr. Sunil Jadav , Mr. Vikrant , Dr. Munish Vashisath," Design and Performance Analysis of Ultra Low Power 6t SRAM Using Adiabatic Technique" International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.
- [3] Mohammad, B.S. ; Dept. of Electr. & Com-put. Eng., Khalifa Univ. of Sci., Technol. & Res., Abu Dhabi, United Arab Emirates ; Saleh, H. ; Ismail, M "Design Methodologies for Yield Enhancement and Power Efficiency in SRAM-Based SoCs", IEEE Trans. Very Large Scale Integration. (VLSI) Syst. , vol. 23, no. 10, October 2015.
- [4] Neil H. E. Weste, David Harris, Ayan Banner-je, " CMOS VLSI Design-Circuits and Systems Perspective ", 2009.
- [5] Sung-Mo Kang, Yusuf Leblebici, " CMOS Integrated Circuits- Analysis and design ", 2005.

- [6] Pavlov, Andrei and Sachdev, Mano, " CMOS SRAM Circuit Design and Parametric Test ", 2008.
- [7] McGraw-hill, " Computer Organization ", 2007.
- [8] Verma N and Chandrakasan, " 6T sub SRAM employing sense amplifier redundancy ", 2007.
- [9] J. M. Rabaey, A. Chandrakasan, and B. Ni-kolic, " Digital Integrated Circuits ", 2003.
- [10] Mr. Viplav A. Soliv, Dr. Ajay A. Gurjar, " An analytical approach to design VLSI implementation of low power , high speed SRAM cell ", 2012.
- [11] Using the basic study from the internet, tak-ing examples and studying about the designing of SRAM Cell. This study is a part from Google.