

Graphene Nanoribbon Fets with Improved I_{ON}/I_{OFF} Ratio and Subthreshold Slope

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Abstract

Recent development and heavy market demands for electronic devices suggest need of novel device material with greater efficiency and exceptional characteristics to enhance device performance. Therefore, Carbon, Carbon nanotubes (CNT) and graphene are considered as the most suitable device materials for replacing silicon material in future. Moreover, one of the most significant and fascinating device material is Graphene nanoribbon (GNR) which exhibits several exceptional electrical and mechanical characteristics and high compatibility with lithographic process on graphene sheets makes GNR a suitable candidate to replace silicon. A full quantum transport model is developed and simulated for a double gate GNR-FET device using Non Equilibrium Green's function (NEGF) approach. This paper provides physical modeling of GNR-FET and investigates the device characteristics and performance based on I_{ON}/I_{OFF} ratio and subthreshold slope parameters for GNR-FET with different high-k dielectric gate oxide materials and oxide thickness. The paper reports an I_{ON}/I_{OFF} ratio of 2.32×10^3 and subthreshold slope of 73.74.

Index Terms—scaling, CNT, graphene, GNR, NEGF, I_{ON}/I_{OFF} ratio, subthreshold slope, high-k dielectric

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I. INTRODUCTION

Graphene consists of several exceptional physical, electrical and thermal characteristics. The Graphene properties such as extreme high carrier mobility, zero bandgap and great tensile strength provide great strength towards numerous applications such as flexible sensor devices, broadband detectors and piezoelectric equipment [1]-[3]. The utilization of electronic devices and integrated circuits becomes limited while using graphene material due to the absence of bandgap in graphene with large area. Moreover, the utilization of graphene in switching applications also becomes limited as current on/off becomes complex and critical process due to absence of bandgap. The above mentioned challenges reduce utilization of graphene over silicon in these applications. Therefore, only Graphene Nanoribbon (GNR) which are graphene thin stripes can be utilized for these applications.

For the development of Nano scale devices and Nano electrochemical systems, Graphene Nanoribbon (GNR) has emerged as the most suitable device material. The electrical characteristics of Graphene Nanoribbons gain even more strength due to the presence of chirality effect, sharp edges as well as lower size factor. GNR consists of numerous exceptional mechanical, electrical, optical and thermal characteristics just like CNT. Moreover, GNR contains fascinating mechanical characteristics with high thermal

conductivity. GNR has high potential of becoming a great electricity conductor. Recent studies claim that thin Graphene Nanoribbon material shows semiconducting properties due to the presence of quantum tunnelling effect which can help in producing bandgap [4-5]. Moreover, Graphene nanoribbon (GNR) can emerge as highly compatible material for Field Effect Transistor (FETs) as GNRs are highly influenced by the external electrical fields [6]. Furthermore, GNR fabrication is segregated into two basic top-down fabrication approach and bottom-up fabrication approach. The fabrication of GNRs takes place using lithographic process on graphene sheets or with the help of unzipping Carbon Nanotubes (CNT) in top-down approach [7-8]. Satisfactory results are acquired in this approach [9-10]. However, the edges and GNR widths are not precise in this approach. Thus, Bottom-up GNR fabrication approach can be utilized to handle this type of GNR challenges [11-13]. The bottom-up approach provides chances of fabricating large-scale ribbons with similar characteristics and structures and also provides full control over GNR electronic structures. With the high influence of applied electric field, GNR bandgap between conduction and valence band can be dragged towards mid range of infrared energies from zero.

Several researchers have shown their interest in making available Graphene Nanoribbon (GNR) material for numerous switching, electronic integrated circuit applications by opening up bandgap in GNR devices. Some of the research work has

been presented in following paragraph. In [14], a hysteresis effect of Graphene Nanoribbon material is demonstrated for Field effect transistor. This work shows transmission of charge carriers in GNR devices using electric transport characteristics and opening of bandgap. In [15], a detailed study of Graphene Nanoribbon FET devices is presented considering four separate gate insulators. This work also mention about the importance of using dielectric constants. In [16], a study of performance enhancement metrics is presented for Nanoribbon FET devices. Moreover, this work also discusses about the effect of dielectric constants in GNR. In [17], a study of Nanoribbon FET devices is presented for opening up bandgap and for channel material efficiency while enhancement while maintaining high carrier mobility. In [18], a carbon based Nanoribbon FET device is introduced for providing precise methods for the transmission of charge carriers in nanoribbon devices. Based on their widths, bandgap and current on/off ratio are determined. However, practical implementation of these techniques is complex and far away.

Thus, the transmission of charge carriers in GNRs can studied by following three methods. First is classical approach, second is semi-classical approach and last is quantum mechanics based approach. The classical approach works on the principles of Newton's law like charge-collection equations [19]. However, the operation of classical approach becomes limited in case of sub-nanometer channel lengths. Moreover, semi-classical approach is also not suitable for charge carrier tunneling. Therefore, quantum mechanics based approach is the most suitable method for charge carrier tunneling for a short channel GNRFET [20, 21]. The most significant and effective method for obtaining precise bottom-up device simulation is Non-Equilibrium Green's function (NEGF). This method obtain solutions for Schrodinger equation based on quantum tunneling effect in non-equilibrium state. Furthermore, NEGF method gives information about atomistic channel details, carrier transmission scattering and contact points in the channel. The NEGF method utilizes device Hamiltonian which can be segregated into two parts such as real space NEGF formulation and mode space NEGF formulation [22]. Here, real space NEGF formulation can utilized for any geometry whereas mode space NEGF formulation divides the device simulations into group of 1D issues over a sub-band.

Furthermore, gate dielectric scaling is required for the precise scaling of channel. The scaling of state-of-art S_iO_2 gate dielectric is very challenging process due to which performance of GNRFET can get affected. However, downwards scaling of S_iO_2 gate dielectric can enhance gate leakage current and can cause oxide breakdown. Therefore, high-k dielectrics is the most suitable dielectric constant for replacing S_iO_2 gate dielectric to obtain low leakage current and great current on-off ratio. Moreover, the presence of high-k dielectrics constant can enhance device performance and output characteristics to a significant level. The utilization of high-k dielectrics constant can enhance switching speed as well as obtained drain current.

The current work formulate a complete quantum carrier transmission model which works upon NEGF formulation for a

Graphene Nanoribbon FET (GNRFET). GNRFET is formulated with a double gated high k-dielectric material to decrease leakage current as well as short channel effect. The paper also explores the different high-k dielectrics as gate oxide materials with different gate oxide thicknesses for application towards graphene FETs with an improved I_{ON}/I_{OFF} ratio and subthreshold slope.

The paper is presented in the following form. Section II describes about the NGEF formulation for the charge carrier transmission and GNRFET simulations for the modelled device. Section III, discusses about simulation outcomes link to various gate oxide dielectrics and gate oxide thicknesses while Section IV concludes the paper.

II. MODELING OF GNRFET DEVICE

A. Quantum Transport

Transport simulations which are dependent on Quantum approach is the most proficient method. In this approach, the length of device is significantly reduced which makes quantum approach more meaningful and provide outstanding outcomes. Moreover, NEGF approach is one of the most precise quantum approach which presents atomistic specifications of channel substances. Furthermore, it ensures precise outcomes and provide great understanding towards GNRFET performance for channel lengths < 10nm as well as carrier transmission take place in the medium which occurs as an impact of exposure. To get even border and minimum variations, the NEGF approach is adopted in GNRFET using mode space methodology. This mechanism ensures high throughout and computational benefits with significant simulation efficiency. A frequentative algorithm is presented in **Figure 1** & **Figure 2** to evaluate potential description with the help of electrostatic and transport solutions. Poisson's and transport equations are utilized to evaluate potential description and charge density. Then, bias current can be determined easily. The summation of hole and electron density is recognized as the total charge density of the channel.

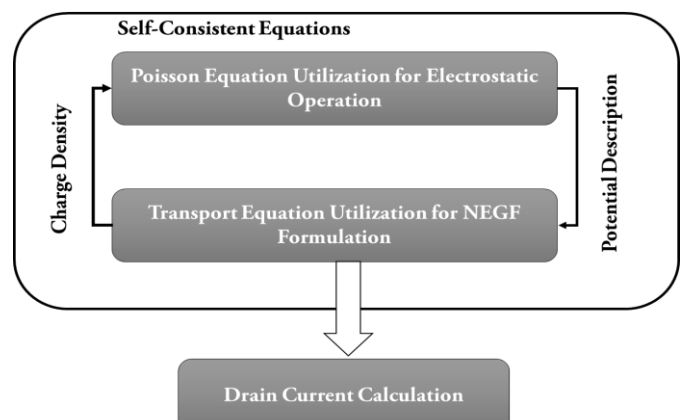


Figure 1: Self consistent electrostatic & transport computations

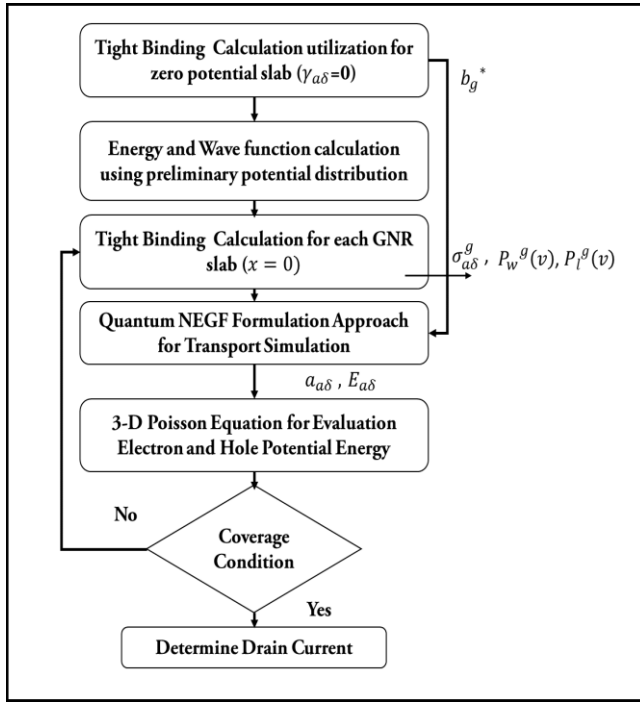


Figure 2: Iterative solution flowchart

The bias current can determined using following stages:

Stage 1: For a particular width and zero potential slab, the actual mass of bottommost sub-bands are determined with the help of tight binding (TB) calculation. This mechanism can further utilized for consecutive transport computations. The required details of consecutive transport computations for GNR sub-bands are obtained using Tight Binding computations with slab length $3a_{cc}$ and $2N_a$ atoms. The matrix components such as δ^{th} atom and λ^{th} atom inside the a^{th} slab and b^{th} slab respectively of the Hamiltonian are shown in the following equation,

$$K_{a\delta, b\lambda} = K_{a\delta, b\lambda}^0 + \rho_{a\delta, b\lambda} \gamma_{a\delta} \quad (1)$$

The one-dimensional quantum impact of the carriers expands band gap and mitigates the velocity of electrons and band recti-linearity close to Dirac point. The actual mass model is utilized to revise non-linearity of every sub-band.

$$\left[P_g(x) - \frac{P_y^g}{2} \right] \left[\frac{1}{2} + \frac{P_g(x)}{P_y^g} \right] = \frac{z^2 x^2}{2b_g^*} \quad (2)$$

Stage 2: The energies and the wave-function are determined using preliminary potential distribution for a sub-band which can termed as longitudinal direction function. This can achieved using successive tight-binding computation for each GNR slab only at $x = 0$. Stage 3: For a particular sub-band parameters such as Green's function, exposure self-energies and their

respective level expansion function and Hamiltonian matrix are obtained. The Hamiltonian matrix obtained using the transport simulations which are dependent on Quantum NEGF formulation approach are same as obtained in the case of Tight Binding. The actual mass model which is dependent on positional energy is utilized for obtaining non-parabolic band structure and presented by following equations,

$$b_g(v, P) = \begin{cases} b_g^* \left[1 + \frac{P - P_l^g(v)}{P_y^g(v)} \right] & \text{if } P > P_j^g(v) \\ b_g^* \left[1 + \frac{P_w^g(v) - P}{P_y^g(v)} \right] & \text{if } P < P_j^g(v) \end{cases} \quad (3)$$

The delayed Green's function is determined based on the evaluated Hamiltonian.

$$H_g(P) = \left[PN - K_g - \sum_d^g - \sum_s^g \right]^{-1} \quad (4)$$

The GNR channel DOS (Density of States) contains acute levels at the least energies of sub-bands due to quantum effect. This happens before the GNR channel become linked with source and drain exposure points. Simultaneously, at source and drain exposure points a relentless distribution of states takes place. Moreover, relentless state outcomes and discretized coupling in a state spread from channel to exposure points and exposure points to channel take place for certain energy range. The level expansion measures can determined as following,

$$\begin{aligned} \chi_d^g &= i(\sum_d^g - \sum_d^{g+}) \\ \chi_s^g &= i(\sum_s^g - \sum_s^{g+}) \end{aligned} \quad (5)$$

Stage 4: Source and drain correlation functions and their respective hole and electron numbers are computed as follows,

$$H_g^<(P) = H_g(P) \left[\sum_d^{g<} (P) + \sum_s^{g<} (P) \right] H_g^+(P) \quad (6)$$

$$H_g^>(P) = H_g(P) \left[\sum_d^{g>} (P) + \sum_s^{g>} (P) \right] H_g^+(P)$$

$$\sum_{T/S}^{g<} (P) = j \chi_{T/S}^g \psi_{T/S}(P) \quad (7)$$

$$\sum_{T/S}^{g>} (P) = j \chi_{T/S}^g [1 - \psi_{T/S}(P)] \quad (8)$$

$$\psi_{T/S}(P) = [1 + \exp\left(\frac{P - P_{Q_{T/S}}}{X_G R}\right)]^{-1} \quad (9)$$

At (a, δ) atom position the hole and electron number is determined using following equations,

$$a_{a\delta} = -2j \int_{P_j(a,\delta)}^{\infty} (2\pi)^{-1} H^<(a, \delta; a, \delta; P) dP \quad (10)$$

$$E_{a\delta} = 2j \int_{-\infty}^{P_j(a,\delta)} (2\pi)^{-1} H^>(a, \delta; a, \delta; P) dP \quad (11)$$

Here, $P_j(a, \delta)$ represents the fermi level of intrinsic type and the charge of electron and hole is evaluated using above equations. Besides, Equation (10) and Equation (11) further composed into following equation,

$$a_{a\delta} = -2j \sum_g [|\sigma_{a\delta}^g|^2 \int_{P_j^g(v)}^{\infty} (2\pi)^{-1} H_g^<(a, a; P) dP] \quad (12)$$

$$E_{a\delta} = 2j \sum_g [|\sigma_{a\delta}^g|^2 \int_{-\infty}^{P_j^g(v)} (2\pi)^{-1} H_g^>(a, a; P) dP] \quad (13)$$

Stage 5: The Poisson Equation is utilized for evaluating novel potential energy for the hole and electron numbers. Then, the 3-dimensional Poisson equation is given by,

$$\nabla \cdot [\xi(\vec{r}) \nabla \gamma_{a\delta}(\vec{r})] = f F(\vec{r}) \quad (14)$$

Stage 6: The coverage state is given by following equation,

$$|\gamma_{a\delta} - \gamma_{a\delta}^{old}| = \varrho \quad (15)$$

Stage 7: The Transmission Function $R(P)$ is utilized for drain current calculation by following equation,

$$N_{ST} = \frac{f^2}{z} \int_{-\infty}^{\infty} \sum_g \frac{4}{f} \Re \{ \text{Trace}[K(a, a+1) H^<(a+1, a; P)] dP \} \quad (16)$$

Where, $\Re$ represents the real part and Trace represents index and z denotes plank constant.

$$N_{ST} = \frac{f^2}{z} \int_{-\infty}^{\infty} \sum_g \frac{4}{f} \Re \{ K_g(a, a+1; P) H_g^<(a, a+1; P) dP \} \quad (17)$$

Moreover, the equation (17) can be decomposed into following form,

$$N_{ST} = \frac{2f}{z} \int_{-\infty}^{\infty} R(P) [\psi_d(P) - \psi_s(P)] dP \quad (18)$$

$$R_g(P) = \text{Trace}[\chi_d^g H_g \chi_s^g H_g^+] \quad (19)$$

B. GNRFET Structure

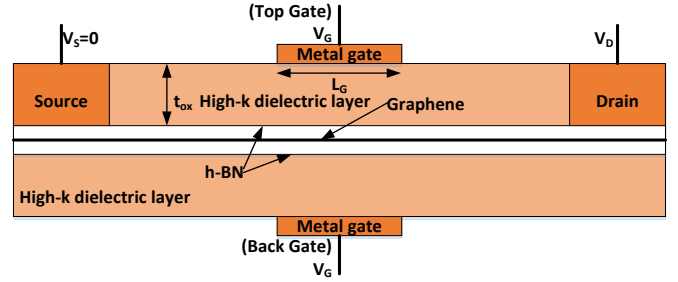


Figure 3: Double gate GNRFET structure

The double gate GNRFET structure is shown in **Figure 3**. A sandwich structure with two insulator layers sandwiching the GNR layer is simulated. The device has a double metal gate topology which provides maximum gate electrostatic control over the GNR channel. A buffer layer of h-BN layer above the GNR layer reduces the trapped impurities. The proposed structure has a high-k dielectric layer and h-BN layer. The combined structure gives an improved effective oxide thickness (EOT). The length of intrinsic GNR channel is 7.5nm and the symmetric regions of GNR channel are heavily doped with concentration of 0.01 n-type dopants per carbon atom and connected to metallic contacts. The dielectric layer thickness is varied for parametric studies. Also, the device is simulated for two different high-k dielectrics HfO_2 and TiO_2 with different dielectric thicknesses. The results are presented in Section III.

III. SIMULATION & RESULTS

The device described in Section II is simulated to obtain drain current under different bias conditions. NEGF formulation as described in **Figure 2** and **Figure 3** is used for full quantum transport modelling in MATLAB. The device is simulated to obtain drain current characteristics for different gate oxide thicknesses of 1nm, 2.5nm, 5nm, 7.5nm and 10nm. It was demonstrated in [23] that GNRFET with GNR index $(3p+1,0)$ gives better performance than the $(3p,0)$. In this paper, GNR index of $(13,0)$ belonging to $(3p+1,0)$ family is selected for simulations.

The characteristics simulated and studied are the drain current with respect to varying drain and gate biases, device trans-conductance, I_{ON}/I_{OFF} ratio and the subthreshold slope. While the drain current characteristics gives insight into the basic device performance, the last two parameters present the quality of device operation as a switch. The I_{ON}/I_{OFF} ratio and the subthreshold slope are important characteristics for a device

operated as a switch wherein the OFF state current is a concern. These two parameters are also important from the perspective of low power devices where in again the OFF state current plays an important role in deciding the power consumption of the device.

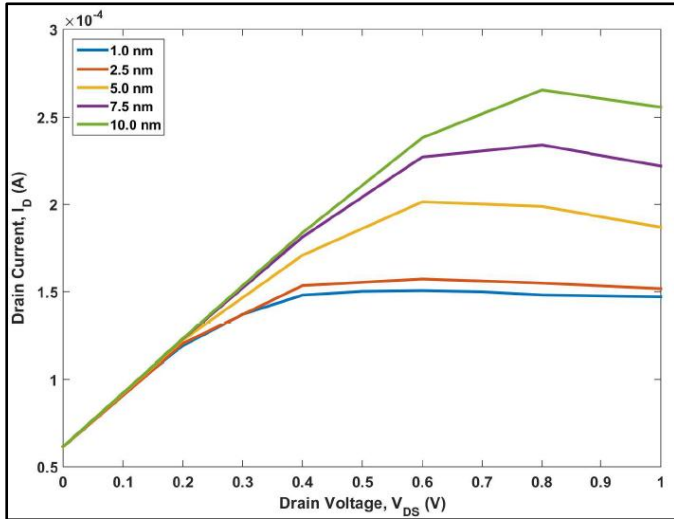


Figure 4: I_D - V_{DS} characteristics with HfO_2 as the gate oxide

Figure 4 presents the I_D - V_{DS} characteristics of GNR-FET with HfO_2 as the dielectric for different dielectric thicknesses. The plot shows a decrease in drain current with decrease in dielectric thickness. Also, the slope of drain current plot w.r.t drain source bias increases with the dielectric thickness. The increasing slope depicts drain induced barrier lowering in the device.

Figure 5 shows the drain current with respect to gate source bias. The plot shows an improved OFF state operation for lower oxide layer thickness. The threshold voltage for the device can be approximated from the trans-conductance plot in Figure 6 which shows a preferred threshold voltage of around 0.4V for dielectric thickness of 1nm.

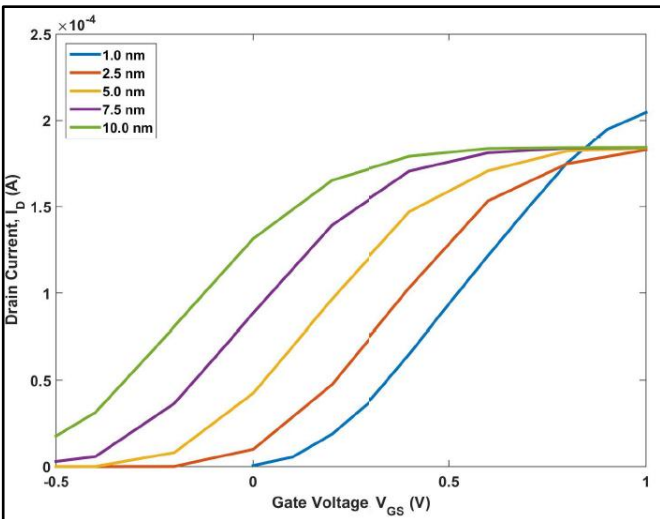


Figure 5: I_D - V_{GS} characteristics with HfO_2 as the gate oxide

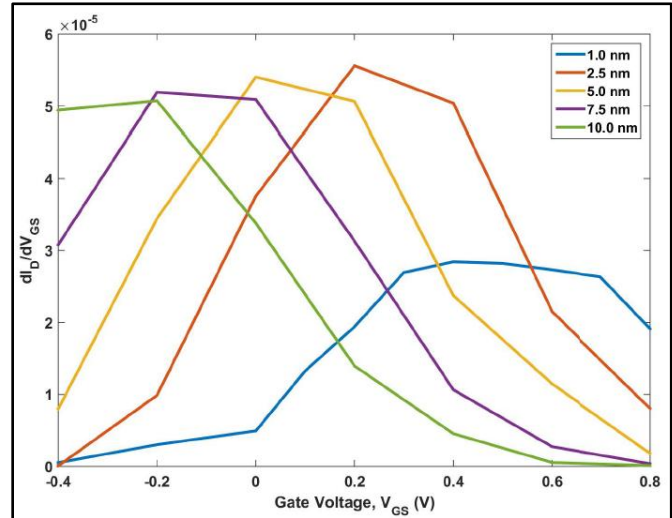


Figure 6: Trans-conductance with HfO_2 as the gate oxide

Similar characteristics are presented in Figure 7-Figure 9 for TiO_2 as the gate dielectric material. There is a reduced drain current in the I_D - V_{DS} characteristics. However, for the I_D - V_{GS} the drain currents are comparable for the two dielectric oxide materials. Moreover, the performance across the dielectric oxide thickness is more uniform for TiO_2 than HfO_2 with comparable threshold voltages. Figure 10 shows the subthreshold slope for the device.

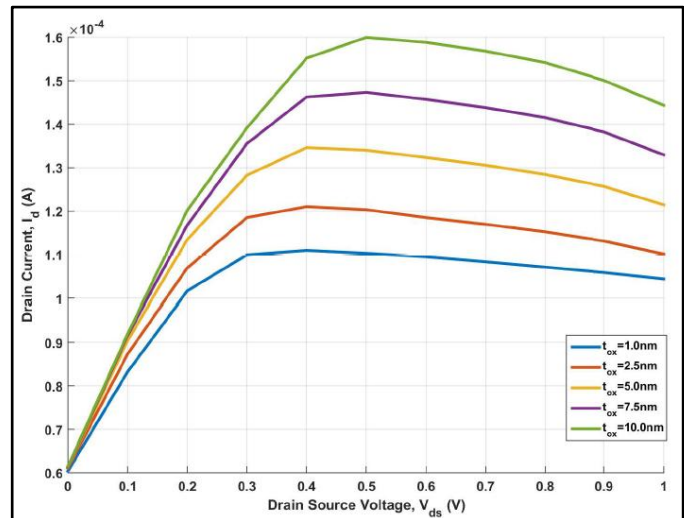


Figure 7: I_D - V_{DS} characteristics with TiO_2 as the gate oxide

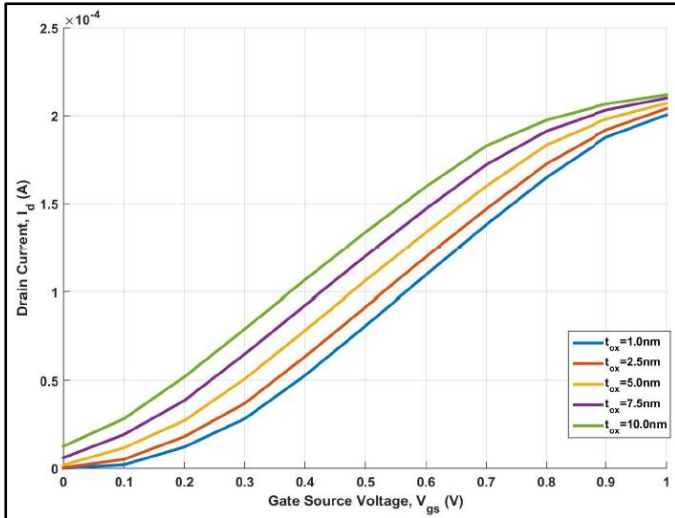


Figure 8: I_D - V_{GS} characteristics with TiO_2 as the gate oxide

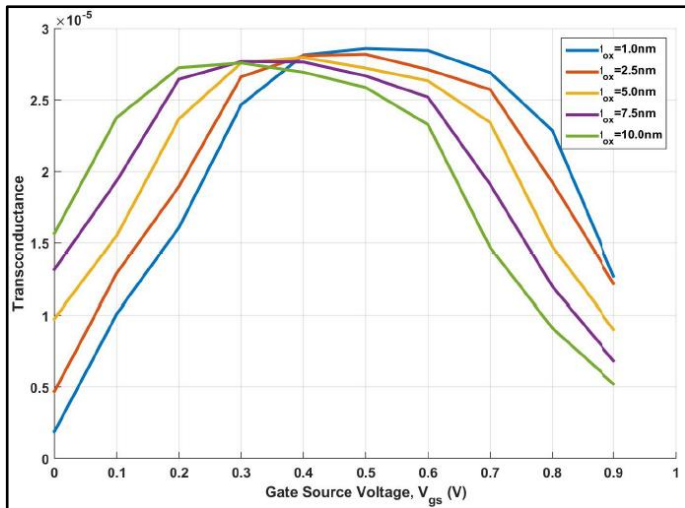


Figure 9: Transconductance for TiO_2 as the gate oxide

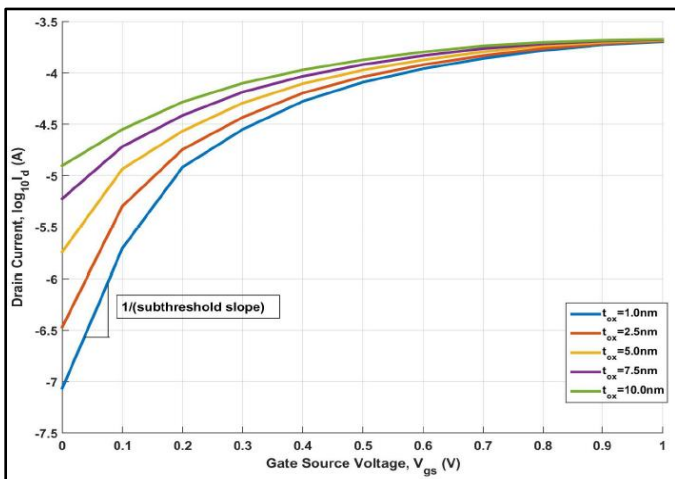


Figure 10: Subthreshold slope for TiO_2 as the gate oxide

The I_{ON}/I_{OFF} ratios are compared in TABLE I for the different variations studied in this paper. It is observed that the device with TiO_2 dielectric oxide gives a better and improved I_{ON}/I_{OFF}

ratios as well as subthreshold slope. This can be attributed to the higher dielectric constant of TiO_2 as compared to HfO_2 . Also a thinner gate oxide gives better I_{ON}/I_{OFF} performance and subthreshold slope.

TABLE I: Performance comparison for different gate oxide thicknesses and gate dielectric materials

t_{ox} (nm)	I_{on}/I_{off}		Subthreshold slope (mV/dec)	
	TiO_2	HfO_2	TiO_2	HfO_2
1nm	2.32×10^3	3.74×10^2	73.74	100.1
2.5nm	597.1	1.84	85.6	147.06
5nm	114	4.33	124.4	280.89
7.5nm	35.2	2.08	197.23	507.61
10nm	17.1	1.40	282.486	1010.1

A comparison with similar works across available literature is presented in TABLE II. The present works reports an overall improved performance in terms of I_{ON}/I_{OFF} performance and subthreshold slope.

TABLE II: Performance comparison with other works

Channel material	I_{on}/I_{off}	Subthresh old slope (mV/dec)	Ref
Si Fin	1×10^3	125	[24]
MoS ₂ with sub 10nm channel	1×10^7	120	[25]
HP Logic	1.35×10^4	-	[26]
SNM (double gate)	1.2×10^4	74	[24]
CNT	1×10^4	94	[27]
Grpahene nano ribbon	2.32×10^3	73.74	This work

IV. CONCLUSION

G NRFET device was simulated with different dielectric oxide materials and dielectric oxide thicknesses. The device characteristics are presented and it is concluded that TiO_2 high-k dielectric with a thinner gate oxide gives an improved performance as compared to HfO_2 .

The results are compared with other works reported in the literature and improved I_{ON}/I_{OFF} ratio of 2.32×10^3 and subthreshold slope of 73.74 is obtained.

REFERENCES

- [1] A. K. Geim and K. S. Novosolov, "The rise of graphene," Nature Mater., vol. 6, no. 3, pp. 183_191, 2007.

- [2] R. C. Ordonez, C. K. Hayashi, C. M. Torres, N. Hafner, J. R. Adleman, N. M. Acosta, J. Melcher, N. M. Kamin, and D. Garmire, "Conformal liquid-metal electrodes for flexible graphene device interconnects," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 4018-4023, Oct. 2016.
- [3] J. Zhao, G.-Y. Zhang, and D.-X. Shi, "Review of graphene-based strain sensors," *Chin. Phys. B*, vol. 22, no. 5, May 2013, Art. no. 057701
- [4] A.D. Zdetsis and E. Economou *Carbon*, 2017, 116, 422
- [5] Y. Son, M.L. Cohen and S.G. Louie *Phys.Rev. Lett.*, 2006, 97, 216803
- [6] A. Nazari, R.B. Dos Santos, FdB. Mota, R. Rivelino and G.K. Guerorgiv *J.Phys.Chem.C* 2007, 121, 26125-26132
- [7] D.V. Kosynkin, A.L. Higginbotham, A. Sinitskii, J.R. Lomeda, A. Dimiev, B.K. Price and J.M Tour *Nature*, 2009, 458, 872.
- [8] M.Y. Han, B. Ozyilmaz, Y. Zhang and P. Kim *Phys.Rev. Lett.*, 2007, 98, 206805
- [9] P. Jangid, D. Pathan and A. Kottantharayil *Carbon*, 2018, 132 65.
- [10] W.S. Hwang et al. *APL Mater.*, 2015, 3, 011101
- [11] E. A. Narita, X.Y. Wang, X. Feng and K. Müllen *Chem.Soc. Rev.*, 2015, 44, 6616.
- [12] L. Talirz, P. Ruffieux and R. Fasel *Adv. Mater.*, 2016, 28, 6222.
- [13] H. Sakaguchi, Y. Kawagoe, Y. Hirano, T. Iruka, M. Yano and T.Nakae *Adv. Mater.*, 2014, 26, 4134
- [14] A. Tries, N.Richter, Z. Chen, A. Narita, K. Muellen, H. Wang, M. Bonn and M. Kläui, *Phys. Chem. Chem. Phys.*, 2020, DOI: 10.1039/D0CP00298D.
- [15] H. Shamloo, A. Nazari, R. Faez and S. Haji-Nasiri, "A Functional Study of a Bilayer Graphene Nanoribbon FET With Four Different Gate Insulators," in *IEEE Transactions on Nanotechnology*, vol. 18, pp. 890-895, 2019, doi: 10.1109/TNANO.2019.2936521.
- [16] N. K. Singh and M. Sahoo, "Investigation on the Effect of Gate Dielectric and Other Device Parameters on Digital Performance of Silicene Nanoribbon Tunnel FET," in *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2966-2973, July 2020, doi: 10.1109/TED.2020.2992016.
- [17] M. A. Kharadi, G. F. A. Malik, K. A. Shah and F. A. Khanday, "Sub-10-nm Silicene Nanoribbon Field Effect Transistor," in *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4976-4981, Nov. 2019, doi: 10.1109/TED.2019.2942396.
- [18] T. Zhang, H. Zeng, D. Ding and R. S. Chen, "A Numerical Simulation of C3N Nanoribbon-Based Field-Effect Transistors," in *IEEE Transactions on Electron Devices*, vol. 66, no. 2, pp. 1087-1091, Feb. 2019, doi: 10.1109/TED.2018.2883298.
- [19] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors", *Nature Nanotechnology*, vol. 3, no. 11, pp. 654-659, 2008.
- [20] Y. Ouyang, Y. Yoon, and J. Guo, "Scaling behaviors of graphene nanoribbon FETs: A three-dimensional quantum simulation study", *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2223-2231, 2007.
- [21] X. Guan, M. Zhang, Q. Liu, and Z. Yu, "Simulation investigation of double-gate CNRMOSFETs with a fully self-consistent NEGF and TB method", *IEDM Tech. Dig.*, vol. 761, p. 764, 2007.
- [22] G. Liang, N. Neophytou, M. S. Lundstrom, and D. E. Nikonov, "Ballistic graphene nanoribbon metal-oxide-semiconductor field-effect transistors: A full real-space quantum transport simulation", *Journal of Applied Physics*, vol. 102, no. 5, p. 054307, 2007.
- [23] Nanda B.S Puttaswamy P.S., "Physical Modeling of Graphene Nanoribbon FET- Quantum Mechanics", *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*, Volume-9 Issue-3, January 2020, pp. 2278-3075
- [24] F. Pan et al., "Silicene nanomesh," *Sci. Rep.*, vol. 5, Mar. 2015, Art. no. 9075. doi: 10.1038/srep09075.
- [25] A. Nourbakhsh et al., "Mos2 field-effect transistor with sub-10 nm channel length," *Nano Lett.*, vol. 16, no. 12, pp. 7798-7806, Dec. 2016. doi: 10.1021/acs.nanolett.6b03999.
- [26] (2014). *ITRS-The International Technology Roadmap for Semiconductors*. [Online]. Available: <http://www.itrs.net>
- [27] B. Doris et al., "Device design considerations for ultra-thin SOI MOSFETs," in *IEDM Tech. Dig.*, Dec. 2003, pp. 27.3.1-27.3.4. doi: 10.1109/IEDM.2003.1269360.