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Design of 8TSram Using Finfet Technology

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Abstract

Retrieving the data is the major aspect of concern in CMOS technology. At present lower power consumption is the primary objective. The lower power consumption the SRAM cells will be used in the near future extensively. The existing models do not give stability in reading operation because of which a correct logic decision at the output cannot be made. In this paper SRAM cell is designed using FinFETtechnology and is compared with existing CMOS 45nm technology, and a new SRAM cell structure is proposed which enhances the read stability and write stability with reduction in noise. The transient analysis is done for both CMOS 45nm and FinFET technology based SRAM cell. This proposed model is designed with 8 transistors where 6 transistors are used for data writing and another two are for data reading. The present design increases the read stability.

Keywords: *stability,8T SRAM,CMOS, FinFET.*

I. INTRODUCTION

The major and key area in scaling down the CMOS technology belongs to SRAM memory because of its high demand [7]. Conventional SRAM cell uses 6 transistors for both reading and writing operations. It has an advantage of less area [5]. Here bit-line acts as an In-Out line which means reading and writing are done through single bit-line [4].Though logic can be made stable it requires extra circuitry like sense amplifier. This results in unstable read output. Even an 8T SRAM cell with a single BL is designed [1].But the logic cannot be restored to expected level. It can be achieved in different ways [3]. While writing bit-line charges and while reading it requires to get discharged. This leads to data retention error. In order to avoid this, separate lines are used for reading and writing operations.Whenever respective lines are activated, respective operations are done without any interference. Existing SRAM cells use 8T, 9T configurations for this purpose. As the length of channel decreases, the operation speed and power consumption decreases. Here the transient analysis is done on CMOS-180, CMOS 45nmtechnologies. The existed circuit proposed in [2] is simulated and transient analysis is done on the circuit. The existed circuit uses 8 transistors. The central idea is that the value which is stored inside the RAM cell is sent through different transistors to get the read output. This is a one bit SRAM cell which can be used to read or write only one bit at a time. Theproposed circuit in this paper uses 8 transistors. The results obtained with the existed circuits are compared to the proposed circuit. It is observed that the existed circuit has 900mv while reading logic “1”. This problem is reduced to a large extent when the transient analysis is done for the proposed circuit with similar specifications of length and width. This circuit overcomes the problem of changing the width specification. For similar width the expected results can be obtained by using proposed circuitry. Cadence virtuoso is the Tool used for simulation.

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II. EXISTED DESIGN

In 6T SRAM [9]one of the difficulties is that during the read operation, logic 0 stored can be override by logic 1 when the voltage at node V1 arrives at Vth of nMOS N1 to pull node V2 down to logic 0 and even pulls up node V1 to logic 1because of positive feedback. This results in unexpected result of read operation when thecell changes state [6].The existed model of 8T SRAM consists of 6 transistors for write operation and the other two for read operation.In this design two nMOS transistors are connected in series to perform the read operation.

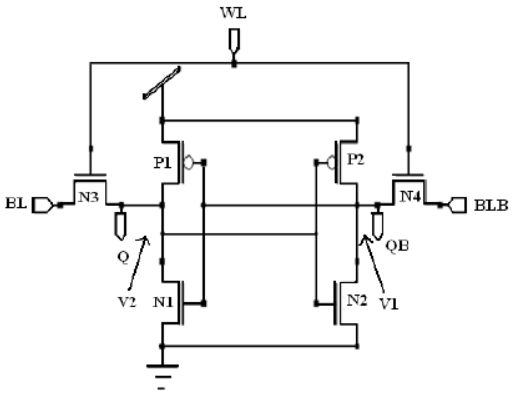

Figure 1: 6T SRAM cell

The RWL is connected to the gate of M7 transistor which is used to enable the read operation. One of the drawbacks of this circuit is that if there is disturbance caused in the voltage stored in Qb, the same would be replicated at the output which is on the RBL.

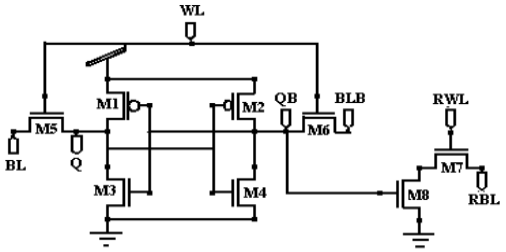

Figure 2: 8T SRAM cell

Circuit cannot restore the logic exactly as the input. Though circuit can restore to some extent by changing the width of the transistors, it would affect the total area which tends to increase further. When the existing circuitry is designed and executed transient analysis,the strong logic 0 and logic 1 could not achieved as outputs, while reading the bits from memory. In this paper a new 8T SRAM design is proposed which overcomes the mentioned drawbacks.

III. PROPOSED DESIGN

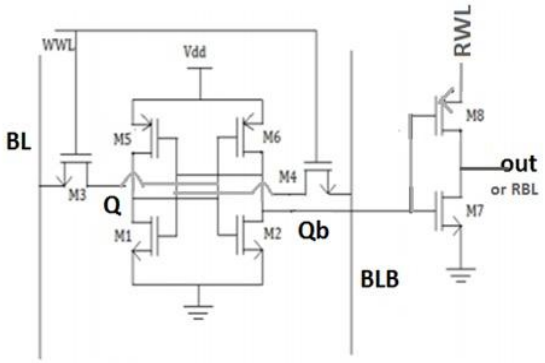

Figure 3: Proposed 8T SRAM

The proposed SRAM cell uses 6 Transistors which are involved in write operation on to the SRAM cell. Out of which M3 and M4 are called access transistors and rest of the four M1, M2, M5 and M6 transistors are used for storing the value. M1 and M5 form an inverter 1. M2 and M6 form another inverter 2. These inverters are connected back to back. The access transistors are activated when WWL is high. The Data is given through BL. The data enters through M3 passes through inverter 2 and the inverted output is given as an input to inverter 1 and the obtained value is stored as Q. This is how the write operation is performed. When it comes to the read operation, the value which is stored at Qb is passed through an inverter composed of M7 and M8, the inverted output is taken as an output. This inverter works only when RWL is high. That means whenever read line is made to high the stored value Q is read.

IV. PROPOSED DESIGN RESULTS

The BL line starts from logic 0.After 20ns the WWL is enabled because of which the bits present on BL are written into Q i.e. they are stored in it. The bits present in Q are written onto to the RBL upon enabling the RWL (read word line).

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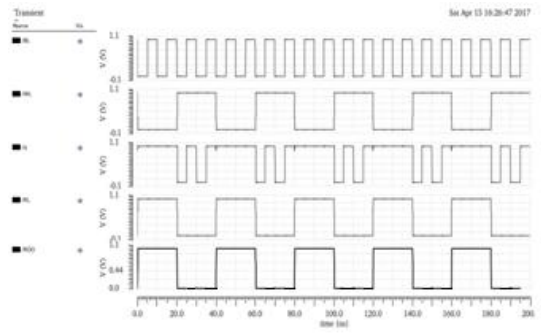

Figure 4: Proposed 8T SRAM Result

In the proposed CMOS 45 nm SRAM is observed that logic 1 is read as 1V and logic 0 is nearly in the order of nano volts which can be considered to logic 0. When compared with the existed design the logic restoration is observed.

The read and write operations are more stabilized in SRAM designed with FinFET.

FinFET

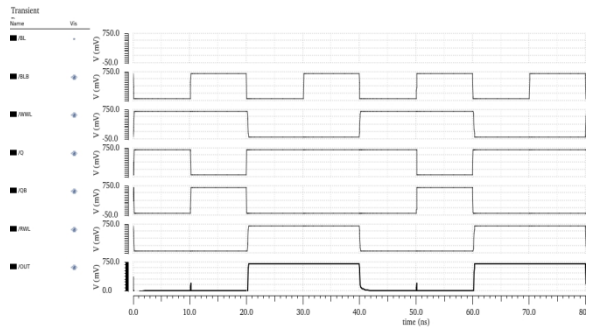

Figure 5: Proposed 8T SRAM cell Result

The time delays for both read and write operations for the proposed 8T SRAM cell in CMOS 180nm, CMOS 45nm, FinFET are calculated and are shown below.

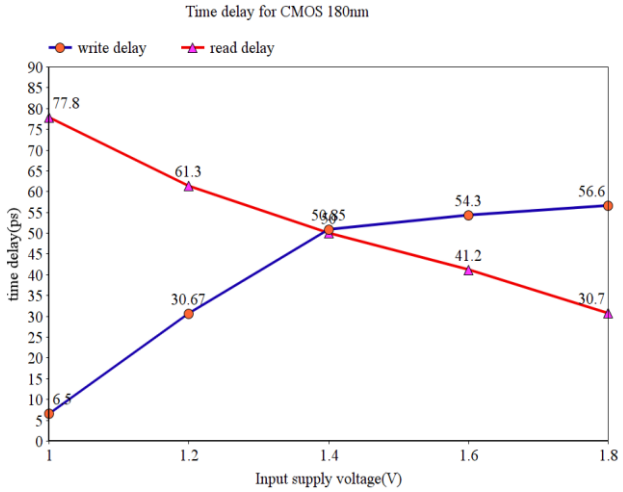

Figure 6: Time delay for CMOS 180nm

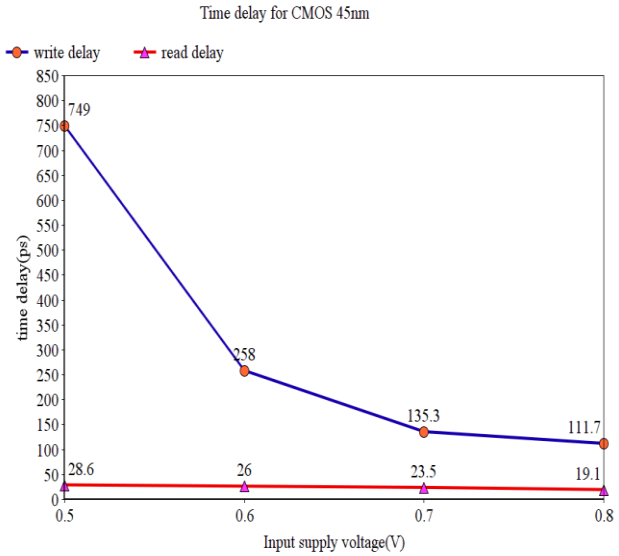

Figure 7: Time delay for CMOS 45nm

The delays have been reduced when compared to existed 8T SRAM cell [8][10]. Figure 8:Time delay forFinFET.

Leakage power for various technologies of 8T SRAM are found from which it can be observed that FinFET has less leakage power when compared to all other technologies, shown in Table I

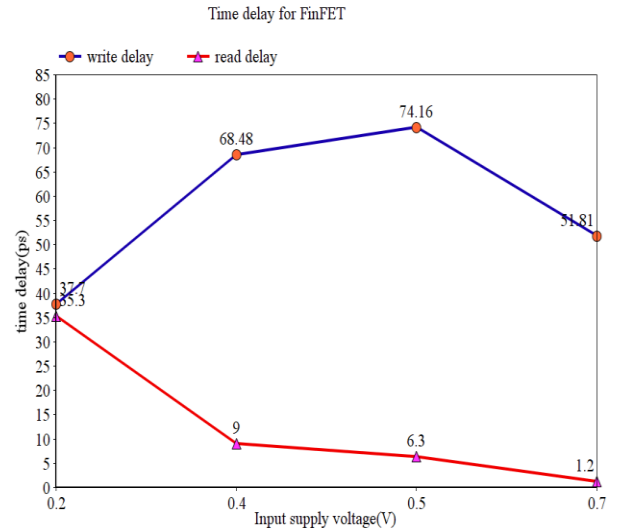

Figure 8: Time delay for FinFET

Table I

Different technologies	CMOS 180nm	CMOS 45nm	FinFET
Leakage power(µw)	984µw	3.67µw	1.036µw

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PERFORMANCE COMPARISON BETWEEN DIFFERENT SRAM CELLSAND PROPOSED 8T CELL

Table II

Parameter Name	6T SRAM	8T SRAM	Proposed 8T SRAM [FinFET](0.5 v)
Leakage power[10]	27.26µw	67µw	1.036µw
Read delay[11]	72.82ps	77.72ps	6.3ps
Write delay[11]	8.9ps	45.47ps	74.16ps

V. CONCLUSION

Design of 8T SRAM cell using CMOS 45nm and FinFET technology has been done by showing the recovery of stable outputs on write and read operations. The logic 0 and logic 1 are stabilized during read operation which was not in the case of existed design and even delays have been calculated and compared with the existing models.The leakage power for this proposed circuitry has been found for the CMOS and FinFET technologies.

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