TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 3163 - 3167

Implementation Of High Speed Built In Self-Test Architecture For Testable Uart

M. Radha Rani, ECE Department, Swarnandhra College of Engineering and Technology, Narsapur, Andhra Pradesh, India.
FazalNoorbasha, ECE Department, KL University, Guntur, Andhra Pradesh, India.

Article Info
Volume 82
Page Number: 3163 - 3167
Publication Issue:
January-February 2020

Article History

Article Received: *14 March 2019*
Revised: *27 May 2019*
Accepted: *16 October 2019*
Publication: *19 January 2020*

Abstract
Abstract:This paper presents the implementation of Testable Universal Asynchronous Receiver Transmitter (UART). High speed test structure is described for testing UART. Built in Self-Test (BIST) is the most commonly used test structure for testing UART. Because of the complex test structures, the test time is very much high. Which can be reduced by pipelined test structures. The increasing growth of sub-micron technology has resulted in the difficulty of testing. Day by day VLSI circuits becoming more and more complex, thereby test circuits needed also becoming more and more complex. Built in Self-Test (BIST) is a technique that allows a circuit to test itself. Integrated Circuit manufacturing process are becoming more and more complex day by day. The design engineers and the test engineers collectively work together to achieve a reliable VLSI chip. Effective test techniques are needed to manufacture a reliable VLSI chip. This paper describes the design of a UART chip which tests itself. Testability is added to the UART circuit with the help of BIST technique. Generally, BIST structure is a complex one. In order to get high speed test process, pipelined BIST architecture is implemented. Entire system is described with HDL language and is implemented on Spartan 3 Field Programmable Gate Array (FPGA).

Keywords: *Built in Self-Test (BIST), Field Programmable Gate Array (FPGA), Testability, Universal Asynchronous Receiver Transmitter (UART).*

I. INTRODUCTION

Gathering procedures are incredibly capricious, inciting creators to consider testability an excitement to ensure the enduring quality and comfort of each in their orchestrated circuits. One of the most exceptional comprehended test systems utilized is Built-in-Self-Test (BIST). A BIST understood one of a kind get transmit (UART) has most fundamental goals regardless to satisfy the favored testability necessities moreover to make the base cost with the crazy principle speaking all around execution use. UART has been one of the most crucial input/output gadget for many years and stays extensively used.

This paper specially makes a speciality of the layout of UART with embedded BIST capability and on the problems of Very Large Scale Integrated (VLSI) sorting out accompanied with the aid of the conduct of UART circuit the usage of Very High-Speed Integrated Hardware Description Language (VHDL). Although BIST strategies have become greater common in organisation, the greater BIST circuit that allows you to boom the hardware overhead will boom layout time and basic overall performance degradation is frequently said because of the truth the motive for the restrained use of BIST. In the implementation segment, the BIST method can be included into the UART format earlier than the overall format is synthesized with the resource of reconfiguring the existing layout to match testability requirements. Today's extensively blanketed multi-layer boards with best-pitch ICs are absolutely now not feasible to be accessed bodily for trying out. Traditional board take a look at

January - February 2020
ISSN: 0193 - 4120 Page No. 3163 - 3167

techniques which include useful check, handiest accesses the board's number one I/O's, offering restricted insurance and bad diagnostics for board-network fault. In circuit trying out, any other conventional check approach works by using physically having access to each wire at the board via highly-priced "mattress of nails" probes and testers. To identify dependable testing techniques which will reduce the cost of test equipment, are search to verify each VLSI testing problems has been conducted.

II.UART DESCRIPTION

Serial communique is the method of sending facts and receiving one bit of information at one time sequentially via a communications channel or laptop bus. On the alternative hand, parallel communications is a method wherein all the bits of each symbol are sent together. In preferred, serial communique is used for all long communications and most laptop networks in which it is impractical to apply parallel communications due to the value of cable and synchronization. Nowadays computer buses or community communication the use of serial communications have become extra commonplace as stepped forward era permits them to switch records at better speeds..

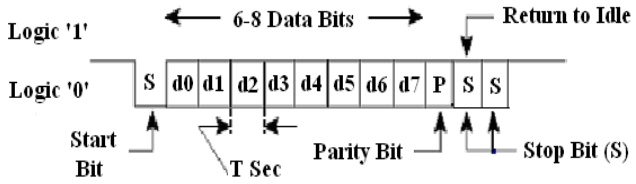

Fig.1 UART Data frame format

Universal asynchronous receive transmit (UART) is an asynchronous serial Receiver/transmitter. It is a piece of pc hardware that usually applied in PC serial port to translate records among parallel and serial interfaces. The UART takes bytes of statistics and transmits the character bits in a sequential fashion. At the receiving element, UART re-assembles the bits into whole bytes.

Asynchronous transmission permits facts to be transmitted without having to send a clock signal to the receiver. Thus, the sender and receiver need to agree on timing parameters in advance and unique bits are delivered to every word, this is used to synchronize the Sending and receiving gadgets.In significant, UART includes of two primary block, the transmitter and receiver block.The transmitter sends a byte of facts little by little serially out from UART at the same time as UART receiver gets the serial in information little by little and converts them right right into a byte of records..

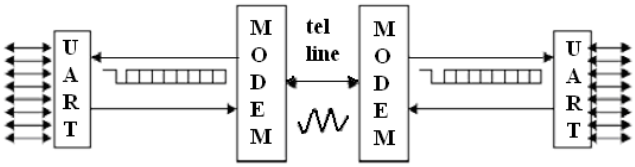

Fig.2 Serial data transmission system

UART starts offevolved the records transmission with the aid of setting forward a bit referred to as the "Start Bit" to the begin of every data This is to be transmitted. On the opportunity, UART the receiver will want to pattern the not unusual enjoy price that being obtained at about halfway thru the length assigned to each bit to decide if it's far common sense 1 or right judgment 0.

When a byte of data has been despatched, the transmitter can also additionally additionally moreover upload a "Parity Bit".The receiver to carry out easy errors checking may also use the Parity Bit.In this mission, parity bit is not being finished.After this, a "Stop Bit" is despatched through using the usage of the transmitter to signify the transmitter has finished the information transmission. If a few one-of-a-type byte of records is to be transmitted, the Start Bit for the new bits of data may be sent as energetic in context on reality the Stop Bit for the past word has been sent.

III.BUILT IN SELF TEST

A pushed contraption is looked into and saw each and every through it lifetime on severa occasions. It will lead in doubt be basic to have abundant and incredibly over the top flaw assurance giving it a shot. One normal and obviously utilized in

January - February 2020
ISSN: 0193 - 4120 Page No. 3163 - 3167

semiconductor experience for IC chip giving a shot is to guarantee this is to show take a gander at one of beyond what many would consider possible and by virtue of this Will make as self-test.A contraption coordinated without a checked research approach which covering all stages from the whole device to included substances is being depicted as chip-mind blowing and gadget ungraceful. A true blue sorted out Built-In-Self-Test (BIST) is fit for offset the charge of brought test gear on a comparative time as at the identical time making sure the reliability, testability and decreases safety cost.

Figure three shows the BIST gadget hierarchy for the 3 diploma of packaging it truly is the device stage, board degree and chip degree.The tool consists of several PCB's (or boards). Each of the PCB has a couple chips.The device Test Controller can prompt self-ask pretty much at the same time on all PCB's.Each Test Controller on each PCB weight up can begin individual test on an enormous bit of the chips at the board.The chip Test Controller runs oneself check at the chip and transmits the stop quit last thing out to the heap up Test Controller. The board Test Controller gathers check results from all chips at the PCB and sends the outcomes to the gadget Test Controller.The machine Test Controller uses all of those consequences to determine if the chips and board are defective.

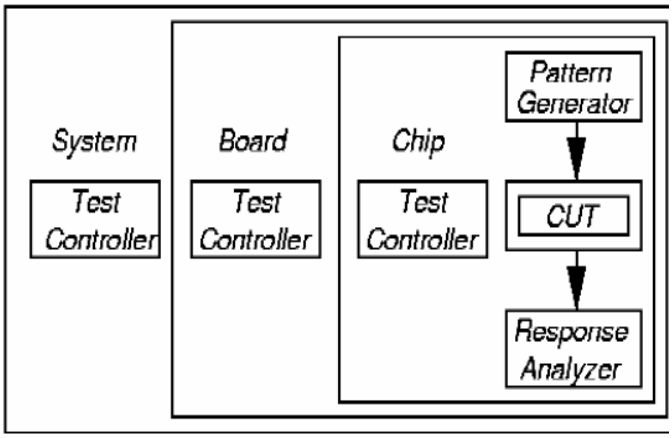

Fig.3 BIST hierarchy

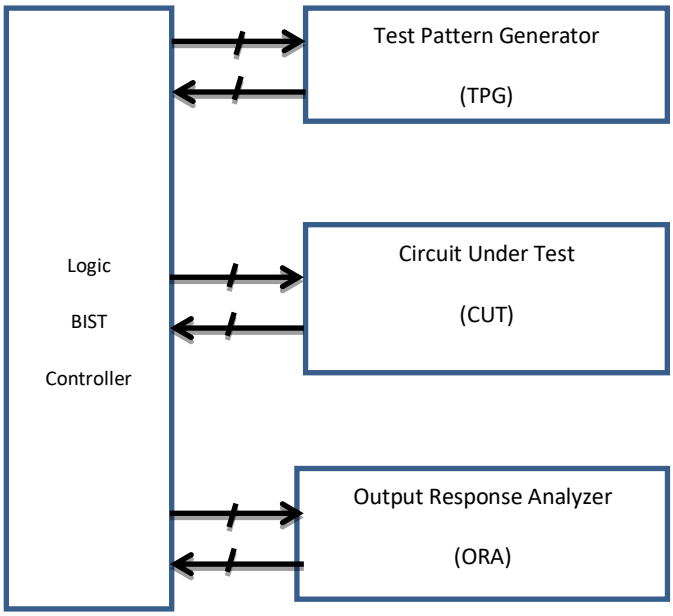

Fig.4 General BIST system

IV.BIST IMPLEMENTATION& RESULTS

Figure 4 Four indicates the BIST hardware structure in more element. Basically, a structure With embedded BIST building joins a check controller, gear test generator, enter multiplexer, Circuit underneath research (CUT). Obviously, a structure with BIST limit in like manner can merge other than the comparator and Read-Only-Memory (ROM). As examined in Figure 3.2, the check controller is used to control the check model and check age all through BIST mode.Hardware structure generator abilities to make the data manual for the CUT.

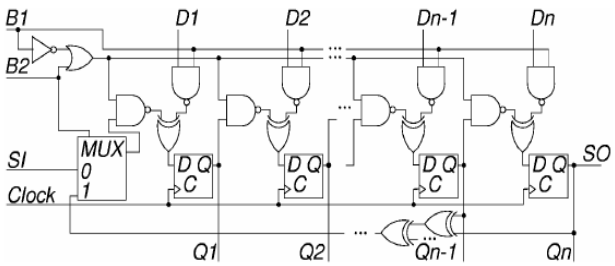

Fig.5 BILBO circuit

Normally, the sample generator generates exhaustive input check patterns to the CUT to make certain the immoderate fault coverage. For instance, a CUT with 10 inputs would require 1024 take a look at patterns.Primary Inputs are the input for CUT in the path of the non-BIST mode or in

January - February 2020
ISSN: 0193 - 4120 Page No. 3163 - 3167

exclusive word, practical mode.Input multiplexer is used to choose accurate inputs for the CUT for one-of-a-type mode.

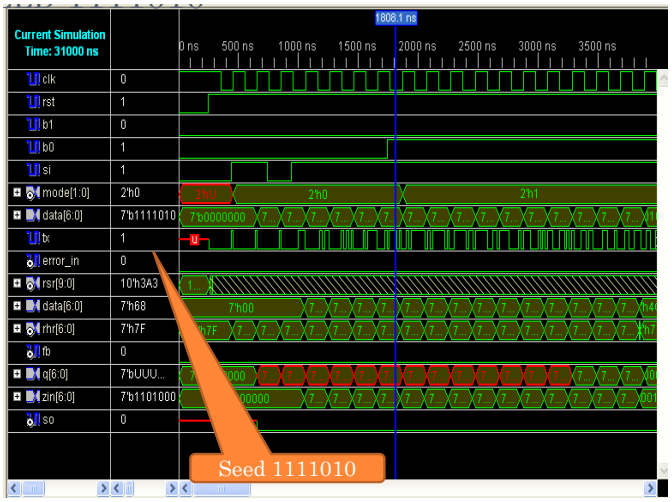

Fig.6 Simulation result for Seed

During BIST mode, it selects input from the hardware During BIST mode, it selects input from the hardware sample generator at the same time as in the course of purposeful mode, selects number one inputs. Output response compactor acts as compactor to reduce the range of circuit responses to possible length that can be used because the signature and saved at the ROM.Implementation of the sample era in addition to the reaction compactor is probably discussed in more data in section below.

During BIST, for every take a look at sample that being generated, the CUT produces a hard and fast of output values.In order to make certain the chip is fault free, each output values from the CUT for each take a look at sample will need to compare with the proper output values received from the simulations.This is a tedious and time-eating approach. Thus, it's far essential to lessen the big of circuit responses to a practicable size that may be each keep inside the chip or can without problems in contrast with the golden response values.For example, a BIST pattern generator in a chip can produce 1 million take a look at styles.If the chip has a entire of one hundred primary output, at the stop of the BIST way, it will generate a total of 1 million output values or 1000000x100 = 100 million bits of output values.With the type of large amount of facts, it is very high-priced and nearly now not feasible to store in the garage or ROM interior a chip.Thus, the circuit reaction want to be compacted.

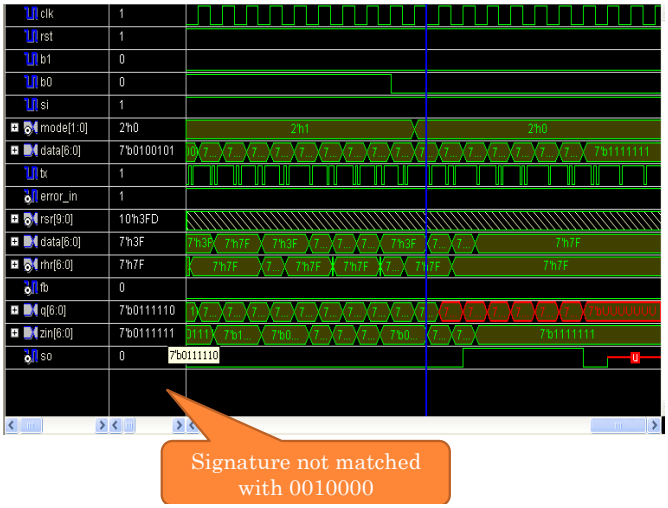

Fig.7 Simulation results for signature

Built-In Logic Block Observers (BILBO) is a circuitry that combines the functionality of the D turn-flop, a wellknown LFSR trying out hardware pattern generator (for the circuit element pushed thru the BILBO Q outputs), a checking out reaction compacter (for the circuit element pushed by using the use of the BILBO D inputs) and a test chain characteristic.By moving in an all-zero pattern into the BILBO in serial check modem the scan chain may be reset to zero. Figure 5 shows the circuit for the BILBO on the identical time as Table 3.1 shows the manage mode for the BILBO of Figure 3.Five.The BILBO in Figure three.Five uses the NAND gate to reinforce up the speed over the implementation with AND and OR gates.

V.CONCLUSION

The reproduced waveforms gave on this paper have shown the unflinching thought of the VHDL use to give an explanation behind the inclinations and the structure of the sorted out UART with embedded BIST. The reenacted waveforms furthermore have certified the passerby how increased the take a gander at envision last thing may be finished by procedure for technique for the use of the BIST framework. With the execution of BIST, over the top analyzer necessities and assessing frameworks starting from circuit or not

January - February 2020
ISSN: 0193 - 4120 Page No. 3163 - 3167

imperative feel degree to concern degree finding are obliged.

The LFSR replaces the piece of the outside analyzer confines together with a test generator by systems for correctly passing on pseudo sporadic styles to give a hundred% flaw thought to the UART module. The MISR goes about as a weight gadget, compacting the yield stop result on an equivalent time as modified pseudo self-vehement model is urged to the UART. The move test in constrained the data/yield overhead through method for moving the parallel etching made through MISR into progressive engraving. The cut expense of the check cost will achieve the game-plan of standard age rate..

REFERENCES

[1] A. P. Stroele, and H. J. Wunderlich, "Hardware-Optimal Test Register Insertion", in IEEE Transactions OnComputer-Aided Design of Integrated Circuits and Systems, June 1998, Vol. 17, No. 6, pp. 531-539.

[2] J. Turino, "RTL DFT Rule Checking - The Circuit Designer's Secret Weapon",Integrated System Design Magazine, 2000.

[3] M. Ibrahim Abubakar, "A Built in Self Testable Bit-Slice Processor", Faculty of Computer Science & Information Technology, University of Malaya, May 1995.

[4] M. S. Michael, "A Comparison of the INS8250, NS16450 and NS16550AF Series of UARTs", National Semiconductor Application Note 493, April 1989.

[5] G. Rajesh Kumar, and K. Babulu. "A Novel Architecture for Scan Cell in Low Power Test Circuitry." Procedia Materials Science 10 (2015): 403-408.

[6] O. A. Petlin, and S. B. Furber, "Built-In-Self-Testing of Micropipelines" in Advanced Research in Asynchronous Circuits and Systems, IEEE, 1997, pp 22-29.

[7] Viswabharathi D., K. Raghuram, and G. Rajesh Kumar. "High Speed Test Architecture for SRAM using Modified March Algorithm."

[8] M. Radha Rani, G. Rajesh Kumar, and A. KarnaRao. "Effective Estimation of Peak-Power for a Testable Digital Circuit." International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) 1.7 (2012): pp-125.

[9] Z. Navabi, "VHDL Analysis and Modeling of Digital Systems", McGraw-Hill Inc., 1991.

[10] Radha Rani, Rajesh Kumar, and Prasanna Kumar. "Implementation of March Algorithm Based MBIST Architecture for SRAM." International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) 1.3 (2012): pp-248.

[11] S. Wang, "Generation of low power dissipation and high fault coverage patterns for scan-based BIST", in Proceedings of International Test Conference, 2002, pp. 834 - 843