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Modeling of Closed Loop ZVS Double Boost DC-DC Converter

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Article Info
Volume 82
Page Number: 3082 - 3092
Publication Issue:
January-February 2020

Article History
Article Received: *14 March 2019*
Revised: *27 May 2019*
Accepted: *16 October 2019*
Publication: *19 January 2020*

Abstract
This proposal presents the analysis of closed loop of ZVS double boost DC-DC converter with increased efficiency and gain for aerospace applications. Boosting the voltage level at the output with low switching losses has been achieved by properly designing the proposed DC-DC converters. However, the output voltage increases in arithmetic progression. Double Boost (DB) technique with ZVS is more powerful than Voltage Boost (VB) technique since its voltage transfer gain increases in geometric progression. To improve the power rating capacity, the proposed control method uses dspic microcontroller to generate the PWM signal and regulate the output voltage. The soft switched double boost DC-DC converter offer benefits particularly higher output voltage with minimal changes than the other boost converters. To verify the concept, simulation and experimentation are carried out. The performance of this converter is experimented for different duty cycles at constant load. The results reveal that the ZVS is achieved in all aspects by reducing the switching losses and increasing the efficiency of the converter to 92%.

Keywords: *Arithmetic Progression, Duty Cycle, Geometric Progression, Double Boost, Soft Switching, Voltage Boost, Zero Voltage Switching.*

I. INTRODUCTION

In DC-DC converter development, the main aim is to achieve high output power with increased efficiency, high power density and less cost topology with modified and simple structure. Stress on the switching devices and the losses occurring during the switching process in the converter circuitsis relative high and it greatly affects the reliability and operating efficiency of the whole circuit. Aalternate switching model should be able to reduce the losses occurring during the switching operation, losses across the other devices used in the circuit and voltage or current pressure without increasing device voltage and current. Inorder to achieve the above said advantages, many techniques have been used in recent years. The methods used in requires two auxiliary switches, which suffer from high current stresses. The devices used in suffers from more voltage stress. Circulating energy exists in the soft switched topologies proposed in and and Zero Voltage Switching is very difficult to achieve at minimal load and increased duty cycles. However, stress due to current during switching on is increased, and converter design becomes more complex. Therefore, this kind of switching cannot be implemented when the converter output voltage goes beyond i.e., twice the applied voltage, and the controllable pulse cycle range in should not exceed the limited by the soft-switching resonant commutation for the topologies proposed in and Voltage liftmethods were used in buck, boost, buck-boost and Cuk converters. The above said converters have increased switching losses, decreased reliability and Electromagnetic Interference (EMI).

The switching devices in the converters uses Pulse Width Modulation (PWM) to have desired output voltage (or) current. These devices are switched on and off at the load current with a high di/dt value. The switching loss could be a significant portion of the total power loss in the converter circuits. Also the converters when operated at high switching frequencies are subjected to high switching losses and high voltage stress across the devices. The EMI is also produced due to increased variation in the current and voltage with respect to time in the converter. To reduce the losses

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happening across the switches during the ON process, electromagnetic interference and to increase the power handling capacity, soft switched process in DC-DC converters with very high voltage conversion ratio are used. These converters offer improved efficiency then the hard switched converters by having either ZV) orZCS in the converter operation.

The soft switching has many advantages over the hard switching which decreases the voltage and current stress across the converter devices, dv/dt and di/dt problems can be minimized so that EMI can be reduced. The ZVS switching technique involves many ways of implementing switching characteristics. Most popularly Quasi Resonant (QR) - ZVS technique is used in order to determine two zero crossing points for switch on and off state[18].To improve the efficiency and lift the output voltage of the converter , this paper implements new techniques to the already available voltage lift DC-DC converter.

II. PRINCIPLE OF OPERATION OF THE ZVS DOUBLE BOOST DC-DC CONVERTER

The schematic figure of double boostconverter topology is given in Figure 1. The circuit have a static device S with resonating components $C_r$andL_r ; two boosting inductors L_1 , L_2; five diodes D_1 , D_2, D_3, D_4 and D_5; total number of capacitors C_1 ,C_2,C_3 and C_4 and the load resistance R. The switch is operated by the PWM signal having the conduction cycle ratio (k) and switching operating frequencyf_s. The power supply values such as input voltage and input current are $V_{in}$and$I_{in}$and output voltage and current parameters such as$V_0$and I_0respectively. The converter voltage gain is $M_d = V_0/V_{in}$.

To analyze the steady-state behavior of this modified DC-DC converter operates in continuous conduction mode, the following assumptions are made:

1.Switching devices used are considered to be ideal.

2.The elements used as reactive components in the circuit are ideal.

3.Inductance L_1 and L_2 are having the bigger value than the resonating inductor L_r.

4.The converter output capacitor $C_4$and the resistive load Rare constant sink of output voltage V_0.

The converter switching time slot isT_s= $1/f_s$, so that the switching on time is $kT_s$and switch-off time is $(1 – k)T_s$. This DC-DC converter has double boost circuit, and a filter capacitor C_4. The boost circuit comprises of D_1-C_1-L_1-$D_2$and D_4-C_3-L_2-D_5. Capacitors C_1, C_2 and C_3 are used to boost the capacitor voltage $V_C$by nine times more than the source voltage V_{in}.

To qualitatively analyze the steady-state action of the converter, each switching cycle is split up into different modes of working. I_M, i_{Lr} and v_{Cr} are given as different values of current and voltage.

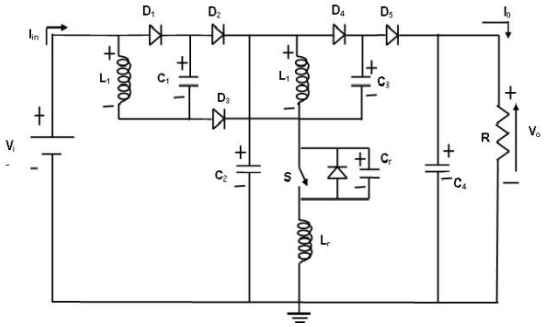

Figure 1 Basic double boost converter.

A. Modes of Operation

Mode 1: Interval T_1= $(t_0 - t_1)$

When switch S is turned off at $t = t_0$, the capacitor voltage $v_{Cr}(t)$ improves linearly with the slope I_M/C_r. The probable sketch forthis mode is given in the Figure 2a. This is the voltage rising interval and it is less than the input voltage V_{in}. The diodes D_1, D_2, D_4 will conduct and D_3 ,D_5 will be in off state. The voltage and current in theresonant capacitor are vCr(t) and i_{Lr} (t)which are written as

$$v_{Cr}(t) = \frac{I_M\, t}{C_r} \qquad (1)$$

$$i_{Lr}(t) = I_M \qquad (2)$$

At $t= t_1$,$v_{Cr}(t_1)= V_{in}$. The time period of this mode is T_1 given as

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$$T_1 = \frac{V_{in} C_r}{I_M} \quad (3)$$

Mode 2: Interval T2=(t1 - t2)

At this mode of operation, as the converter switching deviceS remains in open condition, components such as resonating inductor and capacitor form a circuit and work together; this is the resonance interval as given in Figure 3. Therefore, i_{Lr} starts decreasing and the diodes D_1, D_3 and D_4will go to the off state and D_5 is in the conducting state. The exact mode of operation is presented in Figure 2b. Current through the inductor i_{L1} flows through inductor $L_1$to charge capacitor C_1. Inductor L_1 transfers its stored energy to capacitor C_1. In the meantime, current i_{D2} flows and charges the capacitor C_2 to the voltage V_{C2}. This voltage V_{C2} acts as the source to the next boosting circuit. The current i_{L2} goes through the inductor L_2 to charge the capacitor C_3. Inductor L_2 transfers its stored energy to capacitor C_3 and double the voltage across the load. The deviations of inductor currents are very minimal, so that $i_{L1} = I_{L1}$ and $i_{L2} = I_{L2}$. The inductor currents are given as

$$I_{L1} = \frac{V_{in}\ t_1}{L_1} \quad (4)$$

$$I_{L2} = \frac{V_{C2}\ t_1}{L_2} \quad (5)$$

The capacitor currents are given as

$$I_{C1} = \frac{V_C\ C_1}{t_1} \quad (6)$$

$$I_{C3} = \frac{V_{C3}\ C_3}{t_1} \quad (7)$$

When the capacitor voltage $v_{Cr}(t) > V_{in}$, reactive elements L_r and C_r starts resonating. This interval is called as resonance interval. The capacitor voltage waveform is a sinusoidal function. It reaches its maximum value$V_{Cr(peak)}$and then it decreases to zero at time $t = t_2$.

The state equations are given as

$$i_{Lr}(t) = C_r \frac{dv_{Cr}}{dt} \quad (8)$$

$$V_{in} - v_{Cr}(t) = L_r \frac{di_{Lr}}{dt} \quad (8a)$$

The solutions of the state equations with the starting conditions $v_{Cr}(t_1) = V_{in}$and$i_{Lr}(t_1) = I_M$ will give the resonant capacitor voltage and resonant inductor current for $t > t_1$.

$$v_{Cr}(t) = V_{in} + Z_1 I_M \sin \omega_r t \quad (9)$$

$$i_{Lr}(t) = I_M \cos \omega_r t \quad (10)$$

where $Z_1 = \sqrt{\frac{L_r}{C_r}}$ and $\omega_r = \sqrt{\frac{1}{L_r C_r}}$

When the current through L_r starts moving towards the Zero, it will improve the potential voltage in the resonating C_r. At $t = t_1'$, i_{Lr}moves to zero and v_{Cr}goes to the max. asgiven in the Figure 3. Max.value of the resonant capacitor voltage is given as

$$v_{Cr}(t_1') = V_{Cr(peak)} = V_{in} + Z_1 I_M \quad (11)$$

The i_{Lr}att = t_1' is given as

$$i_{Lr}(t_1') = 0 \quad (11a)$$

In the time intervalbetween t_1' and t_1'', the power and the energy transfers from $C_r$back to L_r decreasing v_{Cr} from its peak value to V_{in} and current i_{Lr}reaches the negative peak $-I_M$.

For $t > t_1''$, the solutions of the Equations 8 and 8a with the basic conditions $v_{Cr}(t_1'') = V_{in}$ and $i_{Lr}(t_1'') = -I_M$ are given by

$$v_{Cr}(t_1'') = V_{in} - Z_1 I_M \sin \omega_r t \quad (12)$$

$$i_{Lr}(t_1'') = -I_M \cos \omega_r t \quad (12a)$$

Exactly at $t = t_2$, the voltage across the resonating capacitor $v_{Cr}(t)$goes to zero, this makes ZVS condition for switch S

$$v_{Cr}(t_2) = 0 \quad (13)$$

$$i_{Lr}(t_2) = -I_M \cos \alpha \quad (13a)$$

where $\alpha = \sin^{-1}\left[\frac{V_{in}}{I_M Z_1}\right]$ (13b)

Time period for this operation is given by

$$T_2 = (t_2 - t_1) = \frac{(\pi + \alpha)}{\omega_r} \quad (14)$$

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Mode 3 : Interval T3=(t2 - t3)

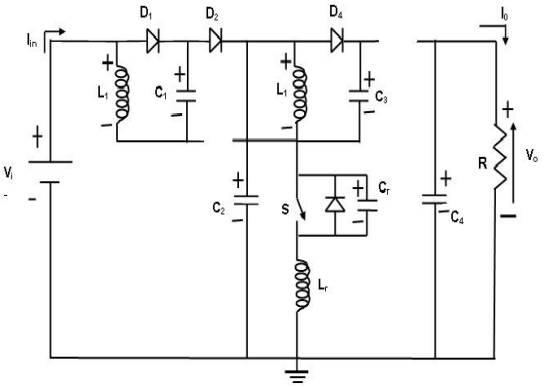
During the point t=t_2 , the converter switching device S is switched on at zero voltage condition. The resonating inductor current starts increasing linearly with the slope $V_{in}/(L_r+L_1+L_2)$. This is the linear recovery interval. The mode 3 working diagram of is given in Figure 6.2c. Since load current I_0 is assumed constant, the current $i_{Lr}(t)$starts increasing from $-I_M \cos\alpha$ to $+ I_M$. At t = t_3, the diodes D_3, D_4 and D_5become reverse biased and stops conducting. The time period of this mode is given by,

$$T_3 = \frac{I_M(1+\cos\alpha)(L_r+L_1+L_2)}{V_{in}} \quad (15)$$

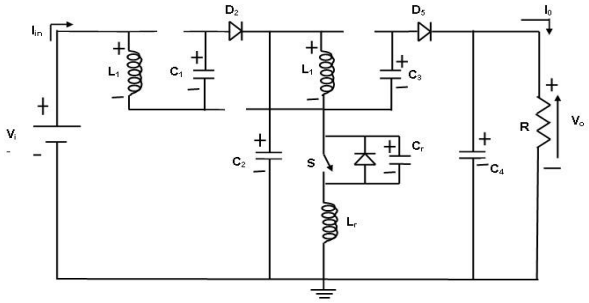
Mode 4: Interval T4=(t3 - t4)

During this period, the current through the load is due to the source voltage V_{in}. The diodes D_1, D_4start conducting and D_2 ,$D_5$are blocked till t = t_4; actual and normal switch on time period as given in Figure 6.3. The source current i1 = i_{L1} + i_{C1} + i_{L2} + i_{C3}. The circuit diagram of this time interval is shown in Figure 2d. During this mode, $i_{Lr}(t)$ remains constant at I_M. This operation continues until the switching deviceS is opened at time t = t_4 and it repeats. The time period of operation of this mode is given by

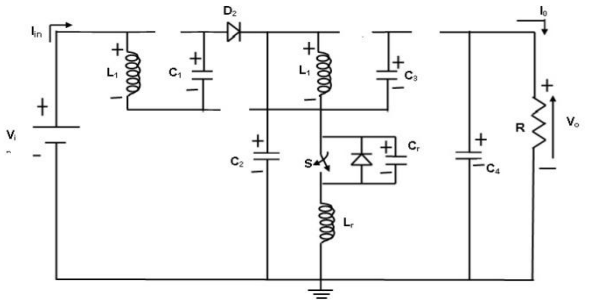
$$T_4 = T_s - (T_1 + T_2 + T_3) \quad (16)$$



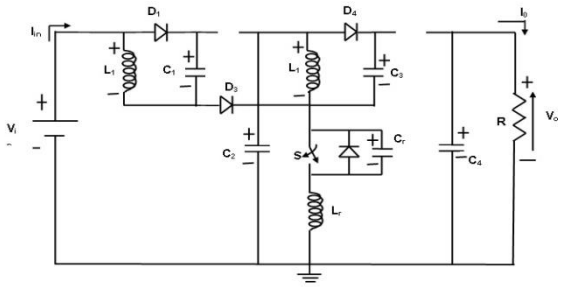
(a) Mode 1 ($t_0 \leq t \leq t_1$)



(b) Mode 2 ($t_1 \leq t \leq t_2$)



(c) Mode 3 ($t_2 \leq t \leq t_3$)



(d) Mode 4 ($t_3 \leq t \leq t_4$)

Figure 2 ZVS high gain super boost DC-DC converter topological modes of a switching cycle (a) Mode 1 – $t_0 \leq t \leq t_1$ (b)Mode 2 – $t_1 \leq t \leq t_2$ (c) Mode 3 – $t_2 \leq t \leq t_3$ (d) Mode 4 – $t_3 \leq t \leq t_4$

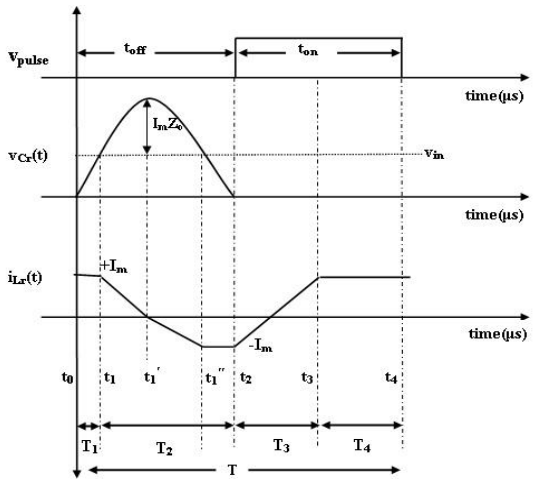


Figure 3 Theoretical waveforms of ZVS double boost DC-DC converter.

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III ANALYSIS OF THE ZVS HIGH GAIN DOUBLE BOOST DC-DC CONVERTER& RESULTS

Considering that the output power is equal to the input power

$$P_{in} = P_o \ (or)\ V_{in} I_{in} = V_o I_o \quad (17)$$

Ideally, from the energy conversion concept, the time interval given , the power supply energy value $E_{in}$is equal to the power output energy value E_0 and it is given by the below expression

$$E_{in} = V_{in}\left[\int_0^{T_1/2} i_{in}(t)\,dt + \int_0^{T_4} i_{in}(t)\,dt\right] \quad (18)$$

whereT_1 and T_4 are the period of time for operating modes 1 and 4 .

In the energy expression 18, limits$T_1/2$ and T_4 will specify the movement of energy from no load to the load for half time of T_1 time interval and for the full T_4 time intervals. Since the supply current $i_{in}(t)$ is more or less equal to I_M during the first and fourth interval,

$$E_{in} = V_{in} I_M \left[\frac{T_1}{2} + T_4\right] \quad (18a)$$

The converter output energy over one complete cycle is obtained by analyzing and evaluating the given below equation

$$E_o = \int_0^{T_s} i_0(t) V_o\,dt = V_0 I_o T_s \quad (19)$$

Therefore, the DC-DC voltage conversion ratio is defined as

$$M_d = \frac{V_o}{V_{in}} = \frac{1}{T_s}\frac{I_M}{I_o}\left[T_s - \frac{T_1}{2} - T_2 - T_3\right] (20)$$

Put the values of T_{d1} – T_{d3}, Expression 20 is changed in terms of circuit parameters as

$$M_d = \frac{I_M}{I_o}\left[1 - \frac{V_{in} C_{r1}}{2 I_M} f_s - \frac{(\pi+\alpha) f_s}{2\pi f_r} - \frac{I_M (1+\cos\alpha)(L_r + L_1 + L_2)}{V_{in}} f_s\right] \quad (21)$$

Resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_r C_r}}$ (22)

Normalized switching frequency $f_{ns} = \frac{f_s}{f_r}$ (23)

Characteristic impedance $Z_1 = \sqrt{\frac{L_r}{C_r}}$ (24)

Normalized load resistance $R_N = \frac{R}{Z_1}$ (25)

Equation 21 will give two different values of M_d, in which, the maximum value $M_{d(max)}$is considered for the design. It is noted that, M_d is a function of R and f_s. The value of $M_d$can be controlled and regulated by varying f_s.

The voltage builds across capacitor C_1 and it is charged to V_{in}. The current i_{L1} flows through L_1 which rises with the input voltage V_{in} during switch-on time period $kT_s$and comes down to the voltage $-(V_1 - 2V_{in})$ during switch-off time period $(1 - k)T_s$. So, the changes in the inductor current i_{L1} is given as

$$\Delta i_{L1} = \frac{V_{in}}{L_1} k T = \frac{(V_0 - 2V_{in})}{L_1}(1-k)T \quad (26)$$

The voltage across the capacitorC_2 is given as

$$V_1 = \frac{(2-k)}{(1-k)} V_{in} \quad (27)$$

The voltage increases in the capacitor C_3 and it is charged to V_1. The amount of current passing through inductor L_2 rises to the voltage V_1 during switch-on time period $kT_s$and comes down to the voltage $-(V_O - 2V_1)$ during switch-off time period $(1 - k)T_s$.

So, the changes on the inductor current i_{L2} is

$$\Delta i_{L2} = \frac{V_1}{L_2} k T_s = \frac{(V_0 - 2V_1)}{L_2}(1-k)T_s \quad (28)$$

The output voltage is given as

$$V_o = \frac{(2-k)}{(1-k)} V_1 = \left(\frac{2-k}{1-k}\right)^2 V_{in} \quad (29)$$

The voltage transfer gain in continuous mode is given by

$$M_s = \frac{V_0}{V_{in}} = \left(\frac{(2-k)}{(1-k)}\right)^2 \quad (30)$$

The input supply current $i_{in}$is equal to (i_{L1} + i_{C1} + i_{L2} + i_{C3}) during switch-on time interval and only equal to i_{L1} + i_{L2}during switch-off time interval.

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Capacitor current i_{C1} is equal to i_{L1} and i_{C3} is equal to i_{L2} during switch off.

We obtain the following equations:

$$i_{in-off} = i_{L1-off} + i_{L2-off} = i_{C1-off} + i_{C3-off}$$

(31)

$$i_{in-on} = i_{L1-on} + i_{C1-on} + i_{L2-on} + i_{C3-on}$$

(32)

IV. DESIGN AND SIMULATION OF ZVS DOUBLE BOOST DC-DC CONVERTER

The ZVS double boost DC-DC converter as shown in Figure 1 is analyzed and designed with the following values:

V_{in} = 5 V, L_r= 100µH, C_r= 1µF, L_1=10µH, L_2=10µH ,C_1=1µF, C_2=1µF, C_3=1µF, C_4 = 200 µF, I_0= 0.09 A to 0.106 A ,V_0 = 45 V , f_r= 16 kHz and R = 500 Ω for a switching frequency of 11.11kHz with the duty cycle of k= 0.5.

The converter is simulated using MATLAB/Simulink software tool with the designed values and relevant waveforms are shown in Figure 4.

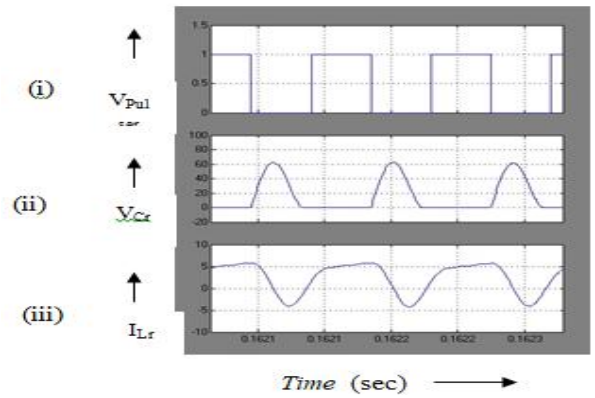

Figure 4 Simulated waveforms of (i) Gate pulse signal generated – 0.5 volts/div Vstime(sec) (ii) Resonating capacitor voltage – 20 Volts/div Vs time(sec) (iii) Resonating inductor current - 5 Amps/div Vs time(sec)

Inference from the simulated waveforms says that the converter switch S when switched on at the point where the voltage across the resonant capacitor become zero or very nearer to zero value, thereby decreasing the converter switching losses.

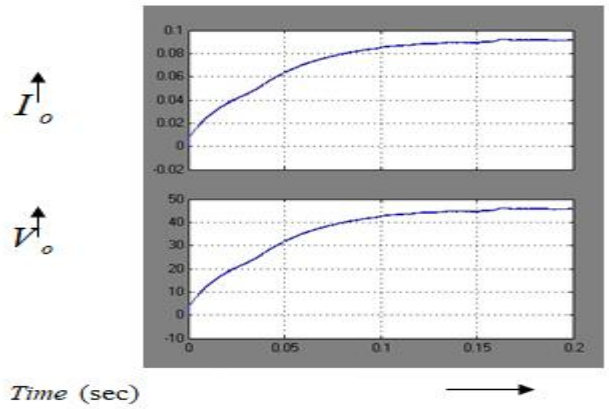

Figure 5 (i) Output current – 0.02 Amps/div Vstime(sec) (ii) Output voltage – 10 Volts/div Vs time(sec)

The M Vsf_{ns} for different normalized load R_N is clearly give in the simulated waveform in the Figure 5a. At normal operating condition, R_N = 50, the voltage changing ratio M is 8.6 for f_{ns}=0.694. When R_N is from 50 to 40, M is from 8.6 to 8.42. In order to have M at 8.6, the f_{ns} has to be varied from 0.694 to 0.564. Similarly, when the load is varied from 50 to 60, M is raised from 8.6 to 8.83. To have M at 8.6, the f_{ns} has to be changed varied from 0.694 to 0.873. It is found that the changes of M with f_{ns} are more of less linear and M is very sensitive to the changes in the load. So, closed loop operation is implemented in order to stabilise and control the output voltage.

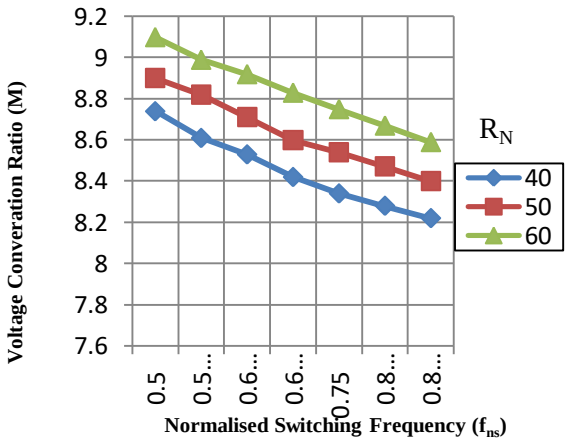

Figure 5a Characteristics of normalized switching frequency (f_{ns}) Vs Voltage conversion ratio (M)

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V. OPEN LOOP EXPERIMENTAL IMPLEMENTATION OF ZVS SUPER BOOST DC-DC CONVERTER

To analyze and verify the design, a ZVS double boost DC-DC converter is experimented and tested with the designed parameters. The inductors are of iron ferrite air core and the capacitors used are made of plain polyester and electrolyte type. The diode FR107 used in the circuit is a fast recovery diode. The IRF540N is active switch which is dynamic and can carry high current at high frequency with simple drive requirement. The triggering pulses at 11.11 kHz with variable duty cycle is generated using dSpic30F4011 controller and it is fed to the driver circuit which consists of transistors BC558 and 2N222, opto-coupler(TLP250), diodes (FR107) , zener diode with the capacitors and resistors. The driver circuit is shown in Figure 6. The practical setup is shown in Figure 7. The performance of the circuit is studied under constant load condition for various duty cycles.

The open loop experimental waveforms are shown in Figures 10 to 14. Noted that the switch is made to switch on when the resonant capacitor voltage is at zero value and it confirms ZVS condition. The experimental outputs obtained resemble the simulated outputs as shown in Figures 4 & 5. The deviations noted between the simulation and the experimental values may be due to parasitic components and noise.

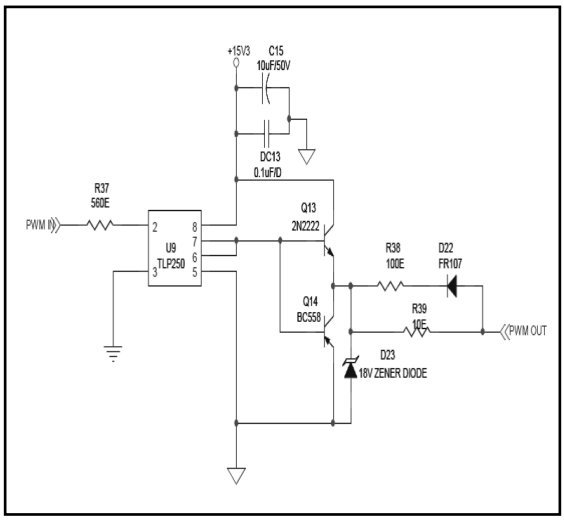

Figure 6 : Driver circuit

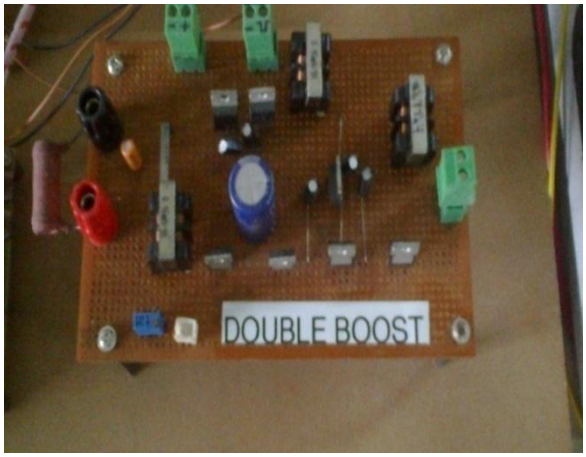

Figure 7: Photograph of experimental setup of ZVS double boost DC-DC converter

For the switching frequency f_s=11.11kHz, V_{in}=5V and R= 500 Ω, Table: 1 and 1a shows the variation of output voltage, gain and efficiency for different duty cycles at constant load for soft switching and hard switching. The same are graphically shown in Figures 8, 9 and 10 respectively. It is inferred that higher output voltage and efficiency are obtained with soft switching compared to hard switching

TABLE 1 : VARIATION OF OUTPUT VOLTAGE, GAIN AND EFFICIENCY FOR VARYING DUTY CYCLE – SOFT SWITCHING

Duty Cycle (K)	I_{in} (A)	V_O (V)	I_O (A)	M_S	%η
0.4	0.85	40.0	0.090	8.0	84.70
0.44	0.87	41.5	0.091	8.3	86.81
0.46	0.88	42.5	0.094	8.5	90.79
0.50	0.90	43.0	0.096	8.6	91.73
0.54	0.94	43.5	0.098	8.7	90.70
0.58	1.01	44.0	0.100	8.8	87.12
0.6	1.12	45.0	0.106	9.0	85.17

TABLE 1A :VARIATION OF OUTPUT VOLTAGE, GAIN AND EFFICIENCY FOR VARYING DUTY CYCLE – HARD SWITCHING

Duty Cycle (K)	I_{in} (A)	V_O (V)	I_O (A)	M_S	%η
0.4	0.92	36.3	0.078	7.26	61.55
0.44	0.98	37.8	0.081	7.56	62.45
0.46	1.08	38.5	0.089	7.70	63.45
0.50	1.19	39.3	0.097	7.86	64.06

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0.54	1.24	40.4	0.109	8.08	71.02
0.58	1.32	41.0	0.112	8.20	69.57
0.6	1.44	41.4	0.118	8.28	67.85

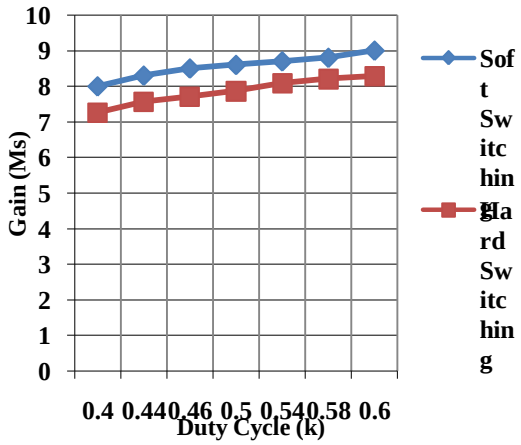

Figure 8: Variation of gain for different duty cycles

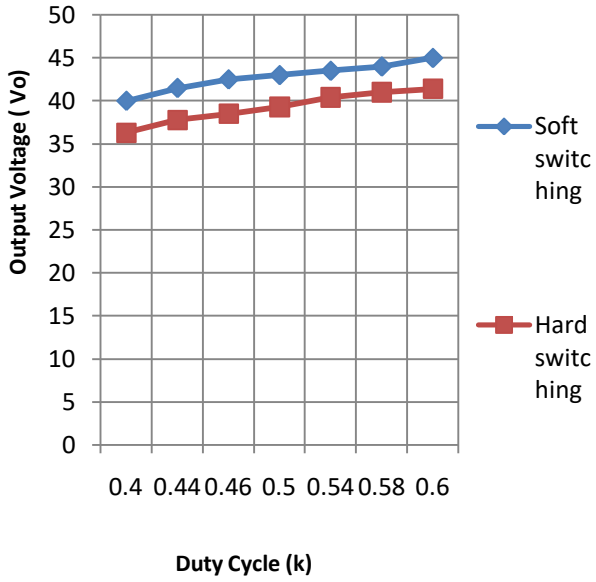

Figure 9: Variation of output voltage for different duty cycles

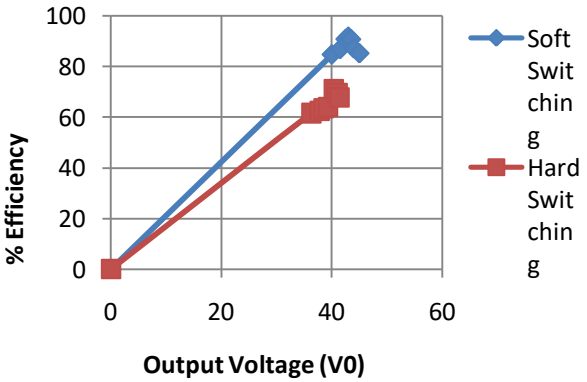

Figure 10 : % Efficiency Vs Output voltage(V_0)

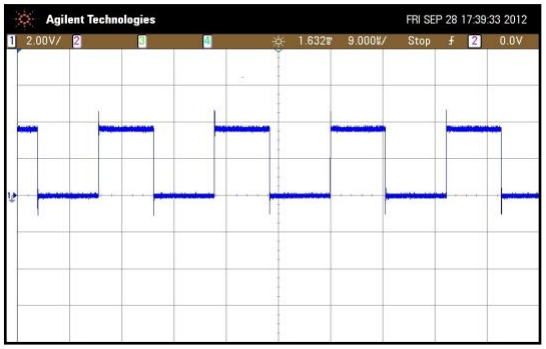

Figure 11: Gate pulse generated using microcontroller
X-axis: 9µs/div, Y-axis: 2 Volts/div

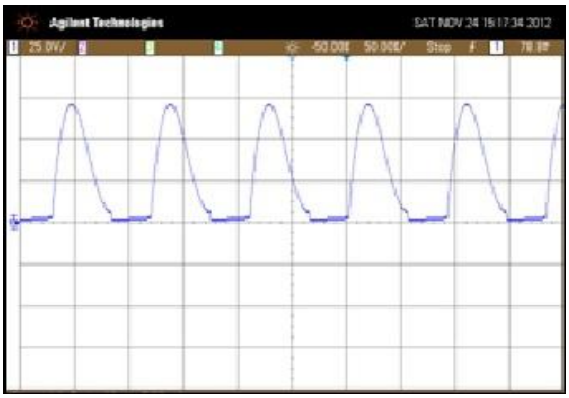

Figure 12 Resonating capacitor voltage
X-axis: 50µs/div, Y-axis: 25 Volts/div

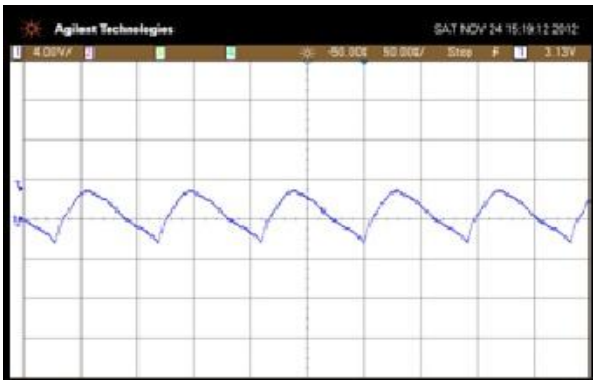

Figure 13: Resonating inductor current
X-axis: 50µs/div, Y-axis: 4 Amps/div

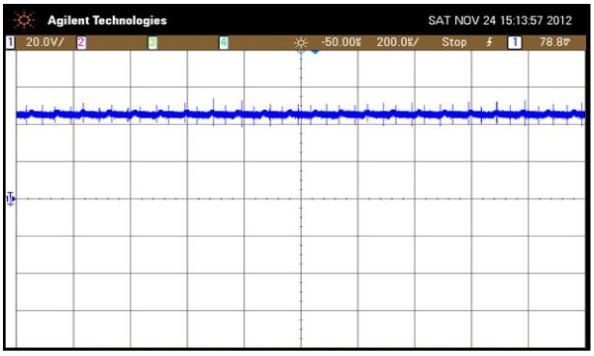

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Figure 14 : Output voltage (43 V)
X-axis: 200μs/div, Y-axis: 20 Volts/div

VI. CLOSED LOOP EXPERIMENTAL VERIFICATION OF ZVS DOUBLE BOOST DC-DC CONVERTER

The closed loop experimental setup with circuit diagram of a ZVS double boost DC –DC converter is shown in Figure 15. For closed-loop operation, the output voltage is measured and sensed using the potential divider and is fed through a signal conditioner which converter analog signal to digital signal. The output from ADC is fed to an error detector. Error detector compares the reference voltage with the actual voltage and the output is fed to a PI Controller with proportional gain Kp=0.099 and integral gain K_i=0.0099. Output of the PI Controller determines the duty cycle of the PWM signal. The PWM control signal is then applied to the switch of the converter circuit without losing the zero voltage switching condition. This configuration is designed for a switching frequency of 11.11 kHz in closed-loop operation. The analysis and the performance of the closed-loop system is studied for different load conditions and different values of supply input voltage. At the time of closed-loop operation, the controller designed is able to keep the output voltage equal to the set value of 45 V despite the changes in the input supply voltage of 1V (20%) and the input voltage waveforms are verified in Figures 6.16a and 6.16b. The digital controller also acts smartly and effectively, brings back the output voltage to the reference value of 45 V with ZVS condition. The resonant waveforms and output waveforms are shown in Figures 17a, 17b, 18a and 18b respectively. The output results show the importance of the PI controller for the voltage regulation of a ZVS double boost DC-DC converter. The efficiency of the ZVS double boost DC-DC converter is estimated and calculated by obtaining the parasitic losses in the inductors, capacitors, switching and conduction losses of devices and it is obtained as 91%. So, the proposed ZVS double boost DC-DC converter has low switching losses, high-voltage transfer gain, high reliability and less EMI.

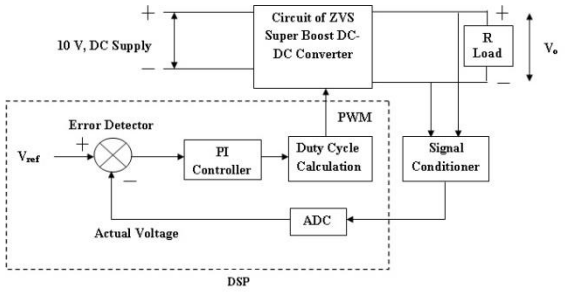

Figure15: Closed loop control of ZVS double boost DC – DC converter

Figure 16a: Input voltage changing from 4V to 6V
X-axis: 1 sec/div , Y-axis: 5 Volts/div

Figure 16b: Input Voltage changing from 6V to 5V
X-axis: 1 sec/div, Y-axis: 5 Volts/div

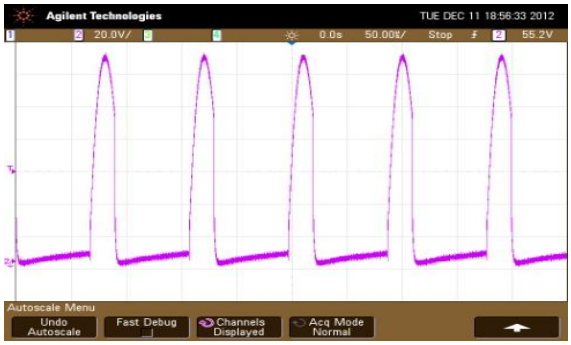

Figure 17a Resonating capacitor voltage for change in input voltage from 4 V to 6 VX-axis: 50μs/div, Y-axis: 20 Volts/div

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Figure 17b Resonating capacitor voltage for change in input voltage from 5V to 6 V X-axis: 50µs/div, Y-axis: 20 Volts/div

Figure 18a: Regulated output voltage (40 V) for change in the input voltage from 4 V to 6 VX-axis: 2 sec/div, Y-axis: 20 Volts/div

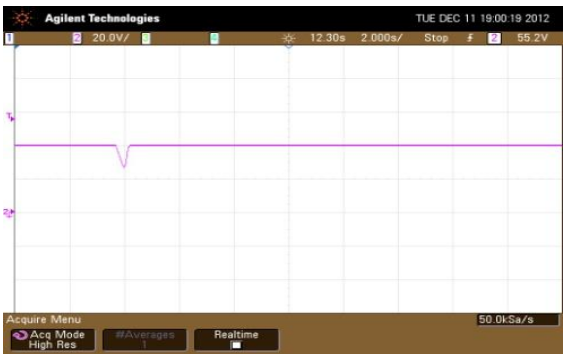

Figure 18b: Regulated output voltage (40 V) for change in the input voltage from 6 V to 5 VX-axis: 2 sec/div, Y-axis: 20 Volts/div

VII. CONCLUSION

In this chapter, the output voltage of the converter is boosted for constant load and variable duty cycle to nine times the input voltage. The zero voltage switching across the switching device S is achieved during the operation. The theoretical, simulated and practical output waveforms for open loop and closed loop were obtained for various duty cycles and input voltage variations. The technique overcomes the effects of parasitic elements and greatly increases the efficiency (91%) and the output voltage of the DC-DC converter with high power density, cheap topology and easy control

VII. REFERENCES

[1] G. Hua and F. C. Lee, "Novel zero-voltage-transition PWM converters," in Proc. IEEE PESC'92, 1992, pp. 55–61.

[2] J. P. Gegner and C. Q. Lee, "Zero-voltage-transition converters using an inductor feedback technique," in Proc. IEEE APEC'94, 1994, pp. 862–868.

[3] D. C. Martins, F. J. M. de Seixas, J. A. Brilhante, and I. Barbi, "A family of dc-to-dc PWM converters using a new ZVS commutation cell," in Proc. IEEE PESC'93, 1993, pp. 524–530.

[4] K. Taniguchi, T. Yoshikawa, et al., "Quasiresonant PWM converter with high quality input waveforms and high efficiency," in Proc. IEEE PESC'94, 1994, pp. 1131–1136.

[5] J. Bassett, "New, zero voltage switching, high frequency boost converter topology for power factor correction," in Proc. Int. Telecommunication Energy Conf., Oct. 1995, pp. 813–820. M. C. Duarte and I. Barbi, "A new family of ZVS-PWM active clamping dc-to-dc boost converters: Analysis, design and experimentation," in Proc. Int. Telecommunication Energy Conf., Oct. 1996, pp. 305–312.

[6] M. M. Jovanovic, "A technique for reducing rectifier reverse-recovery related losses in high-voltage, high-power boost converters," in Proc. IEEE APEC'97, 1997, pp. 1000–1007.

[7] L. R. Barbosa et al., "A family of PWM soft-single-switched converters with low voltage and current stresses," in Proc. IEEE PESC'97, 1997, pp. 469–474.

[8] N. H. Kutkut and K. W. Klontz, "Design consideration for power converters supplying the SAE J-1773 electric vehicle inductive coupler," in Proc. IEEE APEC'97, 1997, pp. 841–847.

[9] LUO F.L., YE H.: 'Essential DC–DC converters' (CRC Press and Taylor &Francis Group, New York, 2006)

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ISSN: 0193 - 4120 Page No. 3082 - 3092

[10] HE Y., LUO F.L.: 'Analysis of Luo converters with voltage lift circuit', IEE Proc. Electr. Power Appl., 2005, 152, (5), pp. 1239–1252
[11] LUO F.L.: 'Positive output Luo-converters voltage lift technique', IEE-EPA Proc., 1999, 146, (4), pp. 415–432
[12] LUO L.: 'Negative output Luo-converters: voltage lift technique', IEE-EPA Proc., 1999, 146, (2), pp. 208–224
[13] ZHU M., LUO F.L.: 'Implementing of developed voltage lift technique on SEPIC, CUK and double-output DC–DC converters', IEEE Trans. Ind. Electron. Appl., 2007, 23, (25), pp. 674–681
[14] ZHU M., LUO F.L.: 'Series SEPIC implementing voltage-lift technique for DC–DC power conversion', IET Power Electron., 2008, 1, (1), pp. 109–121
[15] MOHAN N., UNDELAND T.M.: 'Power electronics converters, electronics, application and design' (John Wiley and Sons, Singapore, 2004)
[16] ARULSELVI S., UMA G.: 'Design and implementation of CFZVS-QRC using analog resonant controller UC3861', Int. J. Electron., 2007, 94, (1–2), pp. 55–73
[17] FANG LIN and LUO HONG YE : 'Advanced DC/DC Converters' CRCPRESS, Boca Raton London New York Washington, D.C

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I am the profession member in IEI, IEEE, ISTE IUCEEE. I have got best faculty award in the academic year 2010 and produced 100% result in more than 5 subjects which I have taught. I am one of the members in advisory committee in some of the leading engineering colleges