TEST Engineering & Management

May-June 2020
ISSN: 0193-4120 Page No. 29462 - 29469

Camera Interfacing using FPGA suitable for Video Processing Applications

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Article Info
Volume 83
Page Number: 29462 - 29469
Publication Issue:
May-June 2020

Article History
Article Received: *19 August 2019*
Revised: *27 November 2019*
Accepted: *29 January 2020*
Publication: *6 May 2020*

Abstract

This paper presents unique, innovative reconfigurable system architecture to interface OV5640 camera module using FPGA with a multifunctional and high-performance realizations that captures images and videos within real time constrains. A method for image capture, processing image and a camera driver are realized in the Xilinx Spartan-6 FPGA board with 256Mbit DDR- SDRAM. The FPGA module is interfaced directly to DDR- SDRAM memory banks for camera interface. Here tradeoff between higher frame rate, device utilization and power consumption has been analyzed. The device performance is analyzed for indoors as well as outdoors. The developed system is compatible to different clock frequencies and number of pixel processing cores. Results obtained shown 1% increase in device utilization and only 0.27mW rise in power consumption of camera controller logic for 100fps compared to 20fps processing. Frames from camera at 85 MHz pixel clock are processed by FPGA operating at 50 MHz thereby synchronizing 256Mbit DDR-SDRAM along with 65 MHz VGA monitor providing up to 100 fps operation.

Keywords: *Video Acquisition, Camera Interface, Video Processing on FPGA.*

I. INTRODUCTION

The requirement of image and video processing systems in the products personal digital assistant, hand held units and mobile phones continue to increase. To meet power and performance demands of these applications there is need to develop standard hardware architecture. The main problems faced by the designers of modern, portable, hand-held, digital systems is the need to reduce the power requirement of the overall system to outspread the duration of battery lifespan. Numerous of these systems execute digital signal processing functions on video signals where the computational requirements consistently grow, putting extra overhead on power requirement.

Video processing systems are believed to provide performance at particular frames per second with restricted battery lifespan that needs to operate for particular time period only. And if during running operation suddenly fast moving object is observed. This will require that frame rate should be increased and it will suddenly increase power requirement. Hence power and resource management is very important for time varying constraints. For less power also performance of system should not degrade ideally. A scene change should trigger requirement to optimize power and resources. For achieving this a system, which is compatible to various values of clock rates and number of pixel processing modules by changing number of

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input/output bits values is required to be implemented.

Real-time digital video processing system needs high throughput rate and huge tasks to be performed by the system. To cater this need, parallel processing in the form of conventional hardware or multiple data processing in the form of software task are therefore crucial. For a certain application, system design using hardware is always superior choice for their lower system cost and faster operation. Over past few years SRAM based FPGAs have made substantial advances in device fabric features and support for partial reconfiguration, various IP components like embedded CPUs, memory, millions of logic gates have become viable option for high demand Image processing applications.

In this work, FPGA is used to implement and test embedded system for camera interface. To program these devices Hardware Description Language (HDL) is used. Since, HDL enables description of circuits precisely; it provides an opportunity for the designers to optimize speed of operation from the available timing constraints. Integrating camera and necessary control logic on FPGA board helps to achieve desired objective. The system is design that helps to process large number of real time image frames per unit time, minimum power requirement and resource utilization of device. Major advantages of said system are ability to carry out huge amount of video data in a system, though preserving minimum power requirement and resource utilization.

The paper has been organized a follows: Section II explains literature review of related work in this area. Section III deals with embedded system architecture for camera interface. Section IV describes experimental results followed by conclusion and future scope of the presented work.

I. LITERATURE REVIEW

FPGA reconfiguration is used in various operations of image and video processing like DCT [1], Kalman and wavelet filters [2], Finger print recognition [3], Finite Impulse Response (FIR) filters [4]. The main objective to use FPGA in these applications is to improve the overall performance of the system (a detailed discussion of this form of the work is, though, beyond the scope of this research article). FPGA is also used in several image enhancement applications. It is used to find the tradeoffs between power, performance, and accuracy of hardware designs in Single pixel processor for Image enhancement [5], Gamma correction [6] [7] [8], Contrast enhancement and Histogram equalization [9], Successive mean quantization transform for image enhancement [10]. Power consumption is estimated using Xilinx power analyzer (XPA) tool which provides an accurate result based on simulated switching activity of the place-and- routed circuit and exact utilization statistics [11]. Power estimation in reconfigurable systems is an area of active research. XPA accuracy of 70%–94% was reported in [12] for dynamic power consumption.

The software implementation of most of computer vision systems could not achieve the frame rate required for real-time processing of video data coming from the camera [13]. For this reason a real-time video acquisition on FPGA board is very necessary requirement. The research article [14] explains interfacing Xilinx FPGA board with a camera for automatically detecting object using dynamic memory features. The paper [15] explains formation of smart camera obtained by coupling of a 1.3 Megapixel CMOS camera and Virtex-6, in which pre-processing algorithms have been used to enhance the dynamic range of recorded images. The research article [16] explains development procedure for the use of FPGA board for interfacing a camera for object detection application. The various ideas in the context of interfacing cameras, with an FPGA are explained in [17]. The organization functions of optical device such as image data capture in addition to some graphical operations viz. vertices detection, processor cooperation and calculation of an optical flow can be performed by FPGA is discussed in [18]. The research article [19] describes the working of an intelligent integrated camera which uses an

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Altera FPGA and limited banks SRAM; the camera is intended to perform real time image processing implementation of different image noise removal algorithms for superior image quality. Dynamic partial reconfiguration ability of the Xilinx Virtex FPGA for interfacing smart camera system is published in [20]. In reference [21], FPGA with dynamic memory reconfiguration is used in the development of video signal processing system. Here captured frame is stored and updated in peripheral memory. Reference [22] describes implementation of a widespread system level hardware strategy using a hardware description language and authenticated on the DE2-115 FPGA evaluation board. Their main objective is to study the attainable performance with a low cost FPGA chip based camera interface suitable for image processing applications. Intelligent cameras are compact systems that combine the functions of image acquisition; detection of object and various parameter analyses is described in [23].

The significant contribution of this work is to develop specific video processing architecture suitable for real time video processing. This paper concentrates on developing a reconfigurable architecture suitable for different frame rates and operating frequencies. Many advanced features are considered within one unit to address following points which did not exist previously:

- FPGA architecture is designed to meet high performance with minimum power consumption and resource utilization.
- Developing FPGA – Camera interface for Image acquisition through the Inter-Integrated Circuit (I^2C) serial bus.

II. EMBEDDED SYSTEM ARCHITECTURE FOR CAMERA INTERFACE

The overall structure of system is shown in Figure 1. The central part of the system is a dynamically reconfigurable FPGA Xilinx Spartan 6 device. Moreover it contains several peripherals on board. It contains 256Mbit Simple Dynamic Random Access Memory (SDRAM) on the board used to store image frames Flash memory with Serial Peripheral Interface (SPI) and I^2C interface. The input output ports are used for communication between camera and FPGA board. The FPGA board also has multiple power supply available. The signals from FPGA module are linked to the peripheral communication interfaces (e.g. Ethernet, USB), VGA output and Camera control interface are available on board. The FPGA is capable of operate with different values of clock rate. During operation it is possible to connect with any memory unit and transfer processed data output to the VGA port. The VGA and camera can operate with various clock rates during working condition. The System allows reading and writing operation into SDRAM by specifying address and selecting specific bank. Memory storage bandwidth of Visualization systems is often limited because large portion memory storage is occupied for storing image frames instead of preferred logic. The implementation requires interfacing external memory SDRAM, because FPGA internal memory is not enough to store captured and processed image frames.

The method developed aims toward an implementation that will help to perform optimal digital video processing as shown in Figure 2. It shows conceptual block diagram to illustrate how data flows in the system. I^2C is used to communicate with camera OV5640.

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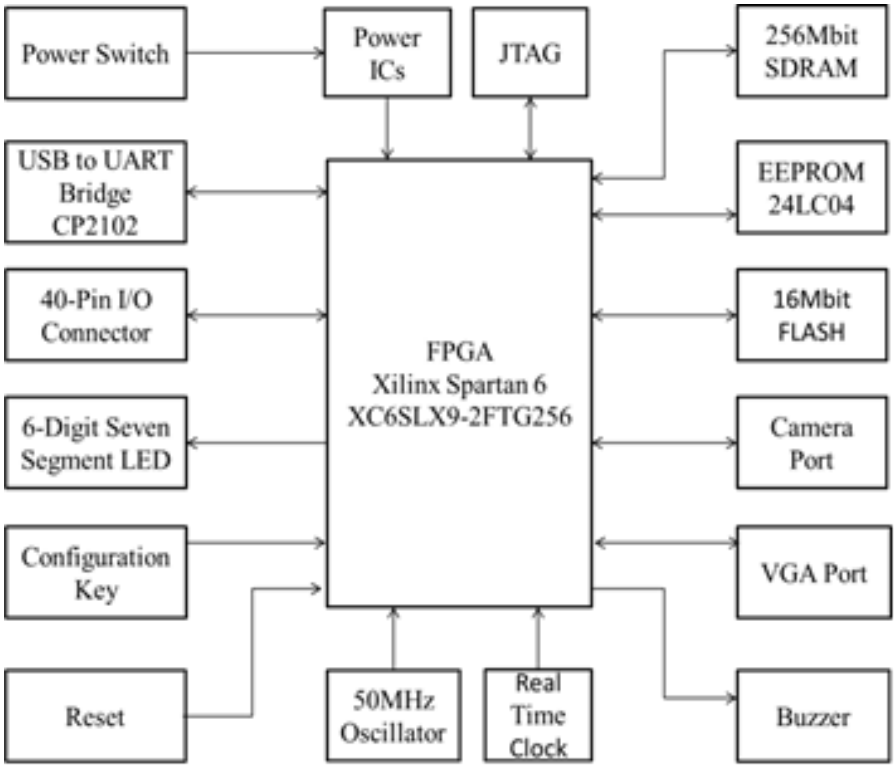

Figure 1: FPGA board schematic

The system is programmed through registers via I^2C serial interface. Serial clock (SIOC) and serial data (SIOD) are the main registers used for communication and programming of I^2C bus. VGA generator is used to generate Red, Green and Blue signals in RGB565 format and it generates vertical and horizontal synchronization signals for 1024 768 pixel resolution. The job of frame buffer is to store runtime data like input image frames and processed image frames. The system is implemented in reprogrammable resource is used perform operations Image acquisition and processing, power analysis and visualization of resultant image. Clock generation and distribution is implemented in hardware.

Capture logic is used to read the data from camera and convert it into 16-bit so that it is compatible with VGA. Input signals to capture logic are Pixel clock, 8-bit data input from camera, V synchronization (VSYNC) and Horizontal reference (HREF). Pixel clock changes on every pixel. For example if sensor is transmitting 1024 768 sized frame following observation can be made. The video frame is of format RGB565 and camera that we are having transmitting 8-bits per pixel clock. This means to transfer one pixel of data 2 pixel clocks are required. Horizontal synchronization is fired by the sensor after every 1024 2 i.e. 2048 Pixel clocks and Vertical synchronization would be fired by the sensor after the entire frame is transmitted i.e. after 2048 768 i.e. 1,572,864 Pixel clocks. The hardware block responsible for camera interfacing which is a part of FPGA, constantly monitors the signals coming from camera to see if it is transmitting anything.

Figure 3 shows the developed FPGA board with OV5640 camera interface used to perform video processing. System development and power optimization are done with following methods.

- Camera acquires the image frame with simple parallel output interface.
- Camera parameters are processed using PC and FPGA.
- Video Output from FPGA is visualized on VGA monitor.
- Instant accessibility of image frames by

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connecting DDR- SDRAM directly to the FPGA.

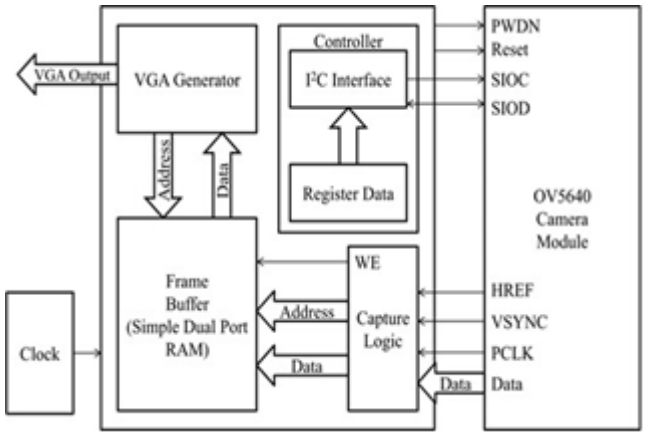

Figure2: Embedded system for camera interface

Figure 3: FPGA board with OV5640 Camera

- Measurement of performance in terms of Number of frames/seconds.
- Power measurement.
- Resource utilization

III. EXPERIMENTAL SETUP

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Text Font of Entire Document Figure 4 shows experimental setup of the developed FPGA based embedded system. The camera controller logic is implemented on the Xilinx FPGA board that consist of device XC6SLX9-2FTG256 Spartan-6 FPGA and a 256Mbit DDR- SDRAM. The FPGA is clocked at 50MHz with peripheral running at 100MHz and 65MHz. The embedded system takes the real time image from camera and sends the captured video frames to the VGA through DDR-SDRAM. This is further suitable for real time video processing. The hardware setup comprises of high feature video camera OV5640 and FPGA board. The necessary control logics are designed using Verilog. Design is synthesized and simulated using Xilinx ISE 14.2 tool chain. The intended system is used to interface peripheral signals of OV5640 camera with appropriate signal pins of FPGA.

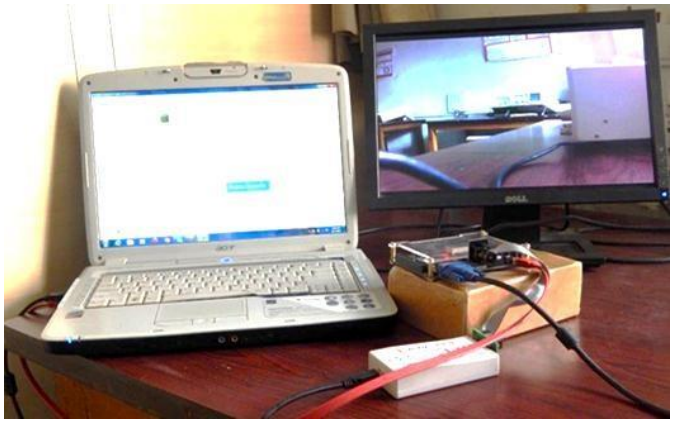

Figure 4: Experimental Setup

IV. RESULTS AND DISCUSSIONS

The detailed camera interface unit is considered for Xilinx Spartan 6 board with XC6SLX9-2TQG144 device. The interface is capable of acquiring videos and images in real time. The designed system is capable of operating with 50MHz frequency. Figure 5 shows video frames captured in real time and final output is presented on VGA monitor. OV5640 camera and VGA monitor is linked with FPGA platform. OV5640 supports maximum up to 5MP image sizes. Figure 5(a) shows frame captured at 100FPS rate. The video streaming to VGA monitor at this frame rate has no performance degradation in run time as compared to video streaming at 20 frames per second. However there are differences in device utilization and power requirements.

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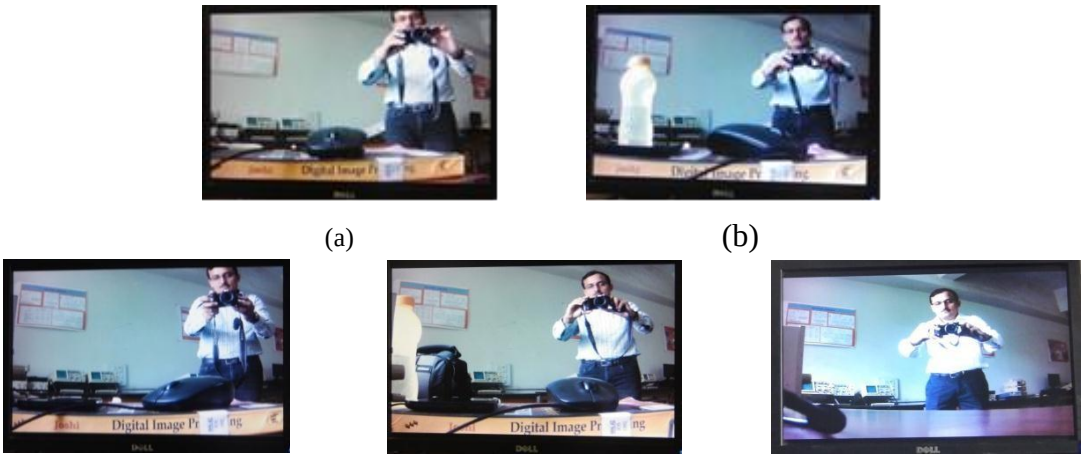

Figure 5: Captured Images with (a) 100frames/s (b)5frames/s (c) 70frames/s (d) 55frames/s (e) 20frames/s

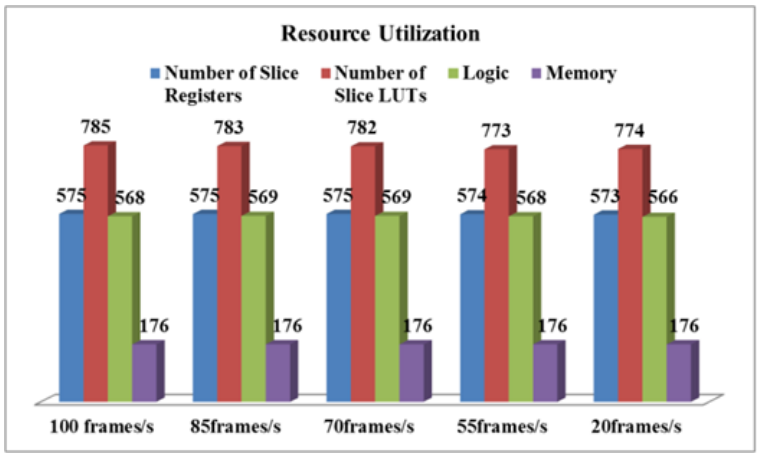

Figure 6:Resource utilization for Spartan-6 for various frame rates

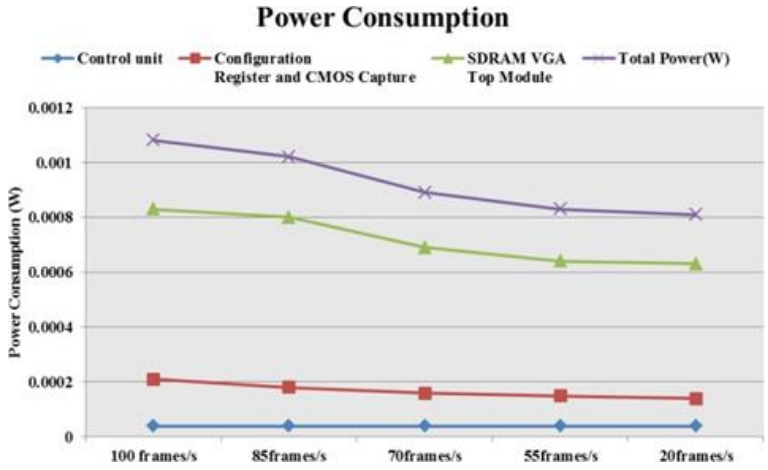

Figure 7: Power consumption for different modules

Resources utilized for developed modules are compared in Figure 6. It shows comparable variations in number of LUTs required for implementing the logic compared to other modules.

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This is because of the increased number of frames per second.

Figure 7 shows power consumption for different modules in system and it shows that as frame rate is decreased power consumption for different modules is also decreased but subjective image quality remains same as shown in Figure 5.

V. CONCLUSION AND FUTURE SCOPE

The implemented system is a functional prototype of architectural realization and implementation of camera interfacing using FPGA suitable for numerous video processing applications. The originality of this effort is in interfacing CMOS camera and FPGA architecture to build intelligent system. The method is based on reducing bottlenecks between camera and processing unit using FPGA reconfiguration and CMOS camera.

The system obtains images of greater quality by means of 5- megapixel camera with OmniBSI technology. Precise frame rate control guarantees the lower power consumption and resource utilization for image and video data. It provides high frame rate up to 100FPS of the system for 1024 768 pixels and provides good quality outcomes as shown in Section V. The blocks of designed scheme are developed in general mode, which means user can modify frame rate and synthesize the project to realize an innovative method.

Extension of this work is to develop a standalone system suitable for applications based on real time video processing and power optimization.

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