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Comparison of various Signal Conditioning Approaches in an IoT based Data Logger

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Abstract

This paper gives brief information about the various signal conditioning approaches that can be used in an IoT based Data Logger. The term signal processing refers to the manipulation of a signal in order to facilitate ease of processing of data in the further stages. The signal processing circuits proposed are used to improve versatility of the product. Generally, data loggers can record and process data only from a set of specific sensors. Using signal conditioning circuits can help expand the scope of sensor outputs that can be given as inputs to the data logger. Output voltages in the range 0-5V and 0-10V are stepped down so that they lie in the range 0-3.3V. The calculations and simulations for the conversion of 0-5V to 0-3.3V using the various approaches are depicted in the paper. A similar procedure can be used to step down 0-10V. After providing the description of said approaches, comparison of these three different signal conditioning circuits is performed and the most resourceful approach is chosen. Conditions with varied loads and varied input voltages have also been covered in this paper. Out of the three proposed approaches, the Buffered Voltage Divider is the ideal solution and has the maximum efficiency.

Keywords: *Data Logger, Signal Conditioning, Voltage Divider, Inverting Amplifier, IoT, ADC.*

INTRODUCTION

This paper emphasizes on the various possible signal conditioning approaches used in a data logger. With the help of a block diagram the paper attempts to give an overview of the entire system and focuses mainly on 3 different signal conditioning approaches.

Figure 1. below shows a versatile data logger using IoT. Unlike conventional sensor specific data loggers, this data logger accepts analog sensor outputs in a particular range as inputs to signal conditioning circuits which convert these voltage levels to a level suitable to the Analog to Digital Converter (ADC) of the microcontroller. From the controller, these signals are further processed and uploaded onto a server and log files are generated which allow the user to analyze when the condition reaches an unacceptable level and make changes accordingly. The reason behind sending the data onto a server is to make it available from any device.

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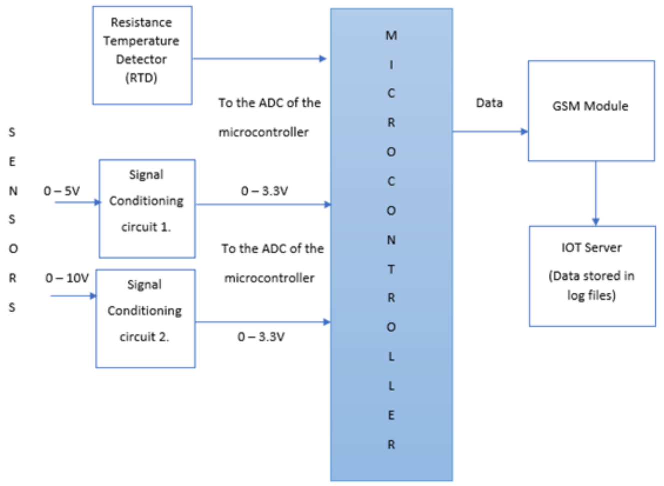

Fig. 1. *Block Diagram of IoT based Data Logger.*

The paper mainly focuses on different signal conditioning approaches. Signal conditioning refers to the manipulation of the signal in order to make it adaptable to the next stage of processing.

LITERATURE SURVEY

Initial Survey of the project involved a comparison of data loggers available in the market to identify the features to be integrated to create an efficient product. The data collected from the sensors is mostly in the numeric form representing the value of required parameter. Comparison of parameters such as number of channels, temperature ranges, sampling rates, logging details, memory and battery life to recognize the ranges that are suitable for a data logger is performed [1-5].

Different sensor outputs need to be passed through different types of signal conditioners in order to make the signal compatible with the controller. Low-voltage analog signals will need to be amplified and subsequently filtered to reduce background noise, prior to digitization. Other sensors may need to be excited by an external voltage to operate [8]. There are various techniques to condition the input signal such as attenuation, amplification, linearization, filtering, isolation, simultaneous sampling etc. [6]. This paper emphasizes on the attenuation technique of signal conditioning.

Attenuation is the process of decreasing the input amplitude of the signal to get it to match with the suitable range of the device digitizer.[8] Since the input voltage ranges dealt with in this paper(0-5V and 0-10V) are greater than the range of voltage suitable to the controller(0-3.3V) decreasing the amplitude of the signal using appropriate resistor networks is performed in the approaches used.

SIGNAL CONDITIONING APPROACHES

The range of the signals obtained from the sensors may differ from that of the microcontroller, therefore changes in these signals need to be made to match it with the voltage levels suitable to the microcontroller. The controller used for experimentation is STM32G070RB from STMicroelectronics. For this data logger the signal has be attenuated to lie within 0- 3.3V, which is also suitable for the ADC of the controller.

1. VOLTAGE DIVIDER CIRCUIT:

A voltage divider circuit is a simple circuit that reduces the amplitude of a signal. The working of this circuit is based on the principle of voltage drop across a resistor. Current is passed through a network of resistors connected in series and the voltage drop across this network is used as the output. In order to match voltage levels of different components this is one of the approaches we can utilise. In the data logger, we needed to match voltage ranges 0-5V and 0-10V with the ADC of the controller, i.e. 0-3.3V.

Considering the case where we require to convert 0-5V to 0-3.3V, it is observed that a simple voltage divider circuit works perfectly in the absence of load. The circuit also works well in the presence of high load to the circuit but a decrease in output voltage is observed as the load is decreased as shown in fig 2(c) and 2(d). The drawback of using this circuit is that it provides lower impedances to the source than analog inputs. They also provide a very high output impedance which makes it unsuitable for multiplexed inputs. Simulations for 0-5V to 0-3.3V for different load conditions are shown in the next section.

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Output Equation:

$$Vout = Vin * \frac{R2}{R1 + R2}$$

2. AMPLIFIER WITH GAIN LESS THAN UNITY:

Operational amplifiers have a very low output impedance and a very high input impedance which means that it does not load down the source. They can therefore overcome the drawbacks of a voltage divider circuit by choosing an appropriate gain value. Input can be given either to the inverting terminal or the non-inverting terminal.

The voltage gain of the inverting operational amplifier is: $Av = -\frac{Rf}{Ri}$

The voltage gain of the non-inverting operational amplifier is: $Av = 1 + \frac{Rf}{Ri}$

From the above equations it is evident that the gain of the non-inverting amplifier can never be less than unity, therefore it cannot be used to step down the voltage level of a signal. Hence the inverting amplifier is used, which produces a 180° phase shift with respect to the input provided at its inverting terminal.

This signal conditioning circuit consists of two parts, the first part acts as an inverting amplifier and the second part acts as an inverting buffer. It is essentially used to change the phase of the acquired output after the first part of the circuit. Hence in the buffer circuit the same values for both the feedback resistor and the input resistor are used.

In the data logger we needed to match voltage ranges 0-5V and 0-10V with the ADC of the controller, i.e. 0-3.3V. Considering the case 0-5V to 0-3.3V, it is observed that the circuit works correctly both in the absence and presence of load. However,

1. VOLTAGE DIVIDER

since this approach utilises 2 operational amplifiers, it makes the circuit bulky.

Output equation:

$$Vout = \left(Vin * \frac{-R2}{R1}\right) * \left(\frac{-R4}{R3}\right)$$

3. BUFFERED VOLTAGE DIVIDER:

To overcome the drawbacks of the above two approaches the buffered voltage divider is used. It is a circuit which combines the simplicity of a voltage divider and ensures the accuracy provided by an operational amplifier.

The voltage divider circuit is attached to a voltage follower circuit, thus providing higher input impedance and lower output impedance due to the presence of an operational amplifier. The addition of the voltage follower isolates the load and the output voltage is dependant only on the values of R1 and R2. It offers a method to transfer a voltage source signal from one impedance level to another without affecting current.

In the data logger, we needed to match voltage ranges 0-5V and 0-10V with the ADC of the controller, i.e. 0-3.3V.

Considering the case 0-5V to 0-3.3V, it is observed that the circuit works accurately irrespective of the value of the load impedance attached.

Output Equation:

$$Vout = Vin * \frac{R2}{R1 + R2}$$

SIMULATION AND RESULTS

The simulations carried out for the three signal conditioning approaches described above are shown below.

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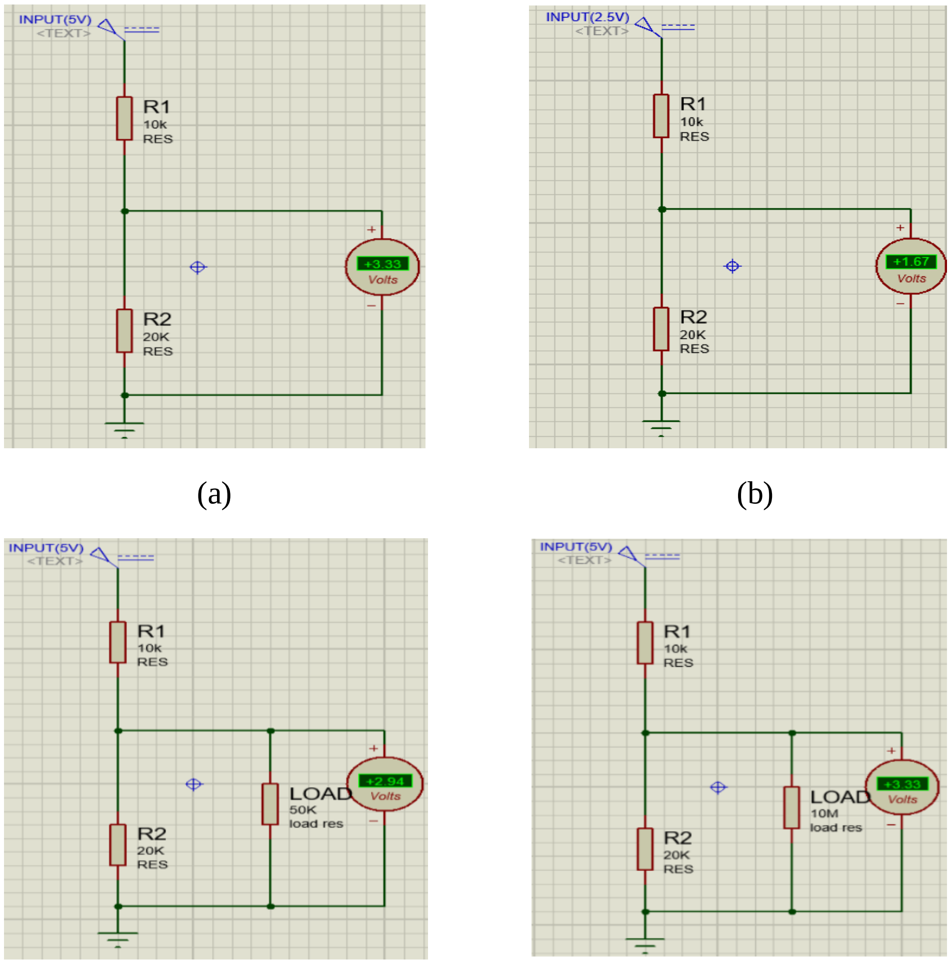

(c) (d)

Fig. 2. Simulation results for voltage divider circuit.

Figure 2(a-d). depicts simulation results for voltage divider circuit under different load conditions. 2(a) displays the no load condition when input is 5V. 2(b) displays the no load condition when input is 2.5V. 2(c) and 2(d) display the output acquired in the presence of different loads. After experimentation and simulation, it is observed that the voltage divider circuit works perfectly for no load and higher load values whereas the output keeps on decreasing as the value of load decreases. The values of the resistances used in the above simulations are R1 = 10K and R2 = 20K. Similarly, for the 0-10V to 0-3.3V resistance values used are R1=20K and R1=10K.

Table 1: *Analysis of output voltage with different loads.*

Input Voltage	Value of Load	Output Voltage
5V	100M	3.33V
5V	10M	3.33V
5V	1M	3.31V
5V	100K	3.12V
5V	50K	2.94V
5V	20K	2.50V
5V	10k	2.00V
5V	5K	1.43V
5V	1K	0.43V
5V	NO LOAD	3.33V

2. AMPLIFIER WITH GAIN LESS THAN UNITY

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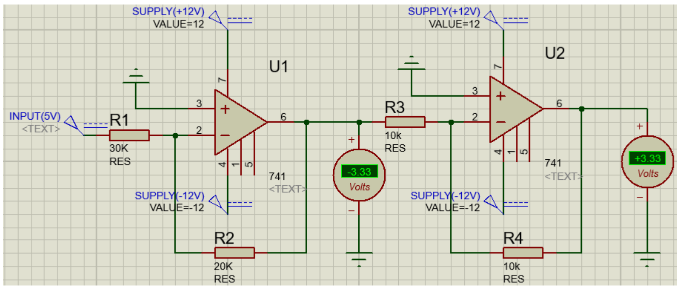
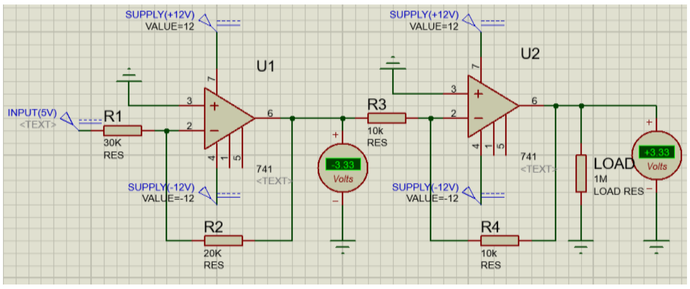
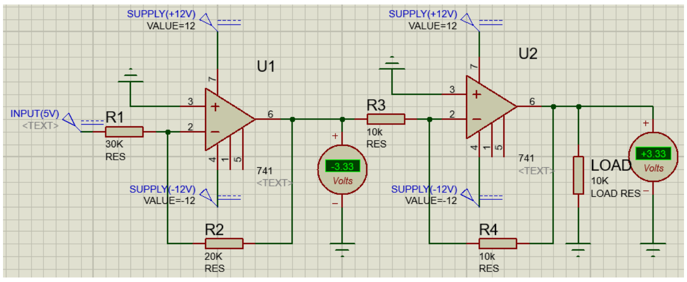


(a)



(b)

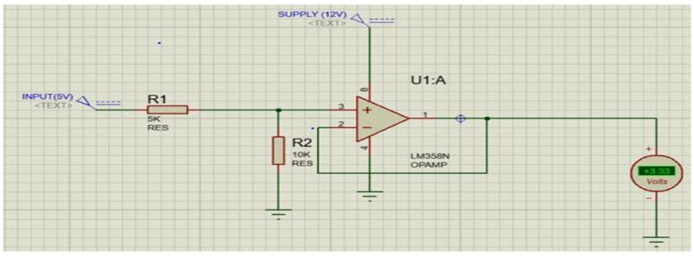


(c)

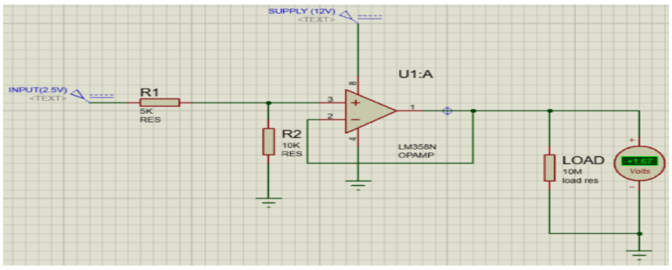
Fig. 3. *Simulation results for the inverting amplifier with unity gain circuit.*

Figure 3(a-c). depicts simulation results for the inverting amplifier with less than unity gain circuit under different load conditions. 3(a) displays the no load condition when input is 5V. 3(b) displays the output when a 1M load is applied to the circuit. 3(c) display the output when a 10K load is applied to the circuit. After experimentation and simulation, it is observed that the circuit works and provides the right output irrespective of the value of the load applied. The values of resistances used in the above simulations are R2 = 20K and R1 = 30K. Similarly, for the 0-10V to 0-3.3V resistance values used are R2=10K and R1=30K.

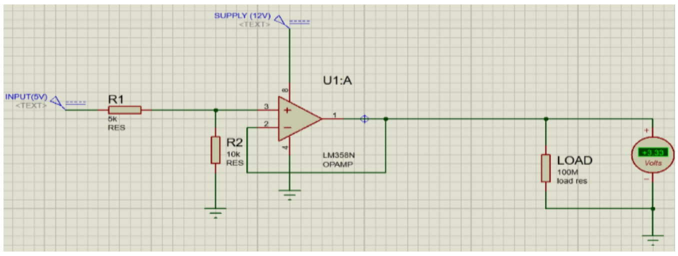
3. BUFFERED VOLTAGE DIVIDER



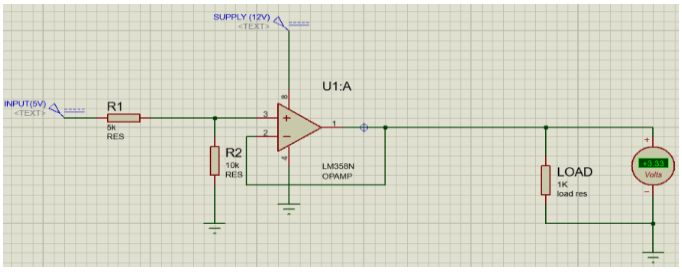
(a)



(b)



(c)



(d)

Fig. 4. *Simulation results for the buffered voltage divider circuit.*

Figure 4(a-d). depicts simulation results for the buffered voltage divider circuit under different load conditions. 4(a) displays the no load condition when input is 5V. 4(b) displays the condition when input is 2.5V and the load is 10M. 4(c) and 4(d) display the output acquired in the presence of different loads. After experimentation and simulation, it is observed that the buffered voltage divider circuit works perfectly and displays the correct output irrespective of the value of the load applied on it. The values of the resistances used in the above simulations are R1 = 5K and R2 = 10K. Similarly, for the 0-10V to 0-3.3V resistance values used are R1= 10K and R1=5K.

Table 2: *Analysis of output voltage for different input voltages for the 0-5V to 0-3.3V circuit.*

Input Voltage	Value of Load	Output Voltage
0V	10M	0V
1V	10M	0.66V
2V	10M	1.33V
2.5V	10M	1.67V
3V	10M	2V
4V	10M	2.67V
5V	10M	3.33V

Table 2. shows the output voltages observed in both, the inverting amplifier with unity gain approach and the buffered voltage approach.

CONCLUSION

Experimentation and simulation were carried out for three different signal conditioning approaches, at different input voltage values as well as varied loads for an IoT based Data logger. After analysis of the results and simulation it can be concluded that the buffered voltage divider proves to be the best amongst the three approaches. It is accurate, less complex and not a bulky circuit. The inverting amplifier with less than unity gain approach is accurate as well but is bulky because of the presence of two operational amplifiers. The simple voltage divider circuit is a small, compact option that can be used in the absence of load or in the presence of very high loads, above 10M ohm.

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