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January - February 2020
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Random Discrete Dopant Induced Variability in Gate-All-Around Si-Nanowire FETs

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Abstract

This paper shows, random discrete dopant distribution effects on the Si (NW-FETs) are studied using three-dimensional, quantum-correction included density-gradient "atomistic" simulations. Effects of the random dopant fluctuation due to the dopant number and their distribution in the channel are investigated. Using threshold voltage fluctuation (as a parameter) due to dopant number fluctuation, we examine four figures of merit of the nanowire transistor: a) subthreshold slope; b) threshold voltage; c) ON/OFF-switch; and d) DIBL. The predicted variability in threshold voltage may help design of integrated circuits using silicon nanowire transistors.

Keywords: *Random Discrete Dopants, Variability, quantum confinement, drift diffusion, technology computer aided design, drift diffusion, NW-FET, RDD, RDF.*

I. INTRODUCTION

The MOSFET (metal-oxide-semiconductor field effect transistors) is the most important part for the evolution of integrated circuits. Recent switching over from the planar MOSFET structures to non-planar 3-D FinFET architectures reported by Intel in 2011 in the 22nm technology node, have reached to 14nm technology node in 2014 [1]. Nanowires are now considered as potential candidates for further miniaturization of MOSFETs in order to reach the 7 or 5nm technology nodes, because of their advantageous geometry as well as their physical and electrical characteristics, in particular, the possibility to implement gate surrounding the entire channel for better electrostatic control [2]. Gate-all-around nanowire with superior gate controllability are being explored. [2, 3]

The surrounding gate around MOSFET, wherein the conducting channel is encompassing through gate, the electrostatic control is maximum, confining the flow of carriers & thus minimize the effects of short channel. GAA-NW FETs have the most optimized gate structure than the tri-gate FinFETs. The key performance metrics for a transistor are: the drain current, drain induced barrier lowering, threshold voltage, and the sub-threshold slope. In any case, as an extraordinary multifaceted nature is engaged with

January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

the creation of transistors in cutting edge innovation hubs, vacillations in the electrical parameters of the transistors are normal, which is known as changeability.

Studies have shown that the increasing the gate number, a better immunity against the effects of short channel isobtained. Thus, a nanowire structure is the ideal for the continuity of Moore's law.

As the devices are scaled down, the source/drain (S/D) extension region requires a very sharp doping profile over only a few nanometers [4, 5]. Although nanowire channels are low-doped or even unlopped, the Source/Drain area is highly doped. When the incapacitatingdeliberation is 1×10^{20} $cm^{-3,}$ there could be only two dopants [6]. Nanowire transistors are extremely susceptible to random dopant fluctuations and interface roughness induced variability. In addition to that, the dopants diffused from drain side has more influence on the characteristics of the FETs than from the source side [7].

From transistor performance point of view the current in the OFF state must be minimal in order to decrease the standby power. On the other hand, the current in the ON state must be maximum since it is inversely proportional to the switching time. As a consequence, serious variability issues such as, random discrete dopant fluctuation comes into play in nanowire transistors, leading to detrimental effects on the electrical characteristics. As the channel dopant distribution leads to significant fluctuations ON/OFF ratio, detail knowledge of theirchannel position are critical to the fundamental understanding of the nanowire performance.

Suzuki et al. [8] have reported consequences of RDFupon I_{ON} for dopants incorporation from the source region using the ensemble Monte Carlo/molecular dynamics simulations. Mori et al. [9] have reported on the fluctuations of ultra-small Si nanowire transistors characteristics because of RDD, where RDF is random dopant fluctuation and RDD is random discrete dopants. Therefore, the discrete dopant investigation impact from the drain side into the channel on various electrical parameters needs to be taken up.

In general, the channel regions of nanowire FETs, are undoped (or lowly doped) and therefore, random dopant fluctuation is reduced. However, in NW-FETs the diffusion of dopants from almost fully incapacitatedsource/ drain zone into its addition and ultimately the result is RDF in the channel [10, 11]. Accordingly, variability due to RDF needs to be considered as a major technology issue during the design of nanowire transistors. This paper explores using the technology CAD tools, the consequences of different incapacitated features of nanowire FETs in 7nm technology node.

As the dimensions of the device is reduced to nanometer regime, carriers are considered as quantum entities at atomistic scale. Since it cannot be approximated due to conventional drift-diffusion, the complex numerical method is used. Several workers [12-15] have reported results on detailed 3-D simulation studies using numerical analyses of NW-FET. Including drift diffusion carrier transport, several authors have simulated Si GAA NW-FET electrical characteristics. Several authors have also examined the major performance metrics for the three transport directions [100], [110], and [111]. Martinez et al. [16, 17] have reported the variability in Si Nanowire MOSFETs studied using a full 3-D NEGF simulation. Si nanowire field-effect transistor ultimate scaling depends on the crystal orientation and cross-sectional size and have been studied by Luisier and Szabó [18] using a full-band and atomistic simulation.

In this paper, the consequences of RDD from drain last part & variability dependence upon the channel length and cross-section of NW-FETs are studied using the extended atomistic quantum corrected drift-diffusion simulator, MINIMOS-NT [19]. We present a statistical analysis of discrete dopant

January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

induced intrinsic figures of merits such as, a) subthreshold slope; b) threshold voltage; c) ON/OFF current; and d) DIBL of nanowire FETs.
The paper is arranged as follows: TCAD calibration is given in Section II. Device structure and the imitationis described in middle section i.e. III. Further in Section IV shows the features of impact of doping variations from first side , wherein first side is drain side upon data which represents action, abilities and quality, for example, the on or off ratio of current, DIBL and GAA Si NW-FETs threshold slope. The conclusion is given in Section V.

II. Technology Cad Calibration

To comprehend, describe, and designing of Si process, TCAD requires constant alignment of design constraints. It additionally requires the prescient scope of any procedure displaying capacity which can shift essentially between process designs. To be "prescient" TCAD wants to have an extremely elevated level of precision. Even legitimate alignment required for prescient TCAD is troublesome. It is necessary to check the presumptions in both the procedure and the gadget test systems, just as the electrical estimations for legitimate alignment.
Towards TCAD adjustment, a 22-nm GAA-NW experiments [20] has been demonstrated first and afterward it downsized to 10-nm length related to gate in this paper. Fig 1. Shows a correlation of reenactment and test ID-VG plot at a VD of 0.05 V for the 22nm GAA-NW. At the electrical adjustment organize the portability models executed in the TCAD gadget recreation device have been tuned to test information related to the distributed versatility models. It has been seen that at a low channel voltage of 50 mV and at entryway voltage more prominent than 0.4 V, the reproduced current match is superb with the exploratory information for 22nm length related to gate.
The Poisson condition and the coherence conditions for the gaps and electrons are remembered for the drift dissemination model. The principle impediment of utilizing the fundamental drift dispersion model is that it doesn't take quantum impacts, similar to the wave idea of electrons. The computationally concentrated expense of a highly quantum portrayal of charging transport (for instance, NEGF) is also computer resource intensive. A compelling option is an alteration for the old-style DD model to incorporate the impacts of quantum mechanics. The demonstrating of gadgets by TCAD regularly portrays the dissemination of transporters. In a nanowire transistor, bearers are kept one way. This influences the outspread bearer thickness, just as the thickness of states, causing the event of sub-groups. The impacts of quantum constrain are reproduced utilizing the self-predictable coupled Schrodinger Poisson model.

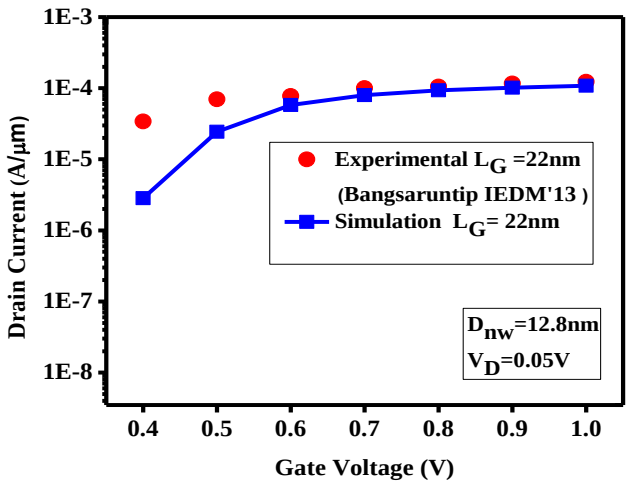


Fig. 1: Examination of reproduction and test I_D-V_G plot at a V_D of 0.05 V for a 22nm GAA NW [20].

III. Device Structure And Simulation Environment

The device performance has been improved by scaling down the device and fabrication cost has been reduced by it.The unintended short channel effects has been induced by scaling down the devices or gadgets. A gadget will be free of short channel impacts if the gate length is made at any

January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

rate 4 to multiple times longer than the common length. Additionally short divert impacts in MOSFETs can be limited by diminishing the gate oxide thickness and expanding the dielectric steady of the gate oxide. The execution of GAA nanowire FET can be improved by the enhancement of the gadget scaling. The short channel impact invulnerability of nanowire FET can be quantitatively examined by utilizing the characteristic length λ and is utilized to break down the insusceptibility towards the short channel impact of nanowire FET. It has been derived from Poisson's equation as [21]:

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{8\varepsilon_{ox}} t_{Si}^2 \ln\left(1+\frac{2t_{ox}}{t_{Si}}\right)+\frac{{t_{Si}}^2}{16}}$$

Where the permittivity of Silicon is presented by ε_{Si}

The permitivity of oxide is presented by ε_{ox}

The thickness of Silicon is presented by t_{Si}

The oxide thickness is presented by t_{ox}

Towards the nanowire design, for simuation study a cylindrical-shaped gate-all-around nanowire FET is used. The dopants which are present within the channel region, has been considered discretely. The doping concentration of S/D is 1 X 10^{20}cm $^{-3}$. To include randomness in the position and discrete dopants number, the desired dopants number in cylindrical nanowire are generated. Discrete dopants are factually put in the 3-dim circular channel zone forexamining the characteristic fluctuations in device performance concurrently capturing both the dopant focus variety and dopant position change impacts [22, 23].

Attributes of all discrete dopantfluctuation in thegadget are assessed by comprehending a lot of 3-D quantum–mechanical correction equations included in density gradient model. Basic three-dimension "atomistic" float dissemination test system MINIMOS-NT [19], with thickness slope quantum amendments, is used to simulate statistically distributed discrete dopants. Device simulations are performed to analyze the potential profile and the fluctuations in the threshold voltage in acylindrical-shaped gate-all-around nanowire FET nanowire at 7nm technology node.

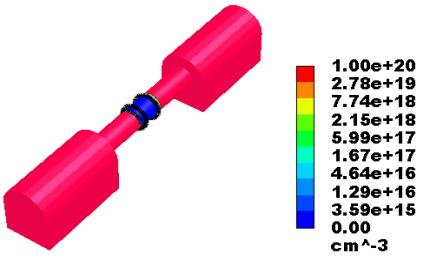


Fig. 2: Cylindrical Si nanowire device structure used in simulation showing the net doping profile.

Figure. 2represents a nanowire along with net doping profile. The devices in this study is doped with 1.0×10^{16} cm^{-3}. The S/D regions are doped with 1.0×10^{20} cm^{-3}. The device has a gate length of 10nm with p-type doping (~10^{16} cm^{-3}), and has a diameter of 6.8nm. The parameters of the imitated nanowires are shown below.

TABLE I .PARAMETERS OF THE IMITATED NANOWIRES.

Parameters of Nanowires	Value
Channel Diameter	6.8nm
Channel Length	10nm
Channel Doping	10^{16} cm^{-3}
Source Drain Doping	10^{20} cm^{-3}
Oxide thickness	0.5nm
High–k thickness	1.5nm

Quantum corrected density gradient model has been used for simulation purposes. The following

TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

3-D DG relationships [19] have been used in simulation:

$$div\,(\varepsilon\,.grad\,\psi) = q\,.(n - p - C)(1)$$

Here, ψ represents the electrostatic potential, n represents the electron concentration, concentration of hole is presented by p, total ionized dopants concentration is presented by C,permittivity is presented by ε, and the charge of electron is presented by q. The distribution of potentialis affected as a results which affects the carrier distribution. The e^- current density is :

$$div\,J_n = q.(R + \frac{\partial n}{\partial t})$$

(2)

Here, J_n= e^- current density,
R = net recombination rate, and
n=Electron concentration.
The current for electron and holes are given by the following relations:

$$J_n = q\,.\mu_n\,.n.\left(grad\left(\frac{\varepsilon_C}{q} - \psi - \gamma_n\right)\right) + \frac{k_B\,.T_L}{q}.\frac{N_{c,0}}{n}\,.grad\left(\frac{n}{N_{C,0}}\right)(3)$$

Herek_B=Boltzmann constant,
T_0 = reference temperatureat reference temperature,
$N_{C,0}$ = effective density of states for electrons evaluation,
ε_C= local band edge energy,
T_L= local lattice temperature,
μ_n= electron mobility, and
ψ= electrostatic potential.
The quantum correction potential $\gamma_n$is given by

$$\gamma_n = \frac{\hbar}{12\,.\,\lambda_n\,.\,m_0}\,.div\;\;grad\frac{\psi + \gamma_n - \frac{\varepsilon_C}{q}}{k_B\,.T_L}(4)$$

Here,$\hbar$= Planck's constant,
T_L = local lattice temperature.

IV. Results And Discussion

In this paper the study has been performed for seventy different ensembles channel discrete dopants which differ from each other due to the dopant variability. However, the typical dispersal of different dopants have been shown in figure 3. The dopants are mainly distributed at the drain extension and the channel regions. As the drain extension region is highly doped (1.0×10^{20} cm^{-3}) than the channel (1.0×10^{16} cm^{-3}) the dopants from drain extension region diffuse towards the channel. . At the point when the quantity of discrete dopants of channel changes, the proportional centralization of channel doping also changes as a results of which potential distribution changes and threshold voltage fluctuation is induced [22, 23].The impact of discrete dopants near drain side of the nanowire are reported below.

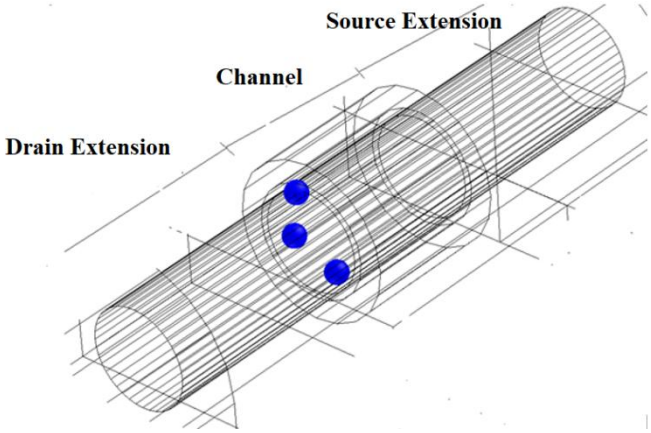


Fig. 3: Discrete dopant distribution for one configuration. Only 3 dopants are considered in simulation.

The impact of increase in diameter on I_D-V_G plot is shown in fig 4. From fig4, it is seen that with increase in diameter the drain current increases. Increase in diameter leads to increase in area and drain current increases. The variation is shown in fig 5. With increase in drain voltage, the inversion charge density increases as a result of which drain current increases.

January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

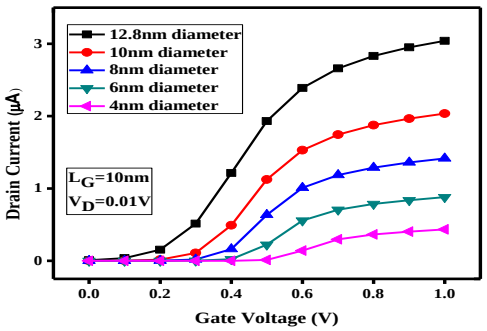


Fig. 4: I_D-V_G plot of Si nanowire at room temperature.

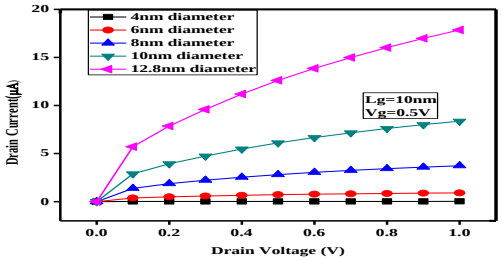


Fig. 5: I_D-V_D plot of Si nanowire at room temperature at V_G =0.5 V.

Whenmajority carriers of the discrete dopants trap, the portable electron focus has been diminished. It prompts a sharp Coulomb potential creation bringing about limit voltage variance. Appropriately, discrete charges are taken care of by appropriately presenting the quantum corrections in simulation. The amount of threshold voltage fluctuation depends on the dopant number as well the dopant position in the channel. Fig. 6 shows the potential associated with individual dopants in the nanowire without ((a) and (c)) and with ((b) and (d)) discrete dopants. It is observed that the potential distribution in the center of nanowire is maximum in comparison to periphery (Fig. 6(a) due to quantum confinement effect). However, the potential is maximum in the region of discrete dopants (Fig. 6(b)) and the potential distribution does not vary significantly. The potential associated with the discrete dopants are maximum than the potential without discrete dopants. Along with it the transfer characteristic of GAA-NW is shown in figure 7 with discrete dopants for seventy different configurations for (a) V_D=0.05V and (b) V_D=0.7V.

The variation of drain current for seventy different configuration is shown in figs. 7(a) and (b) for two different drain bias. It can be clearly seen from Figs. 7 that in presence of these discrete definitely helps in reducing the drain current dopants because of Coulombic interaction between the dopants. It may be noted from Fig. 7 that the deviation in drain current is more at low drain voltage than at higher drain voltage.

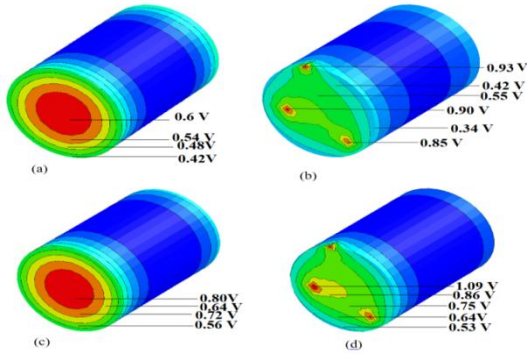
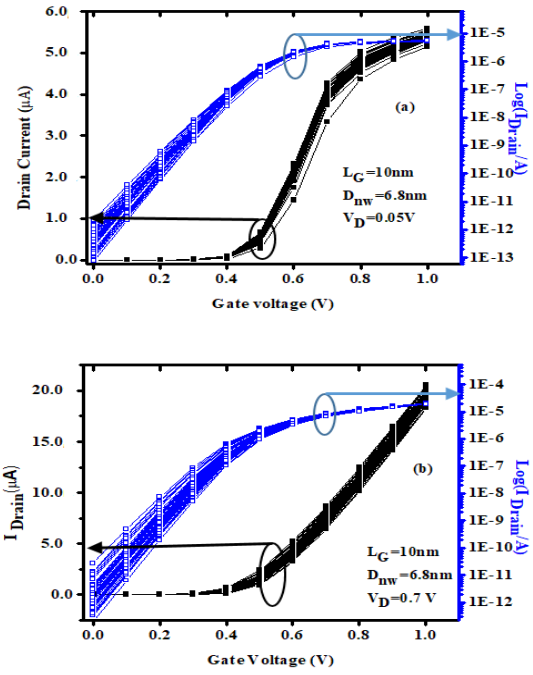
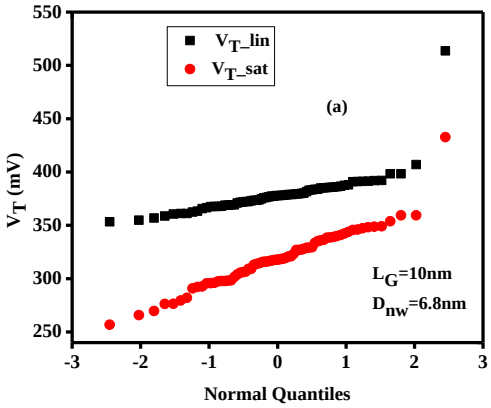


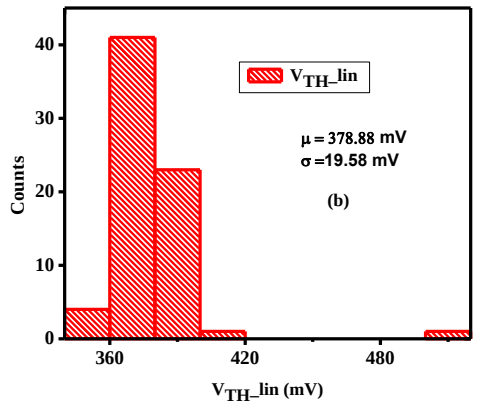
Fig. 6: Potential distribution (a) and (c) without discrete dopants (b) and (d) with discrete dopants near drain side for one (3 dopants) configuration at V_D= 0.05V and 0.7 V, respectively.



January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

Fig. 7: I_D-V_G plot of nanowire for seventy different configurations for random discrete dopants near drain side at two different drain voltage (a) V_D=0.05V and (b) V_D=0.7V.





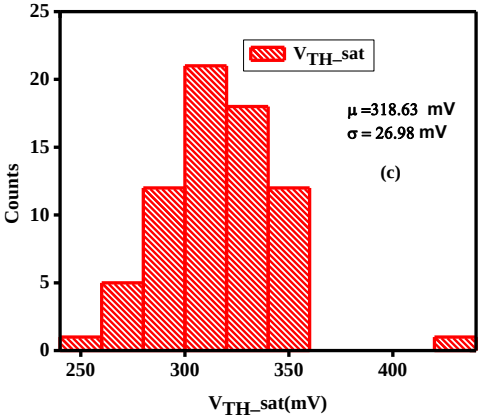
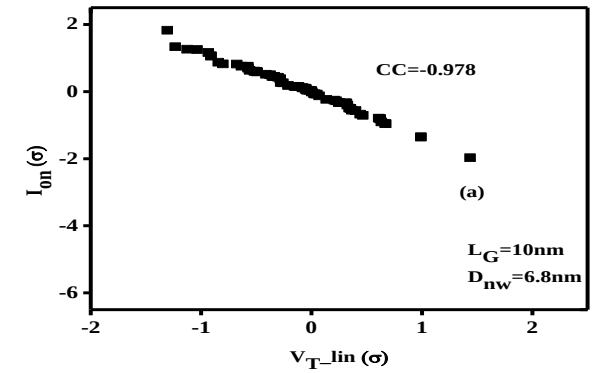


Fig. 8: (a) The Q-Q test on V_T distribution due to random discrete dopants in the channel at V_D=0.05 V and 0.7 V respectively, (b) Histogram plot of V_{TH}_lin at a drain voltage of 0.05 V, and (c) Histogram plot of V_{TH}_sat at a drain voltage of 0.7 V.

According to fig 8(a), it is seen that the distribtion of V_T is deviating more from normal distribution at lower drain bias. V_{TH}_lin histogram has higher value of kurtosis than the V_{TH}_sat histogram plot. Both the histogram plots have positive value of skew. So the distribution of V_T_lin is highly away from normal distribution. The variation of I_{ON} with threshold voltage is prsented in figure 9.



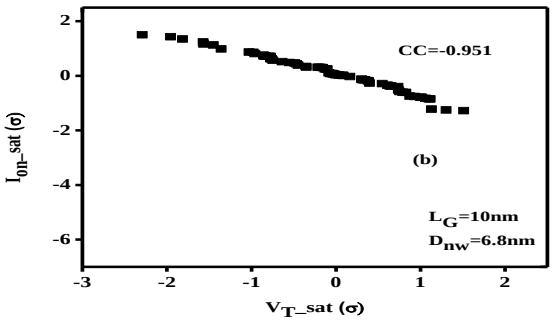


Fig. 9: Scatter Plots of I_{ON} versus threshold voltage for seventy different configurations for (a) V_D=0.05V and (b) V_D=0.7V.

From fig 9, it is seen that there is a poor correlation between I_{ON} and V_{TH}. The variation in on current occurs because of variation in threshold voltage, current onset voltage and G_m. The variation contributed by G_m is negligible in this case. The variation contributed by current onset voltage is negligible due to intrinsic channel. So the variation in on current occurs due to variation in source access resistance which leads to the variation in

January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

effective gate source voltage. The effect of on/off current is shown below (fig10).

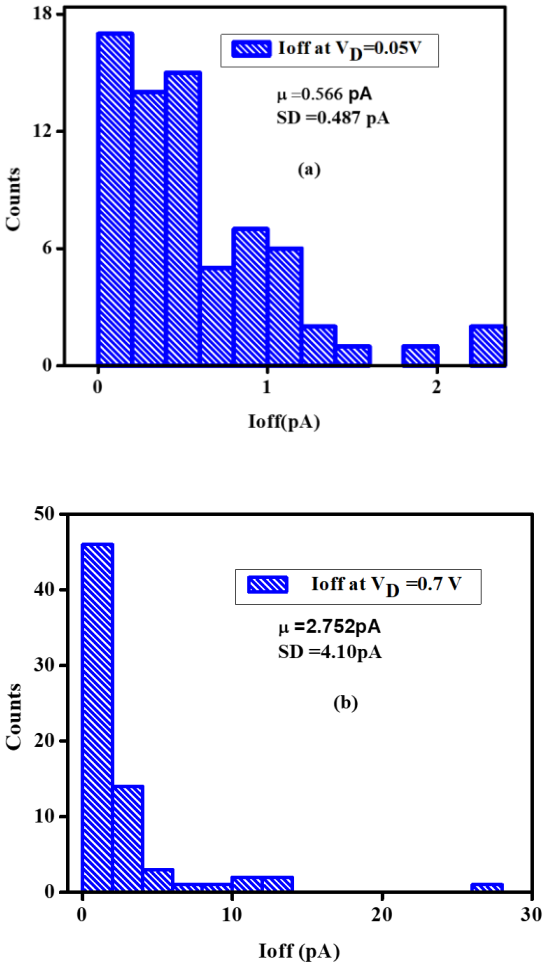


Fig. 10: Histogram of $I_{off}$for seventy different configurations for (a) V_D=0.05V and (b) V_D=0.7V. SD stands for standard deviation.

I_{off} in linear region is found to be 0.566pA and SD is found to be 0.487pA. The mean of I_{off} is found to be 2.572pA and SD is found to be 4.10pA at a drain voltage of 0.7 V. The skew in both the drain bias is found to be positive .The kurtosis value is higher at a drain voltage of 0.7 V than at a drain voltage of 0.05 V. The histogram of I_{off} at higher drain bias is highly away from normal distribution. The effect of these dopants on SS is shown in fig 11.

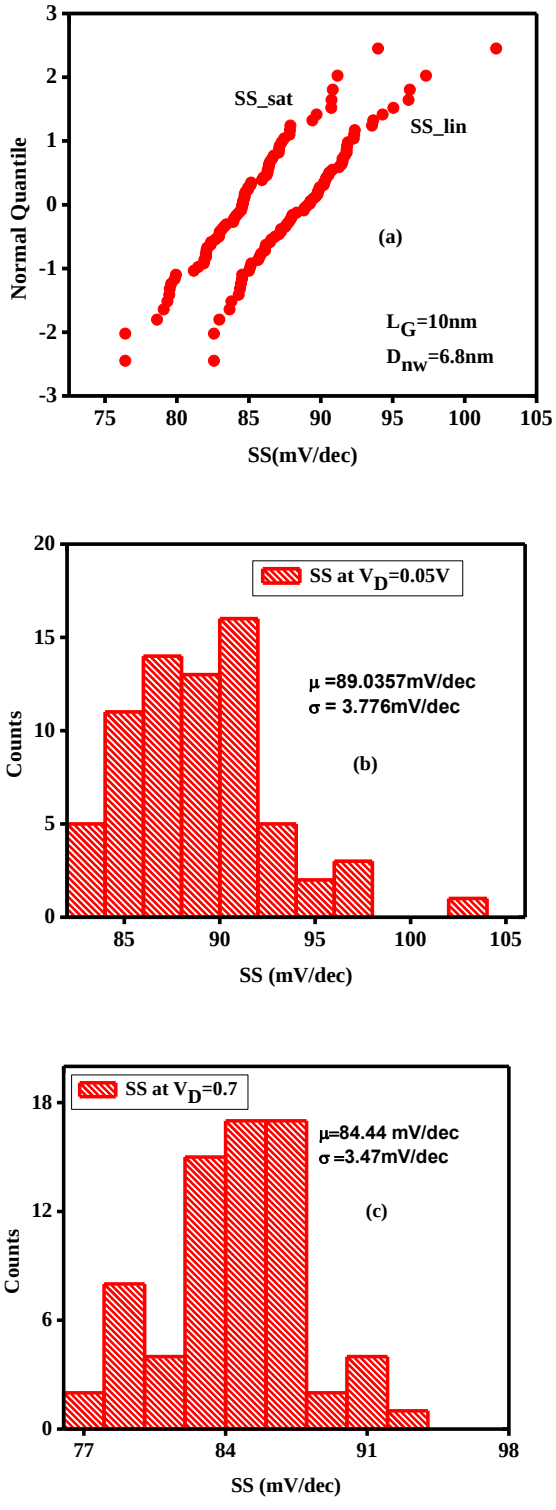


Fig. 11: (a) Q-Q plots of SS for seventy different configurations for V_D=0.05V and V_D=0.7V, (b) Histogram plot of SS for seventy configurations for V_D=0.05V, and (c) Histogram plot of SS for seventy configurations for V_D=0.7V.

TEST Engineering & Management

January - February 2020
ISSN: 0193 - 4120 Page No. 2409 - 2418

From figure 11(a) it may be noted that QQ plot indicates the skewness in the distribution. The skew and kurtosis are found to be 0.674 and 1.042. The SS mean in linear region is found to be 89.035mV/Dec and standard deviation is found to be 3.77mV/Dec. The mean of SS is found to be 84.44mV/Dec and SD is found to be 3.14mV/Dec at a drain voltage of 0.7 V. In both drain voltage, the skew is found to be positive.The kurtosis value is higher at(drainvoltage) 0.05 V than 0.7V. The QQ plot of DIBL is presented in fig 12.

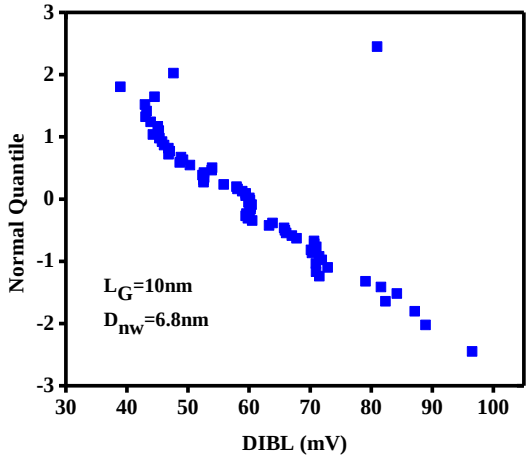


Fig. 12: Q-Q plots of DIBL for seventy different configurations.

Fig. 12 shows the DIBL variation in the presence of discrete dopants near drain end.The variation in DIBL occurs due to asymmetry in potential distribution between source and drain.

V. Conclusion

Due to the rapid scaling of nanowire transistors into the deep sub-nanometer regime, statistical variations and quantum effects cannot be neglected any more. This paper presents a comprehensive methodology for variability prediction including TCAD calibration of GAA nanowire transistors when RDD is present. To the best of our knowledge, impacts of discrete dopant fluctuations from drain end into the channel are being reported for the first time.The reproductions is done by utilizing a three-Dimension DG reenactment approach that joins quantum adjustments. The Fermi–Dirac measurements is utilized to precisely demonstrate intensely doped Source/Drain. Simulations have been performed in presence of relatively small doping levels of DRD (discrete random dopants) in cylindrical-shaped gate-all-around Si-nanowire FET to study the variability.

The key findings of this study indicate that a GAA NW-FET with relatively small doping level in channel show better DC characteristics and good immunity to threshold voltage fluctuation. Variations in $V_{th,}$ ON current, DIBL, SS and OFF current have been investigated. As drains electric field is higher, the variations in all parameters (I_{ON}, I_{off}, SS, and DIBL) are found to be higher.

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January - February 2020
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