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Design of Parallel Pipelined DIF- FFT Architecture

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Abstract
To compute the Discrete Fourier Transform a formal procedure for designing FFT architectures using folding transformation and register minimization technique. This research work presents a new approach to develop parallel pipelined 128 points Radix2[3] Real Fast Fourier Transform (RFFT) and Complex Fast Fourier Transform (CFFT) architecture. The area, frequency, throughput, delay and power consumption can be reduced in the parallel pipelined by using RFFT & CFFT architecture. The power and area consumption can be reduced in parallel pipelined by using RFFT & CFFT architecture. The output samples are obtained, to a desired order to implement on XILINX Virtex-4Xc4vfx12 FPGA.

Keywords: *Fast Fourier transform (FFT), Parallel Pipelined, RFFT, CFFT, Radix2[3]*

1. Introduction

FFT algorithm can be used to obtain the spilitted sequence of frequency or in time domain analysis. Parallel pipelined architectures designed based on these algorithms for various radixes. The parallel architectures assume the input signal has to be real values. An increased number of parallel architecture with various values of an input signals in the analysis of FFT for real and complex. In signal processing the real valued signal are most importance to reduce the computation complexities.

2. Radix-2 DIF-FFT

The Decimation In Frequency-DIF FFT method separates the given input sequence that produced decimated output.

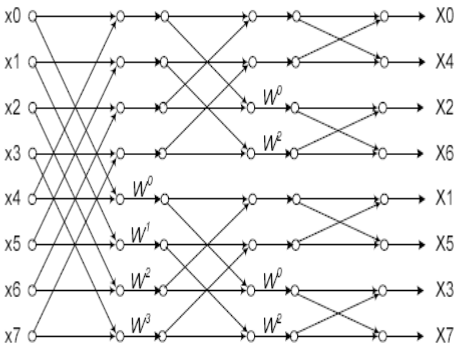

Figure 1: Flow graph of a8 point radix-2 sequence

The following equations are DFT algorithm

$$X[2n]=\sum_{n=0}^{\frac{L}{2}-1}\left(x[l]\,x\left[l+\frac{L}{2}\right]\right)e^{-\frac{j2\pi ln}{\left(\frac{L}{2}\right)}},\quad n=0,1,\ldots\ldots\frac{L}{2}-1 \qquad (1)$$

$$X[2n+1]=\sum_{n=0}^{\frac{L}{2}-1}\left(x[l]-x\left[l+\frac{L}{2}\right]\right)e^{-\frac{j2\pi}{Ll}}e^{-\frac{j2\pi nl}{\left(\frac{L}{2}\right)}},\quad n=0,1,\ldots\ldots\frac{L}{2}-1 \qquad (2)$$

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Applying the above equation continuously that leads to produce into 2-point, 4-point and 8-point DFTs.

3. Radix-2^2DIF-FFT

The above two stages of computation, twiddle factors W_N^{nk} multiplier are used to form a 2-point, 4-point, 8-point radix architecture. The next level of computation can be radix-2^2 with the help of FFT algorithm. Fig. 2.shows the butterfly architecture of L= 16 point flow graph sequence according to separation of sequence in DIF FFT method.

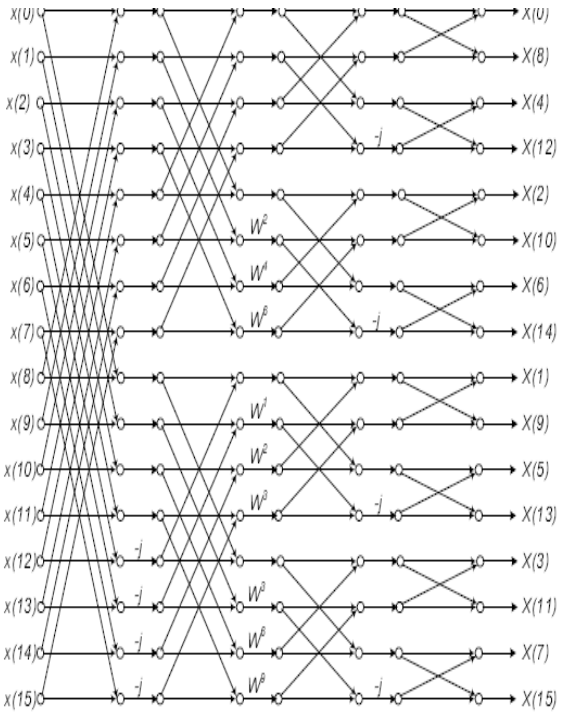

Figure 2: 16-point radix-2^2 DIF FFT butterfly flow design

The flow graph represent in each stage have same multiplication operation done with the help of the twiddle factor.

4. Parallel Radix-2^2Architecture

The DIF FFT algorithm is used to design with various input samples for parallel pipeline architecture realization is made easy. We can design the architecture with Radix-2^2 by simply use the Single-path Delay Feedback (R2^{2}SDF) approach with just replace the first butterfly stage into real value signal. But, this method easy way to find the output samples with the help of algorithms of the FFT, where almost half of the output samples are obtained.

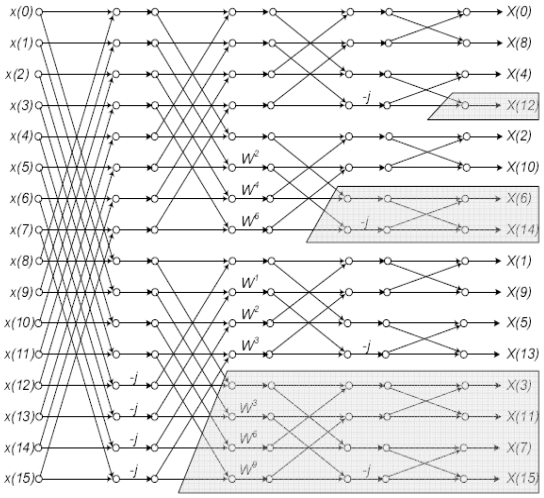

Figure 3: Flow graph of a 16-point radix-2^2 DIF FFT.

The boxed regions are redundant operations for decimation in frequency RFFT. These types of architectures are designed using two types of scheduling approaches.

5. Scheduling Type 1

The proposed butterfly flow graph of 16-point radix-2^2architecture shown in Fig. 4. The nodes from *P*0,*P1* ...*P7* represent first stage of the FFT and *Q*0,*Q1* ...*Q7* represent the second stage and *R*0,*R1*...*R7* represent third stage of the FFT *S*0,*S1* ...*S7* represent Last stage of the FFT. This radix-2^2feed forward method involves the reduction of computation that produces 2 outputs. In this type of assumption is only valid for the RFFT case due to the redundant operations.

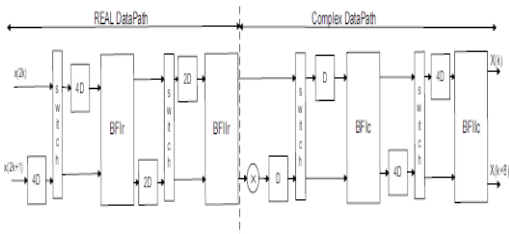

Figure 4: Proposed 2-parallel 16-point radix-2^2 DIF RFFT.

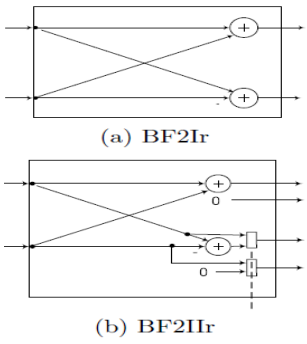

Figure 5: a&b real data path of BF2Ir and BF2IIr

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The architecture design of the flow graph uses four types of butterflies. BF2Ir and BF2IIr are real data path butterflies respectively as shown in Fig 5.

The complex multiplicative factor "*-j*" used in the flow graph, the real-valued data path are consists of first two stages only. The next stage of the architecture can be designed based on the real and complex values.

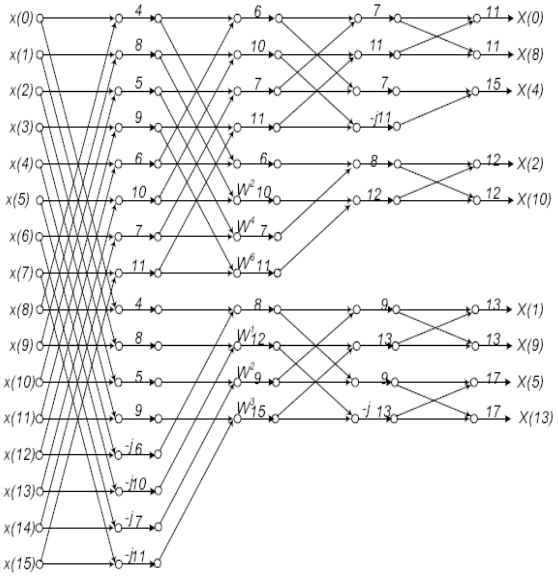

Figure 6: Simplified flow graph of a 16-pointradix-2^2 DIF RFFT

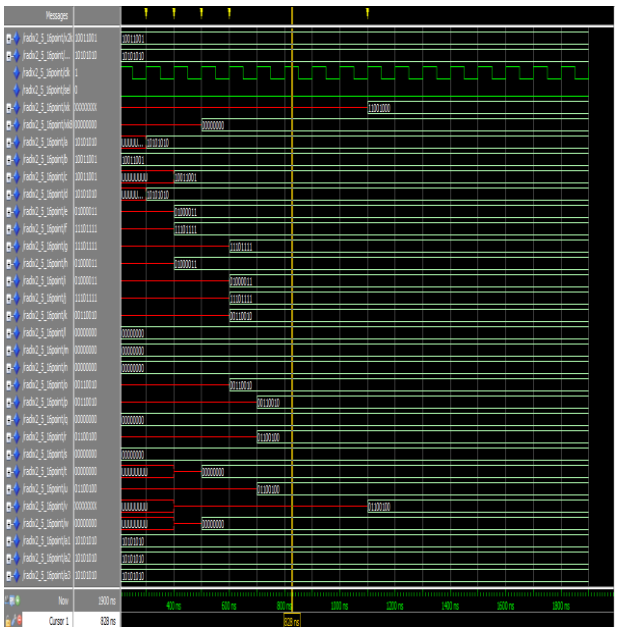

Figure 7: 16-point radix-2^2 DIF RFFT scheduling Type 1 output

6. Scheduling Type 2

Nexttype of scheduling is proposed 2-parallel pipelined architecture. In this type of schedulingthe input signal sequence is processed orderly.

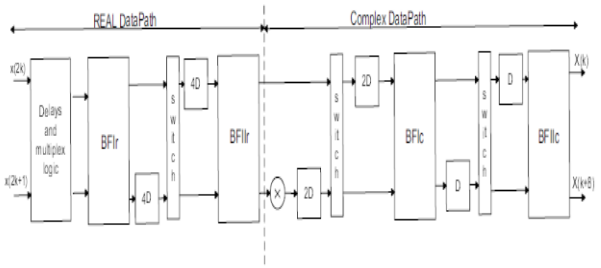

Figure 8: 16-point radix-2^2 DIF RFFT.

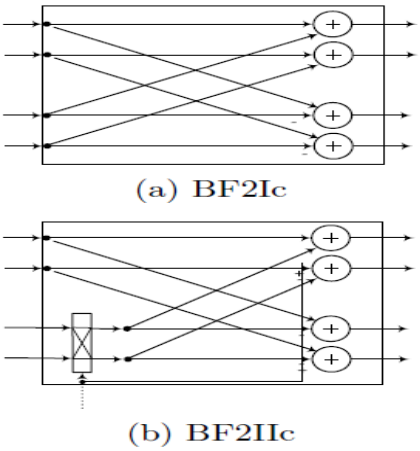

Figure 9: complex data pathof BF2IC and BF2IIc architecture

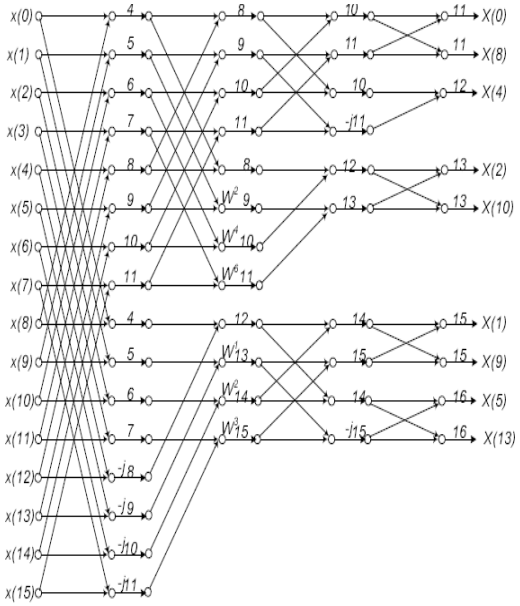

Figure 10: Simplified flow graph of a 16-point radix-2^2 DIF RFFT

The final output can be obtained by using the minimum delay elements and also the various types of multipliers. In the final stage, we need to store final signal sequence output samples.

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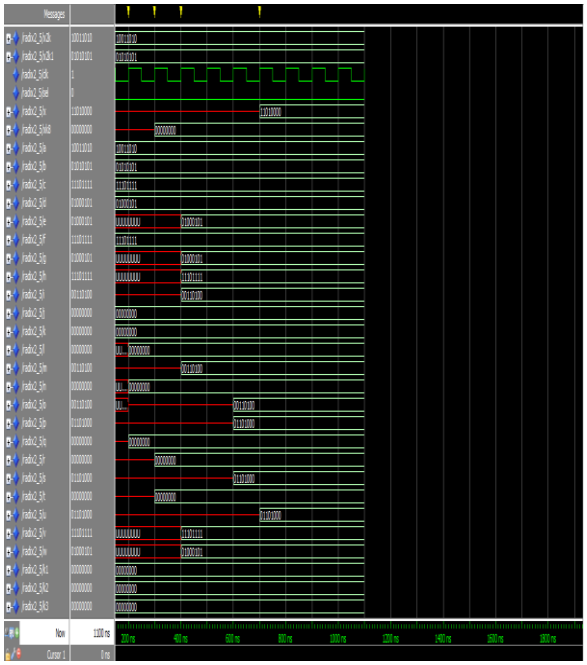

Figure 11: 16-point radix-2^2 DIF RFFT along with the proposed scheduling 2 output.

7. Conclusion

The architecture for 2-parallel Radix2^2 DIF-RFFT & CFFT for two different type of scheduling approaches small complexity in control logic. It's very useful method for signal computation process. Future work will be directed towards design of RFFT & CFFT architectures can be designed with booth multiplier, Wallace code multiplier and Vedic multiplier instead of canonic signed digit multiplier (CSD).

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